Chapter Five

Problem 5.1.

Since the gate of MOSFET is connected to +2V constant voltage source by a resistor, the MOSFET will be in strong inversion. From the circuit shown in Figure P5.1, the drain, source and body of this MOSFET are all connected to ground. Hence, the MOSFET in this circuit acts as a capacitor. The capacitance is

$$C_{tot} = C'_{ox} \times W \times L = (800\text{aF}/\mu\text{m2}) \times 150\ \mu\text{m} \times 150\mu\text{m} = 18\text{pF}$$

For the 1mv AC input, the AC out

$$V_{out} = V_{in} \times (1/j2\pi fC_{tot}) \,/\, [R + (1/j2\pi fC_{tot})] = V_{in} / (1+ j2\pi fRC_{tot})$$

The amplitude of Vout is $1\text{mv}/[1+(2\pi \times 10\text{MHz} \times 250\text{k}\Omega \times 18\text{pF})^2]^{0.5} \approx 0.003535\text{mv} =$ <u>$3.535\mu\text{v}$</u> @ 10MHz, and the phase of this output voltage is $\tan^{-1}(-282.743) =$ <u>$-89.8°$</u>

Problem 5.2

Ans: From Eq (5.8), the number of acceptor atoms in the substrate

$$N_A = n_i \exp(|\phi_F|\, q/KT) = 8.354 \times 10^{14}\ \text{atoms/cm}^3$$

Use Eq (5.20),

$$C'_{ox} = (2 \times q\varepsilon_{si} N_A)^{0.5}/\lambda = 369.72\ \text{aF}/\mu\text{m}^2$$

The KP of this n-channel MOSFET is

$$KP = \mu_n \times C'_{ox} = 550\text{cm}^2/\text{V} \times 369.72\ \text{aF}/\mu\text{m}^2 = 20.33\mu\text{A/V}^2$$

From Eq. (5.36), $\beta = KP \times W/L = 20.33 \times 10/2 = 101.56$
From Eq. (5.21), $V_{THN} = 0.8\text{V} + 0.45 \times ((.57+1)^{0.5} - (.57)^{0.5}) = 1.024\text{V}$

Since $V_{DS} > V_{GS} - V_{THN}$ and $V_{GS} > V_{THN}$, the MOSFET is operated in saturation region. With λ=0, use Eq (5.39),

$$I_D = \beta\,(V_{GS} - V_{THN})^2 / 2 \approx \underline{48.4\mu\text{A}}$$

If use CN20 process, the C'_{ox} is 800 $\text{aF}/\mu\text{m}^2$, and $KP = 44\ \mu\text{A/V}^2$, $I_D = 104.78\mu\text{A}$

Problem 5.3

Since the MOSFET is operated in the strong inversion, a large amount of electrons are attracted under the gate, and an induced channel is formed below gate oxside. This channel connects source and drain, so the gate overlap of the source/drain has no effect on the capacitance. The capacitance between gate electrode and the source/drain electrode is simply <u>$C_{ox} = C'_{ox} \bullet W \bullet L$</u>

Problem 5.4

When the MOSFET is operating in the accumulation region, a lot of holes are attracted below the gate oxide. There is no induced channel between source and drain. Therefore, the capacitance between gate and source/drain is equal to overlap capacitance, $\varepsilon_{ox} \bullet W \bullet LD / TOX$.

Problem 5.5

$C'_{ox} = \varepsilon_{ox} / TOX = (8.85 \times 3.97\ aF/\mu m) / (400 \times 10^{-10}\ m) = \mathbf{878.4 aF/\mu m^2}$

Problem 5.6

From Ex 5.2, the electrostatic potential of the substrate ϕ_F is -290mV. With V_{SB}=2V, the electrostatic potential at the oxide interface $\phi_S = -\phi_F + V_{SB} = 2.29V$ @ $V_{GS} = V_{THN}$, and the depletion layer width

$$X_d = [\,2 \times 11.7 \times (8.85aF/\mu m) \times (2.29 + .29)V / (1.6 \times 10^{-19} \times 10^{15})]^{0.5} \approx 1.83\mu m$$

The charge contains in this region is

$$Q'_b = qN_AX_d = 292.8\ aC/\mu m^2$$

Problem 5.7

For the p-channel model, with $N_D = 10^{16}$ atoms/cm^3,

$$\gamma \approx 0.721V^{0.5}$$

while the γ given in the level 2 SPICE model is 0.7327 (GAMMA). The doping concentration of the nwell is very close to BSIM model's results.

Problem 5.8

The electrostatic potential of the oxide semiconductor interface when $V_{GS} = V_{THNO}$ is: $\phi_S = -\phi_F = \frac{kT}{q} \ln \frac{N_A}{N_i}$

Where N_A is the number of acceptor atoms in the substrate, N_i is the intrinsic carrier concentration of silicon.

Problem 5.9

From Ex 5.5, without soduim contamination,

Let $V_{THN0} = -126mV + qN_I/ C'_{ox} = 0.8V$. Plug into $C'_{ox} = 800\ aF/\mu m^2$ and $q = 1.6 \times 10^{-19}$ C/atom,

Problem 5.10

With soduim contamination of N_S=100×10^9 ions/cm^2, the threshold voltage is

$$V_{THN0} = -126mV - qN_S/C'_{ox} + qN_I/C'_{ox}$$
$$= 0.8V - 1.6\times10^{-19}C/ion \times 100\times10^9\ ions/cm^2 \times 800aF/\mu m^2$$
$$= 0.8V - 0.2V = \underline{\mathbf{0.6V}}$$

then the threshold voltage will decrease 200mV, for Problem 5.9, to 0.6V.

Problem 5.11

Assume the MOSFET is operating in strong inversion, $V_{GS} > V_{THN}$. The total charge available in the channel, for conduction of a current between the drain and the source, is given by Eq. (5.28), where the V(y) is V_{DS}. When $V_{DS} = V_{GS} - V_{THN}$, the inversion charge under the gate at the drain-channel juctioin is zero. The enhanced electrons are attracted by positive V_{DS} and cause the drain-channel to pinch off. The MOSFET is in its saturation region.

Problem 5.12

For p-channel MOSFET, from figure 5.9, assume all voltages are positive, i.e. using V_{SG}, V_{SD} to replace V_{SG} and V_{SD}. The total charge available in the channel for conduction is $Q'_I(y) = C'_{ox} \times (V_{SG} - V(y) - V_{THN})$, and the differential resistance of the channel region is given by

$dR = dy/[W\times \mu_p \times Q'_I(y)]$, and transconductance parameter is $KP_p = \mu_p \times C'_{ox}$

$dV(y) = I_D \bullet dR$

$I_D \bullet dy = W \times KP_p (V_{SG} - V(y) - V_{THN}) \bullet dV(y)$, integrating this equation,

$$I_D = (KP_p \times W/L) \times [(V_{SG} - V_{THN})V_{SD} - V_{SD}^2/2]$$
$$\text{for } V_{SG} \geq V_{THN} \text{ and } V_{SD} \leq V_{SG} - V_{THN}$$

Problem 5.13

Since every MOSFET shown in Figure P5.13 has the same V_{DS}, V_{GS}, KP, L and V_{THN}, the current flowing through every MOSFET is

$$I_{Dn} = (KP\times W_n\times /L) \times [(V_{GS} - V_{THN})V_{DS} - V_{DS}^2/2],\ n = 1,2, ..., N$$

(neglect the body effect and for both triode and saturation region, this equation is effective.)

Therefore, the total current from drain to source is

$$I_D = [KP\times(W_1+W_2+...+W_N)/L] \times [(V_{GS} - V_{THN})V_{DS} - V_{DS}^2/2]$$

This I-V characteristic is the same as one single MOSFET with a width equal to the sum of each individual MOSFET's width.

Problem 5.14

From Figure 1, P5.14,
Vgs1=Vg, Vds1=V1, Vgs2=Vg-V1, Vds2=Vd-V1

If M1 operates in the saturation region, then
Vds1≥Vgs1-Vthn, i.e. V1≥Vg-Vthn

For M2, Vgs2-Vthn=Vg-V1-Vthn ≤ 0

Under this condition, M2 is either in cutoff or just into the invertion region, so the current flowing through M2 is zero or very small. Since M2 and M1 are in a series connection, M1 cannot operate in the saturation region.

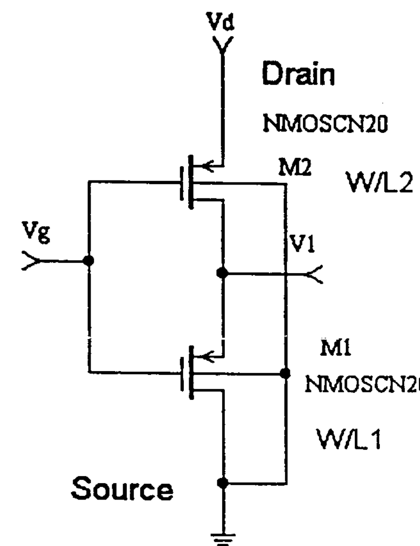


Figure 1: P5.14

Problem 5.15

From Figure P5.14, we assume that both MOSFET are in the triode region. Neglecting the body effects,

1) $I_D \times L1/(KP\times W) = (Vgs1 - Vthn)\,Vds1 - Vds1^2/2 = (Vg - Vthn)V1 - V1^2/2$

2) $I_D \times L2/(KP\times W) = (Vgs2 - Vthn)\,Vds2 - Vds2^2/2$

$$= (Vg - Vthn - V1)(Vd-V1) - (Vd-V1)^2/2$$

1)+2)

$$I_D \times (L2+L1)/(KP\times W) = VgVd - VthnVd - Vd^2/2 = (Vg - Vthn)Vd - Vd^2/2$$

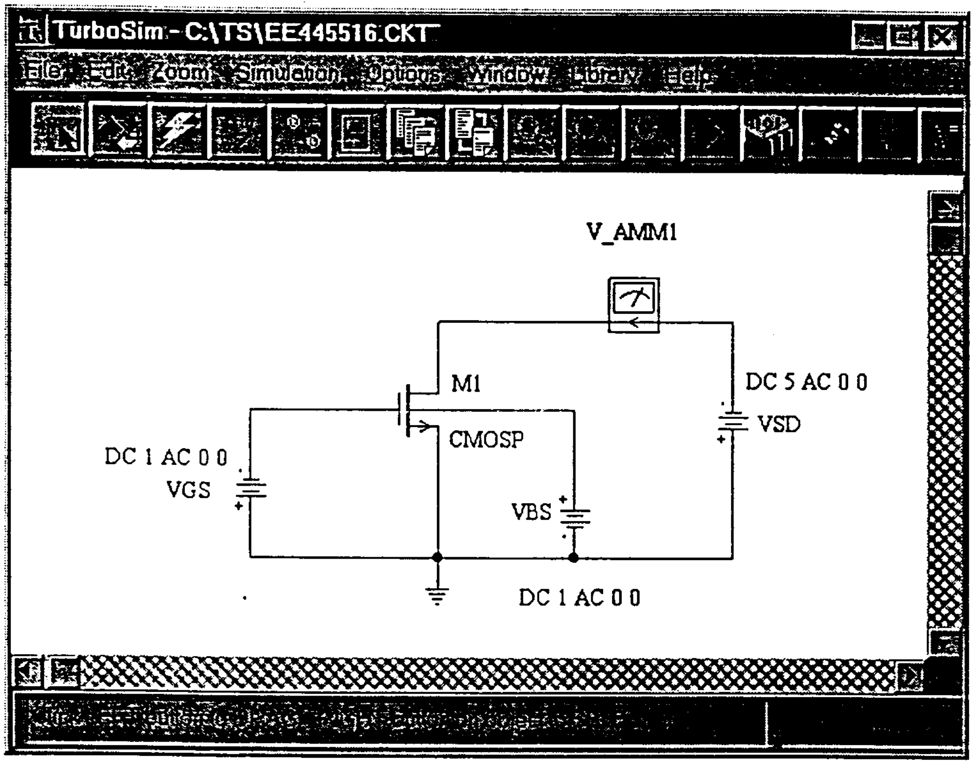
Re-arranging this equation,

$$I_D = [KP\times W/(L2+L1)] \times [(V_{GS} - V_{THN})V_{DS} - V_{DS}^2/2]$$

From this equation, Figure P5.14 does behave as a single MOSFET with the length equal to the sum of the individual MOSFET's length.

Problem 5.16

Using SPICE and the level 2 model given in Appendix A for the p-channel MOSFET, plot I_D versus V_{SG} for V_{BS} changing from 0 to 5V and V_{SD} =5V. Assume the device W=L=5μm.



*** (TurboSim V 1.87) Netlist for C:\TS\EE445516.CKT

*** Top Level Netlist ***
M1 6 10 0 14 CMOSP L=5u W=5u
V_AMM1 17 6 0V
VBS 14 0 DC 1 AC 0 0
VGS 0 10 DC 1 AC 0 0
VSD 0 17 DC 5 AC 0 0

***** Spice models and macro models *****

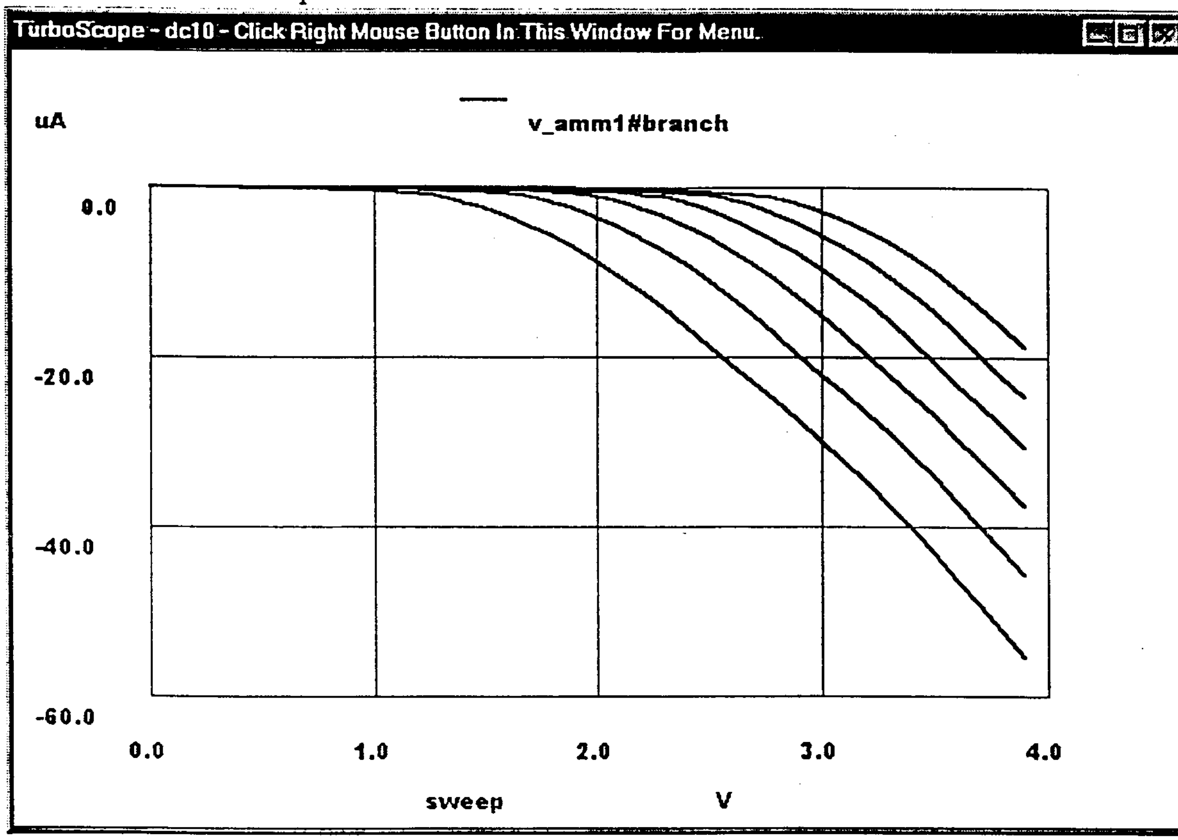
.MODEL CMOSP PMOS LEVEL=2 model in App. A

***** End of spice models and macro models *****

.DC VGS 0 4 .1 VBS 0 5 1
.end

(Problem 5.16 continued)

Simulation results for problem 5.16.



Problem 5.17

Lay out eight MOSFETs in parallel, and W/L for each MOSFET is 25/2 (μm)
For device 200μm×2μm, this layout uses two standard cellframes. The drain area is 25μm×8μm each. For the source area, the leftest and rightest ones are 25μm×7μm, and the others are 25μm×8μm.

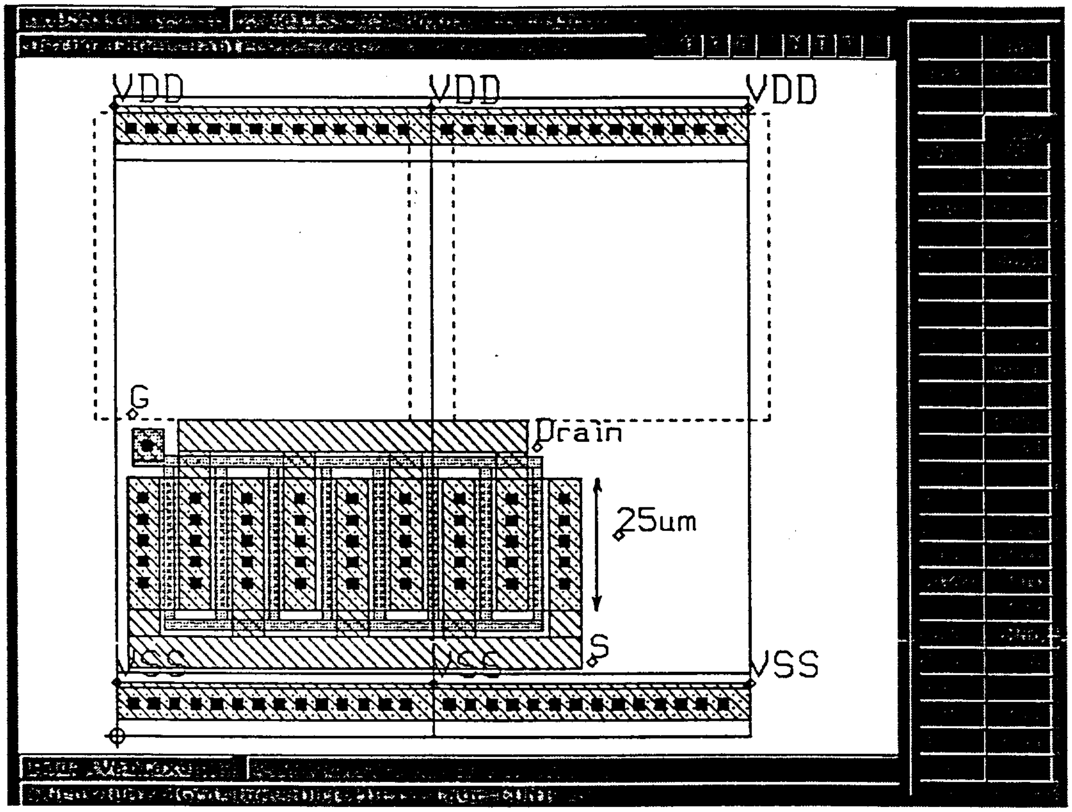


Figure: P5.17 Layout a MOSFET

Problem 5.18

For each MOSFET in Figure P5.17, the area of the drain is 25μm×8μm, and the total area of drain is $4\times200\text{pm}^2 = 800\text{pm}^2$; the perimeter is 264μm. For the source, the area is $(2\times175+3\times200)\ \text{pm}^2 = 950\text{pm}^2$; the perimeter is 390μm. The number of squares in the drain and souce regions are NRD=4×25/8=12.5 and NRS=2×25/7+3×25/8=16.5 respectively. Therefore, the SPICE statement for problem 5.17 is

CMOSN L=2u W=200u AD=800p AS=950p PD=264u PS=390u NRD=12.5 NRS=16.5

Problem 5.19

For the Fig. P5.19, the layout of an n-channel MOSFET is equal to 5 MOSFETs, each with W/L=4/25, connected serially. Therefore, the device's width is 4 μm and length is 5×25=125μm.