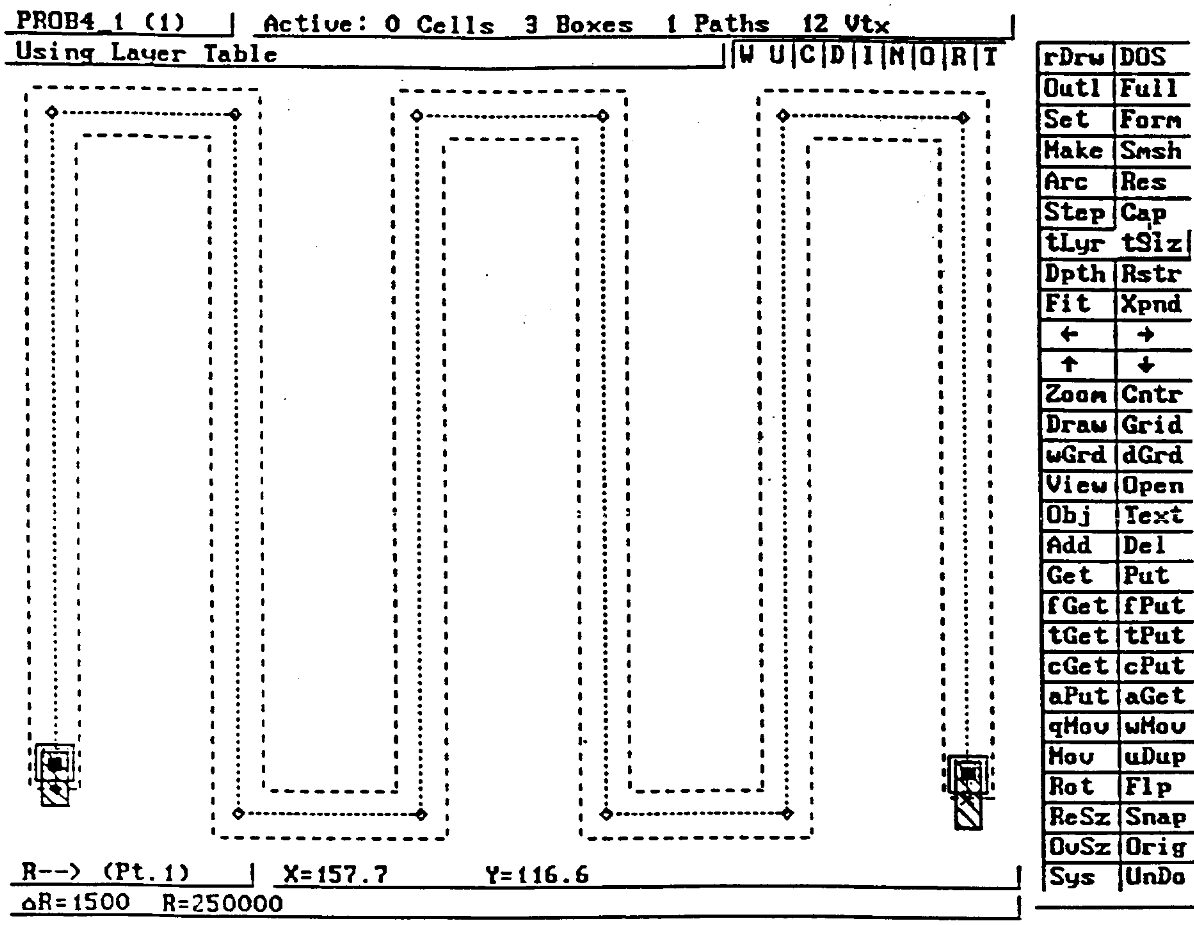
CHAPTER FOUR

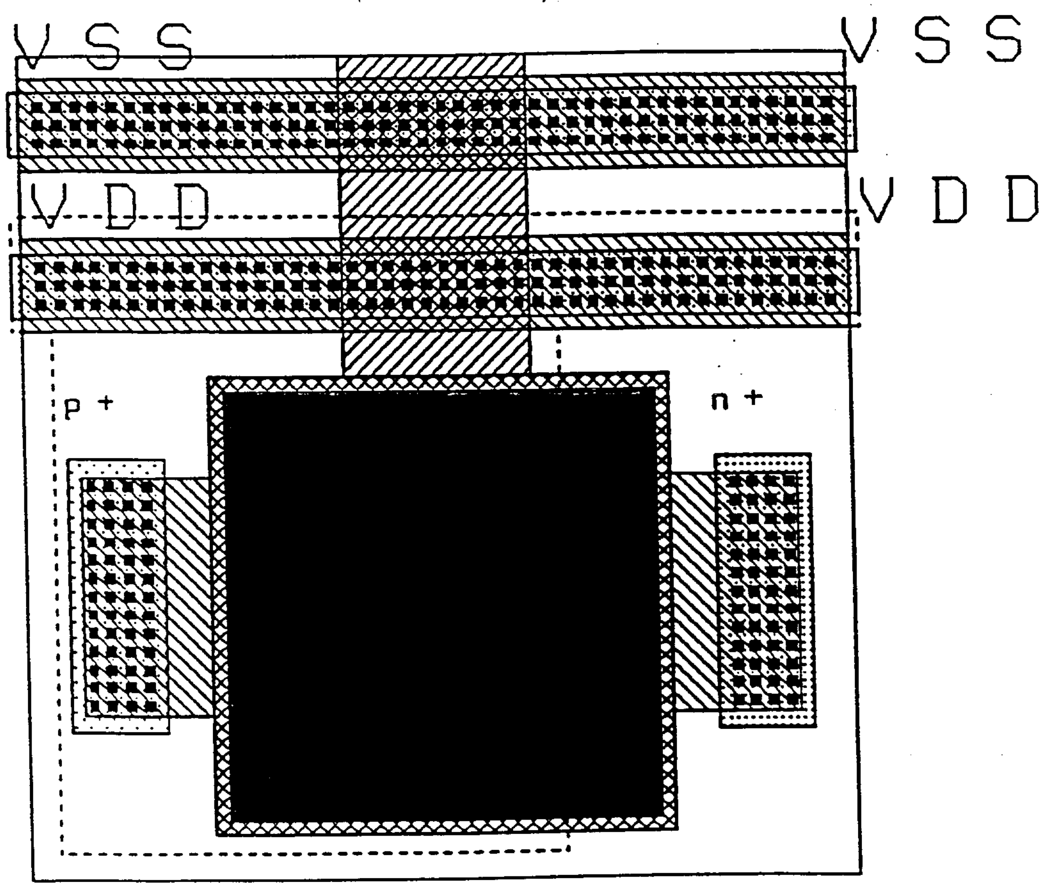
Problem 4.1



If the layout did not include n+ under the contacts, a rectifying or schottky diode is formed.

Problem 4.2

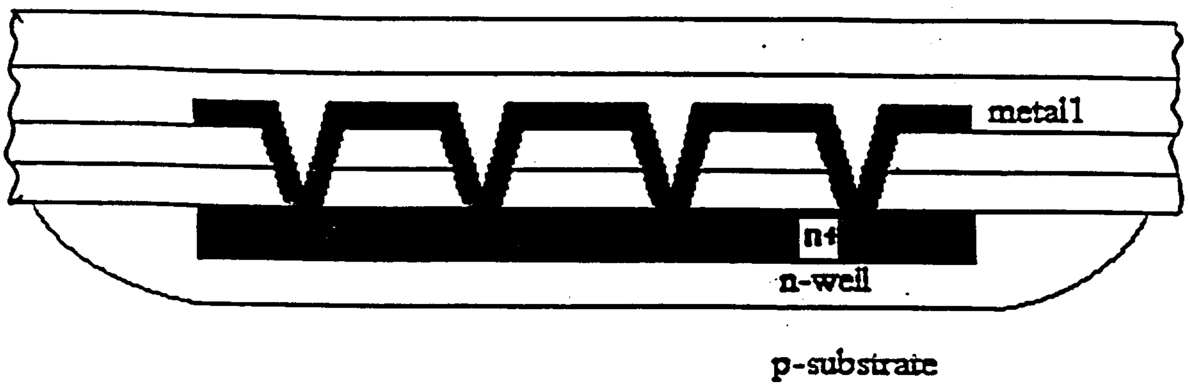
Layout and DRC the pad of figure 4.6. Show it in the following figure:



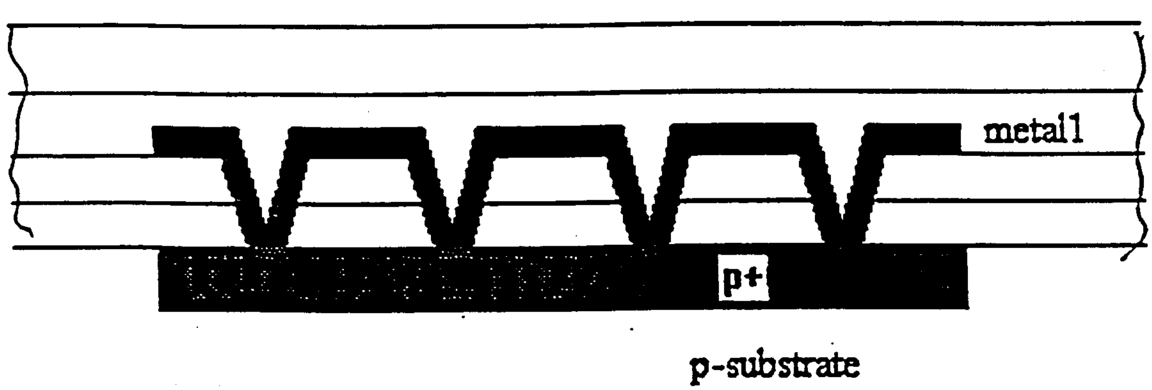
The top diode in the figure 4.5 of page 67 is made of by using the n-well under VDD above figure and the p+ located in the left part of above figure. The bottom diode is made of by using the substrate under the above VSS with n+ in the right part of above figure. These two diodes can pull the excessive charge away from the MOSFET gate for ESD protection.

Problem 4.3

The cross sectional view across the VDD power bus of the standard cell frame of figure 4.9.



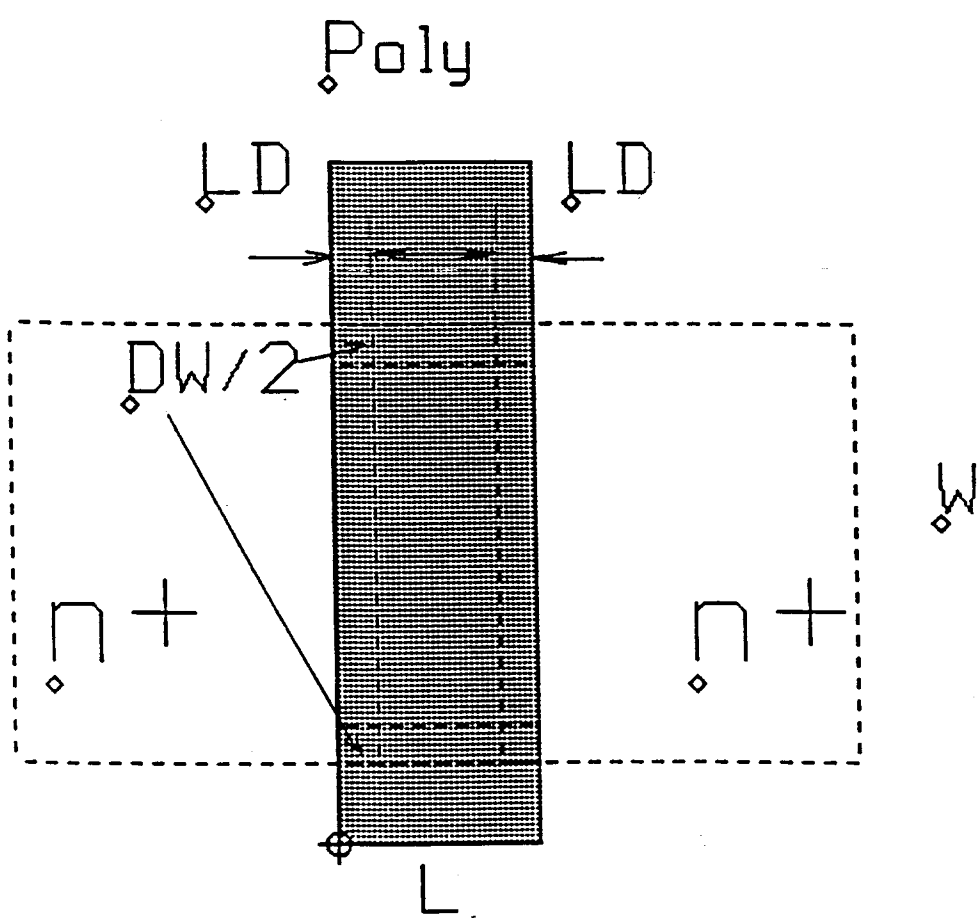
The cross sectional view across the VSS power bus of the standard cell frame of figure 4.9.



Problem 4.4

a. From the BSIM model parameters for the p-channel MOSFET in appendix A, DW (dw) = 0.162551 μm.

b. The oxide encroachment does not affect the length of the MOSFET. From the following layout, the location of the oxide encroachment can illustrate this clearly.

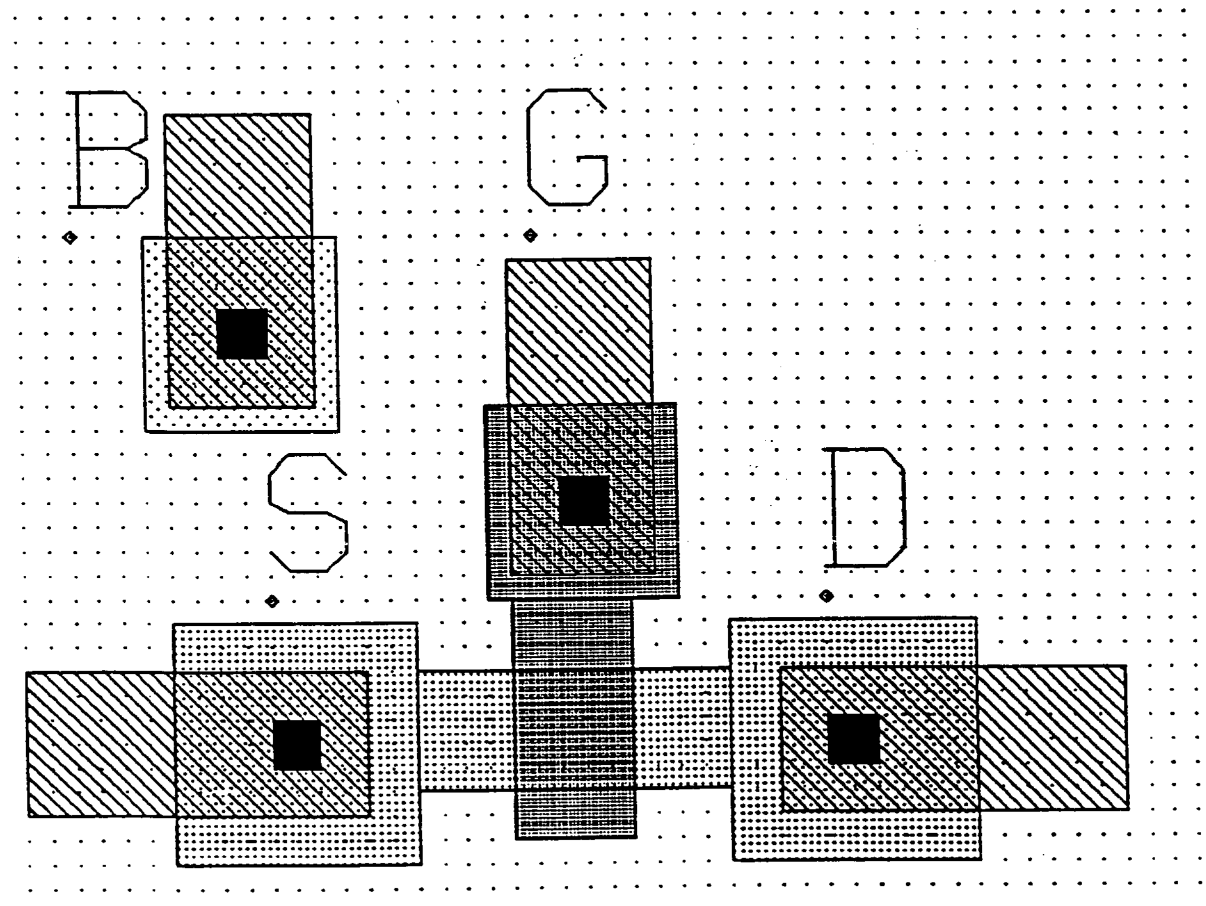


Problem 4.5

a. From the BSIM model parameters for the p-channel MOSFET in appendix A, DL (dl) = 0.84424 μm.

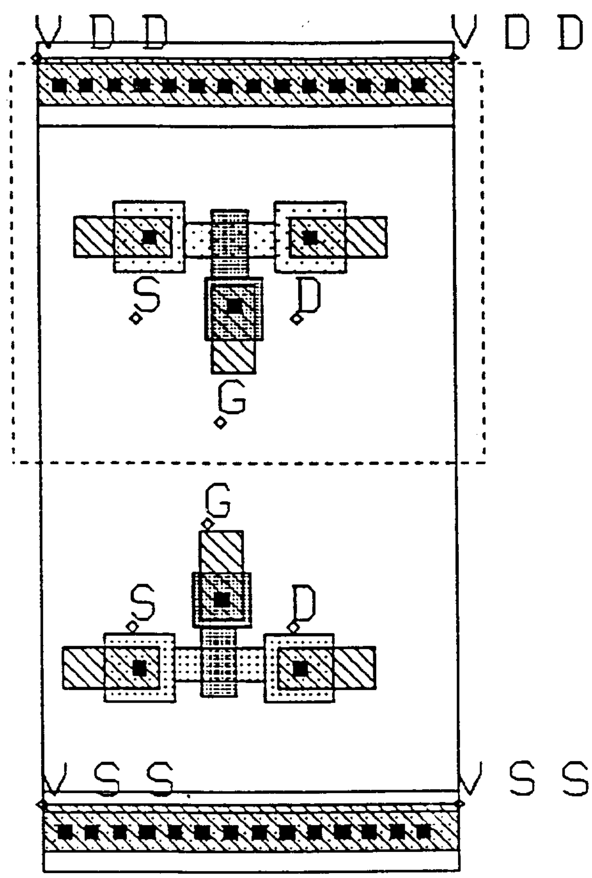
b. The lateral diffusion does not affect the width of the MOSFET. From the above layout, the location of the lateral diffusion can illustrate this clearly.

Problem 4.6



The above layout has been passed through DRC.

Problem 4.7



Yes, the P-substrate and well are connected to VSS and VDD respectively. The connection are made through p+ and n+ respectively.

Problem 4.8

cj of n+ inplant is $1.0375\text{x}10^{-4}$F/m^2, and cjsw is $2.1694\text{x}10^{-10}$F/m, from page 710 and also page 77, A_D=10x10 μm^2, P_D=4x10 μm, therefore, the maximum capacitance, i.e. the zero bias depletion capacitance=$1.0375\text{x}10^{-4}$F/m^2 x10x10 μm^2 + $2.1694\text{x}10^{-10}$F/m x40 μm =10.375 fF +8.6776 fF = **19.0526 fF.** This depletion capacitance will decrease if the n+ inplant is held at a constant potential and the substrate is reduced.

Problem 4.9

The R = R_{square}x L/W= 21Ω / □ x 1000/2 = 10.5 kΩ; while C = 100 fF x 1000/10 =10 pF, so the delay t = 0.35 x 10.5k x 10 p = **36.75ns**.

Problem 4.10

The cross-sectional views of Fig. P4.10 are shown in Figure P4.10a and P4.10b.

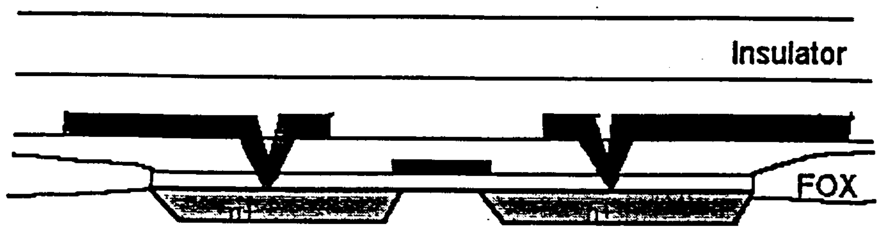


Figure P4.10a.

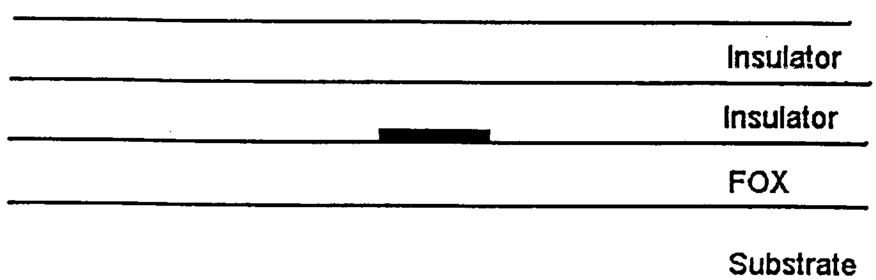
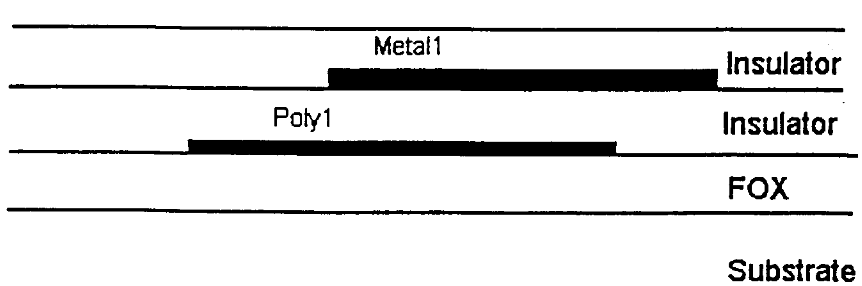


Figure P4.10b.

Problem 4.11

The cross-sectional view is shown below.



Problem 4.12.

The layout of a diode using the n+ diffusion and the p-substrate is shown in Figure P4.12a. The cross-sectional view of the diode is shown in Figure P4.12b.

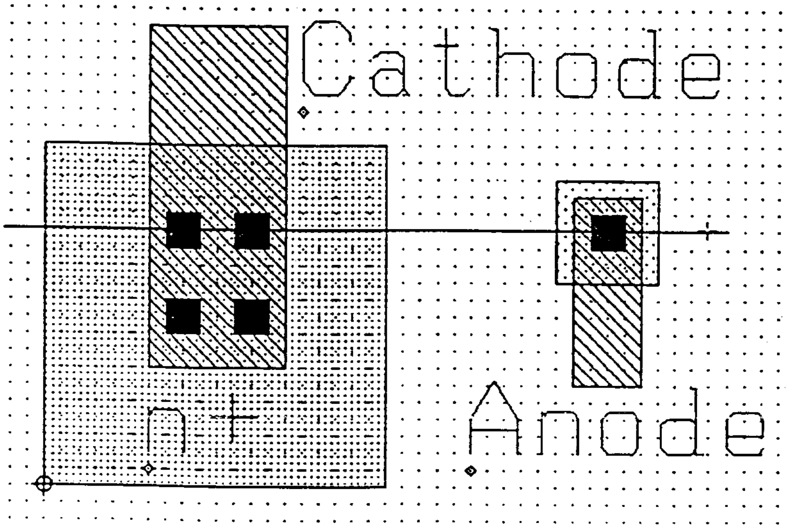


Figure P4.12a n+ and p-sub diode

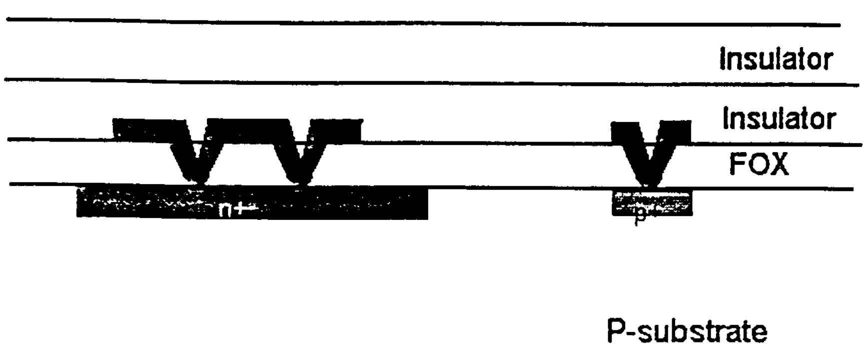


Figure P4.12b Cross-sectional view of the diode

For this diode, we can calculate the series resistance and zero bias capacitance between n+ and p-sub. From Appendix A, sheet resistance of n+ active is 27.9Ω/square, and $cj=1.0375\times10^{-4}F/m^2$, $cjsw=2.1694\times10^{-10}F/m^2$, $js=1\times10^{-8}A/m^2$

For the SPICE model, neglecting the sidewall component

$RS = 27.9 \times 20/20 = 27.9\Omega$

$CJ0 = 1.0357 \times 20 \times 20 \times 10^{-16}F \approx 41.43fF$

$IS = js\ (A/m^2) \times 20\ \mu m \times 20\ \mu m = 4aA$

(Problem 4.12 continued)

Note that the diode transit time effects have been neglected here. Since the anode of diode is connected to p-substrate by p+, which is the lowest potential in CMOS circuits (VSS), the diode will always be reverse biased.

Problem 4.13

Since MOSFET is a four-terminal device, for figure P4.13, the body of p-channel MOSFET, the n-well, must be connected to a fixed potential which is higher than VSS. We can use n+ active in the n-well and connect it to VDD. The fatal error associated with this layout is to create a floating body, which will cause big problems for this MOSFET used in circuits.