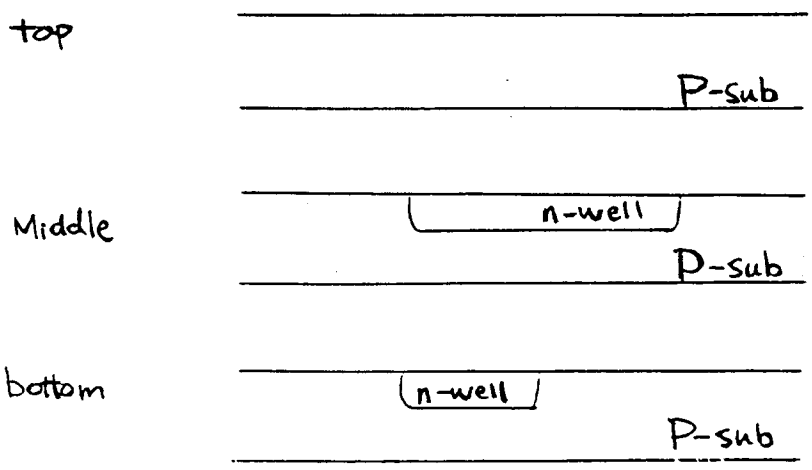
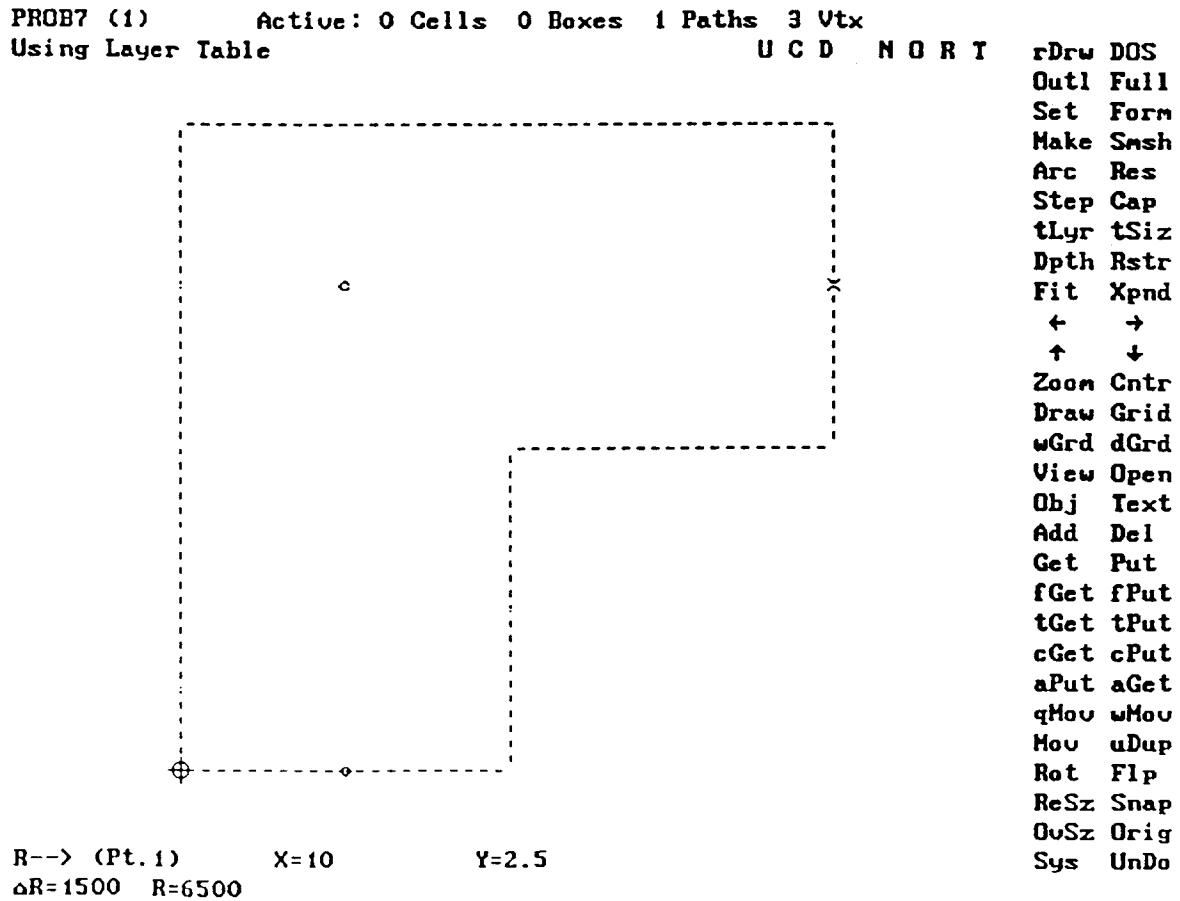
CHAPTER TWO

Problem 2.1

The cross sectional view is the following:



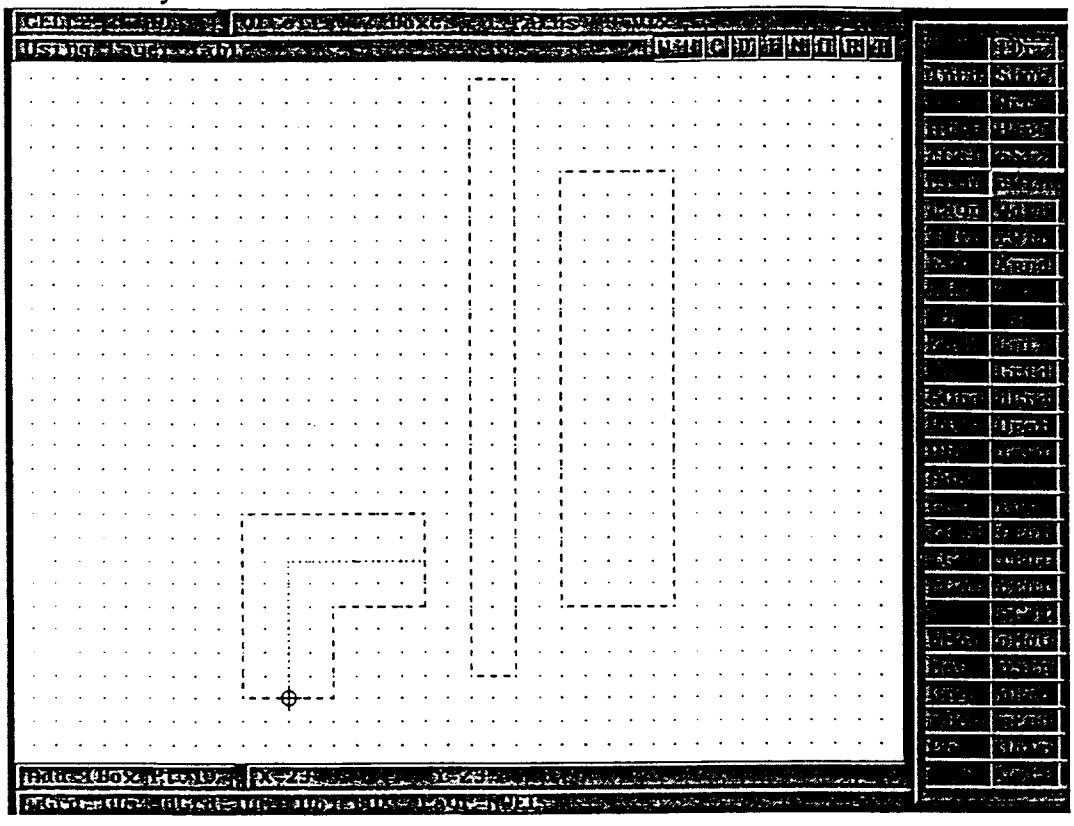
The screen result using Res is the following:



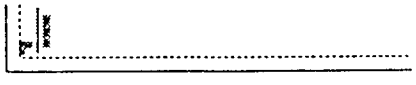
The result obtained from Res is as same as the one with the $2.6R_{min}$ used for the layout in

Problem 2.2.

Draw the layout at first.

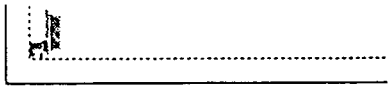


Using LASIDRC, we can find two violations:



L=-8um B=-8um

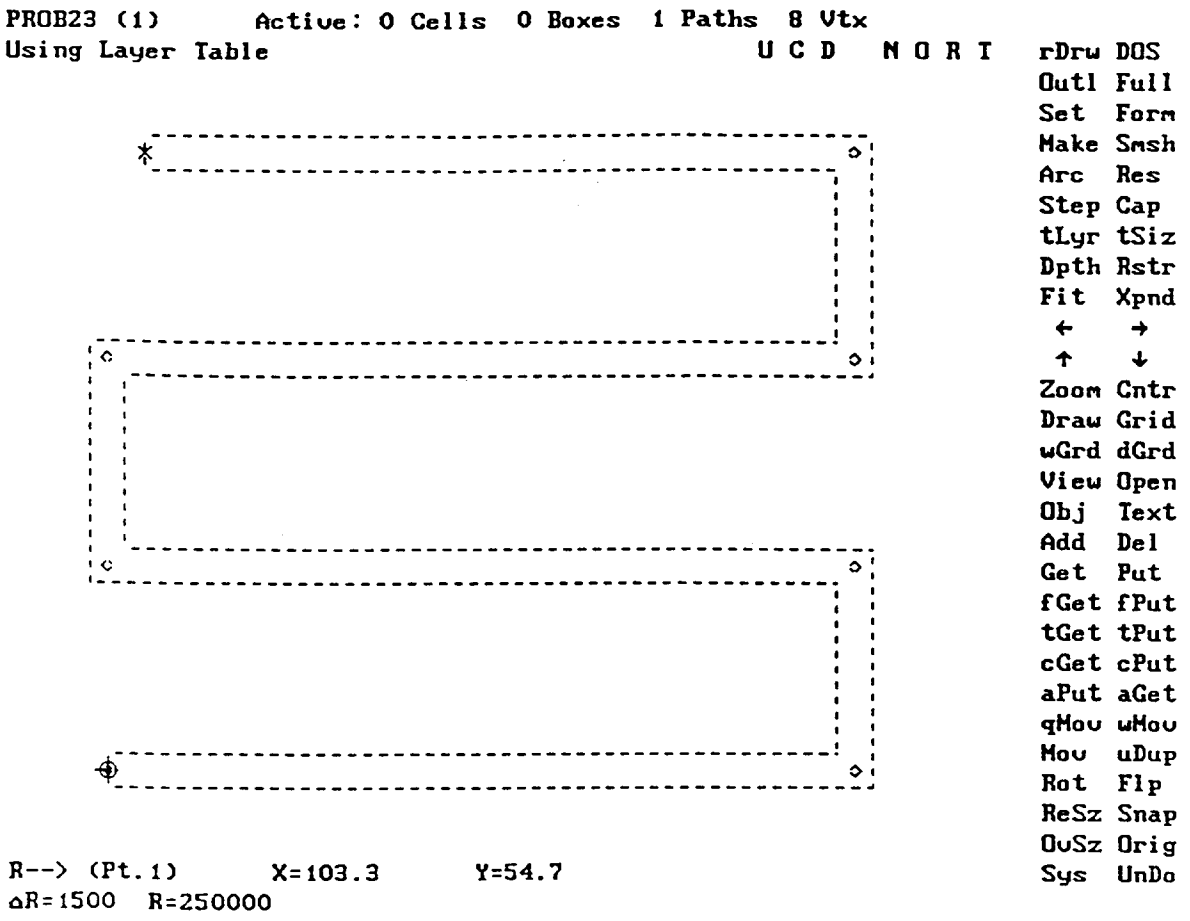
Check 1: 1.1 N-well width >=3 um (1)
Cell: CELL2-2 Date: 09/19/97 Time: 15:29:53



L=-14um B=-14um

Check 2: 1.2 N-well spacing >=9um (2)
Cell: CELL2-2 Date: 09/19/97 Time: 15:34:36

Problem 2.3



The maximum length of a segment is 86 μm, the width of the n-well is 4 μm, R=250 kΩ and the layout passed the LASIDRC check.

Problem 2.4

The minimum, typical and maximum values of the 3μm depth n-well resistivity ρ which is equal to R_{square} are 6,000 Ω·μm; 7,500 Ω·μm; and 9,000 Ω·μm respectively.

Problem 2.5

$I_s = J_s \cdot L \cdot W = 10^{-8}$ A/m^2 x 10^{-4} m x 10^{-4} m = 10^{-16} A.

Problem 2.6

$I_s = J_s \cdot L \cdot W + J_s \cdot (2L + 2W)$ depth = 10^{-8} A/m^2 x 10^{-4} m x 10^{-4} m + 10^{-8} A/m^2 x (2×10^{-4} m + 2×10^{-4} m) x 3×10^{-4} m = 1.12×10^{-16} A.

Problem 2.7.

According to Ex. 2.3,

$$C_j = C_{j0} / (1-(V_d/0.7))^{0.33} = 1.12\,pF / (1-(-1/0.7))^{0.33} = 0.8357pF$$

$$f_{3db} = 1/(2\pi RC) = 1/ (2 \times \pi \times 10k \times 0.8357pF) \approx 19\ Mhz$$

Problem 2.8.

The SPICE simulation circuit and results of Problem 2.7 are shown in Figure P2.8a and Figure P2.8b, with netlist.

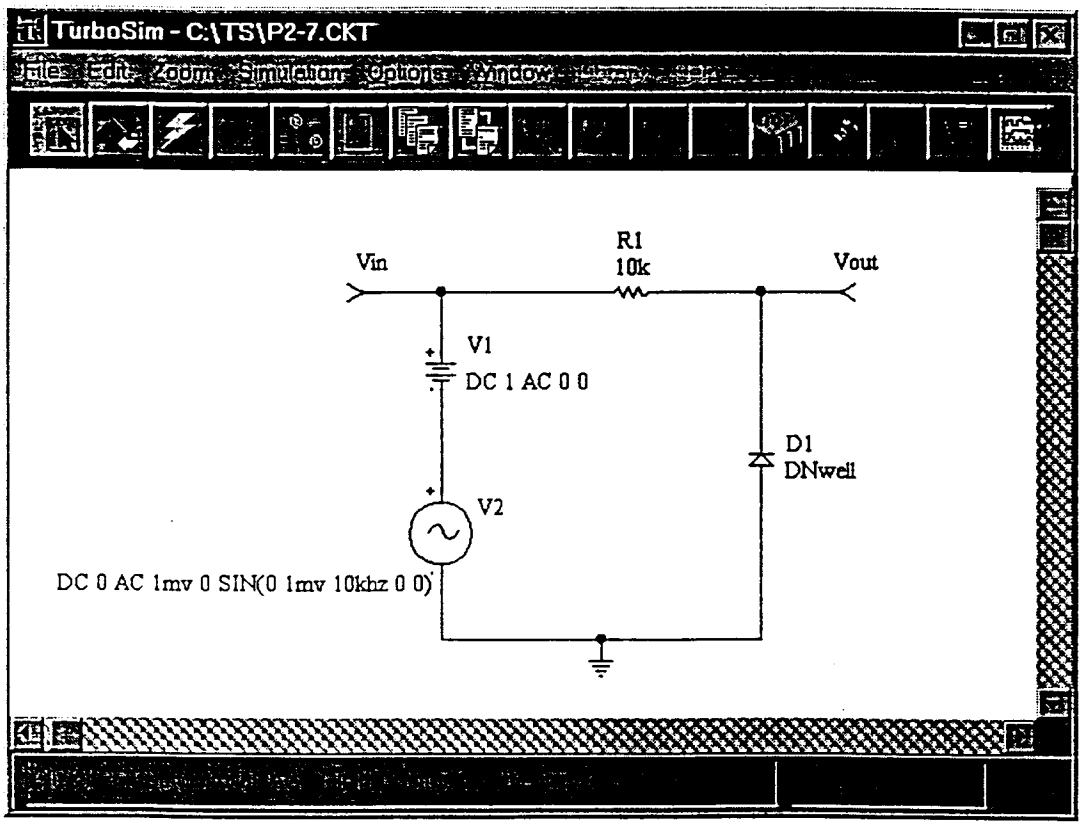


Figure P2.8a SPICE Circuit of Problem 2.7

```
*** (TurboSim V 1.87) Netlist for C:\TS\P2-7.CKT, Problem 2.8

*** Top Level Netlist ***
D1      0 Vout DNwell
R1      Vin Vout 10k
V1      Vin 4  DC 1 AC 0 0
V2      4 0    DC 0 AC 1mv 0 SIN(0 1mv 10khz 0 0)

***** Spice models and macro models *****

.Model DNwell D
+ IS=1.0E-15 TT=30e-9 CJO=1.12p VJ=.7 M=.333
***** End of spice models and macro models *****

.ac DEC 100 1MEG 100MEG
.end
```

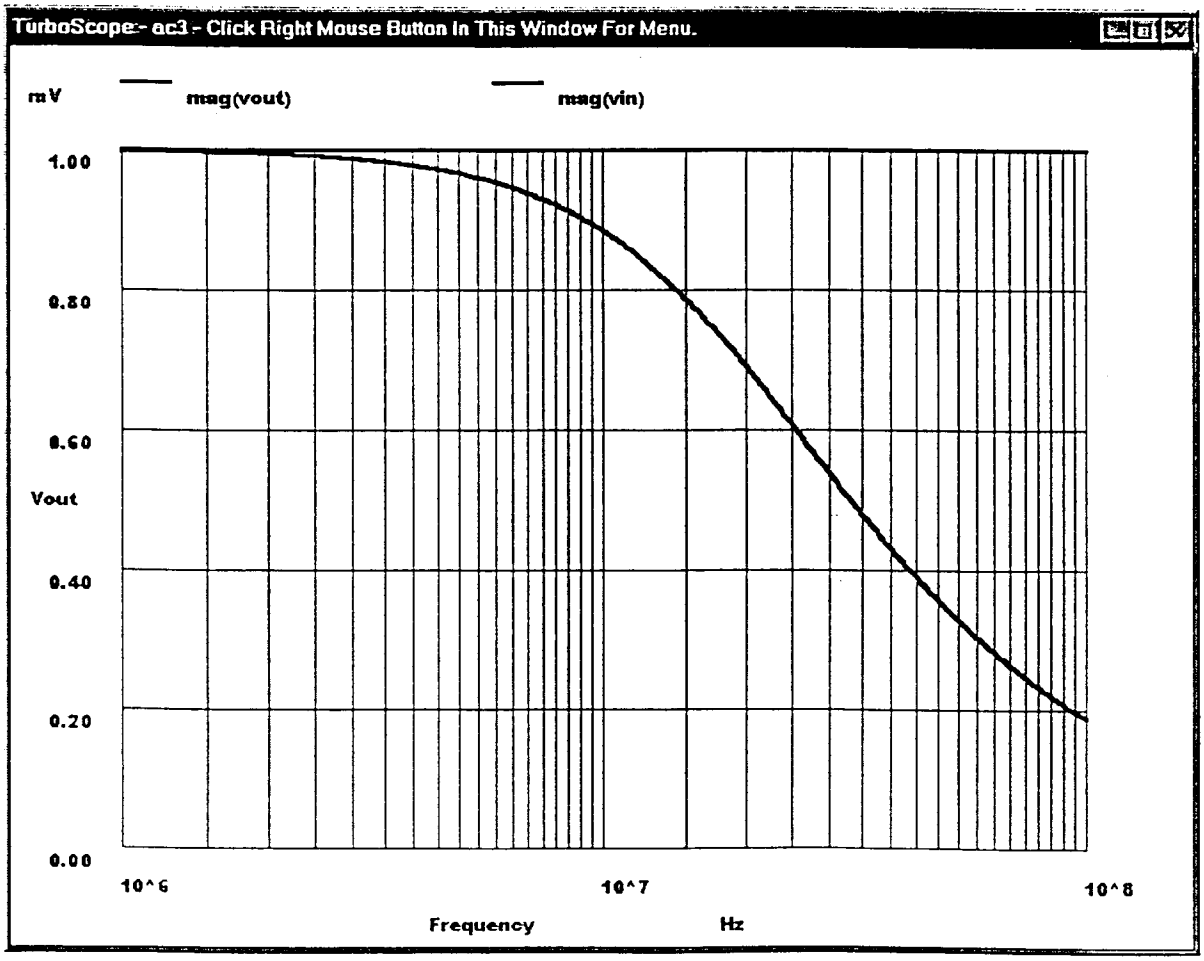


Figure P2.8b SPICE Simulation Results for Prob. 2.7

(Problem 2.8 continued)

If we zoom in the results, as shown in Figure P2.8c, we can find the frequency at 707uv voltage drop (3dB drop) is 19MHz.

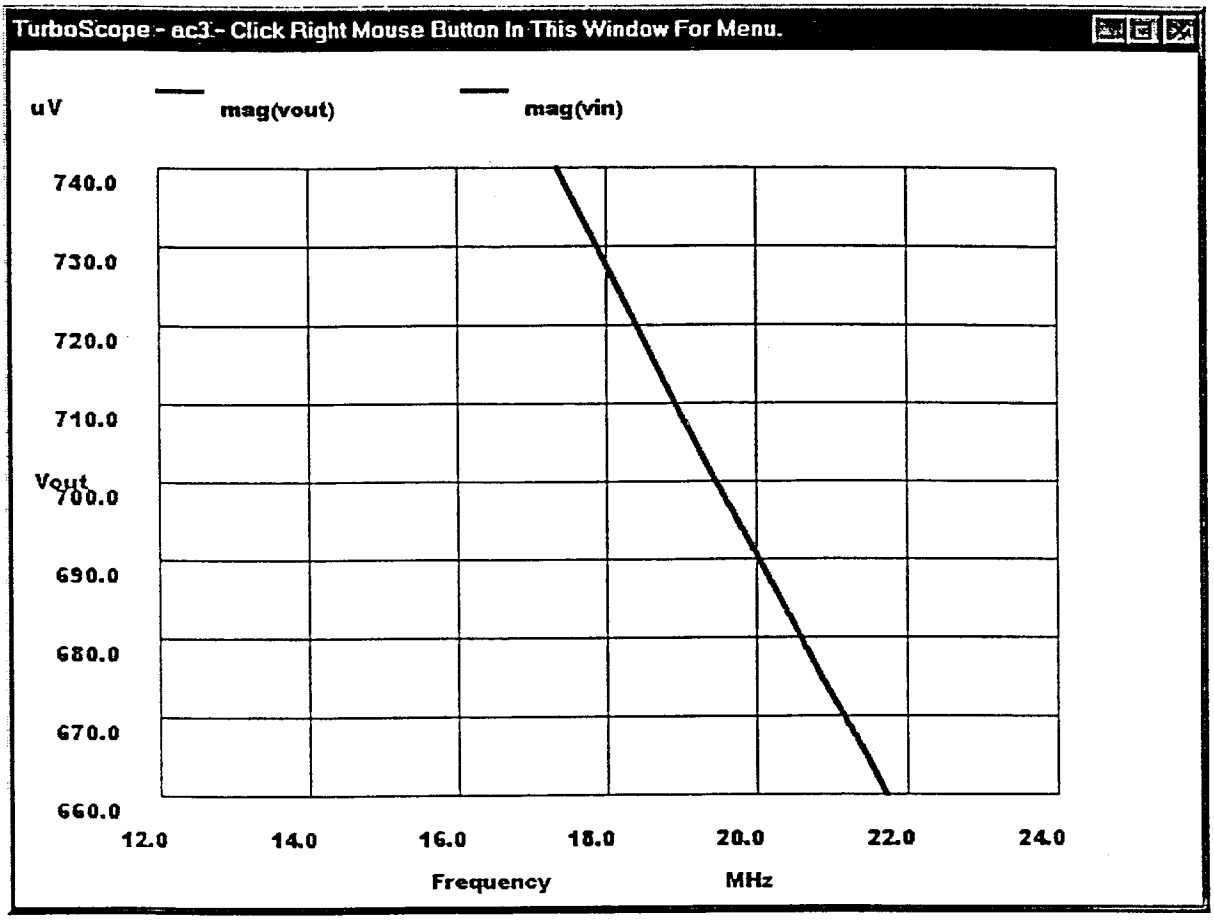
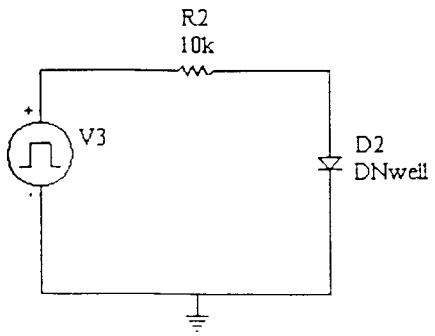


Figure P2.8c SPICE Simulation Results for Problem 2.7

Problem 2.9

Use SPICE to simulate following circuit. The results are shown in Figure P2.9.



(Problem 2.9 continued)

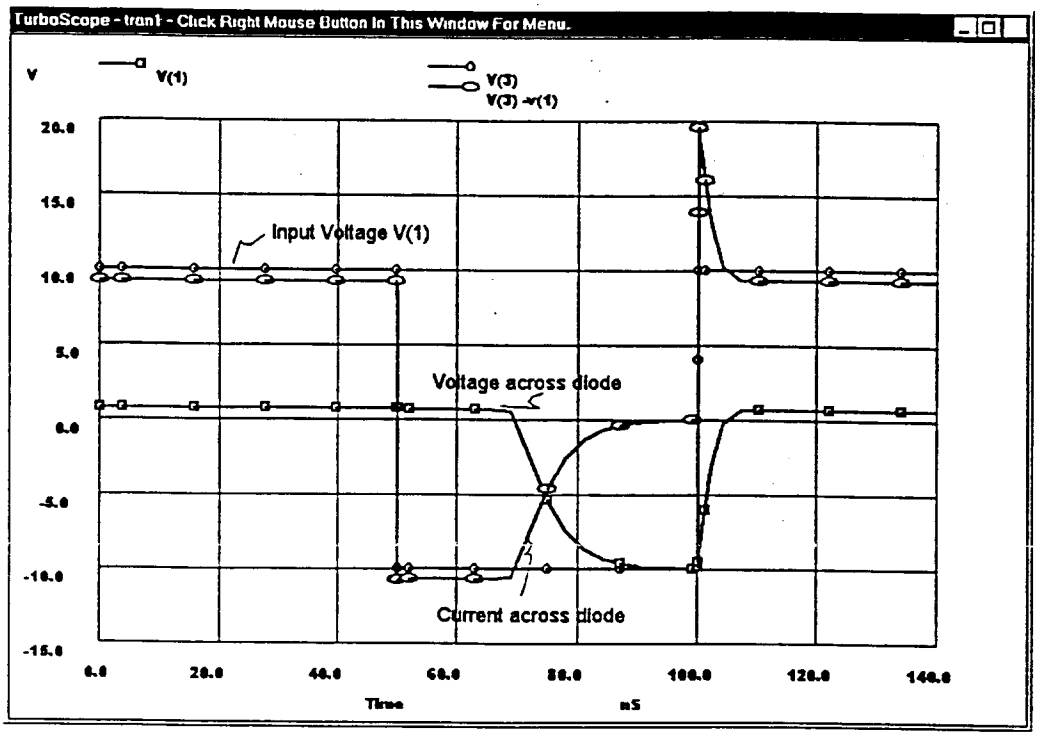


Figure P2.9 SPICE Simulation Results for Problem 2.9

From above simulation results, it can be seen that from about 50 to 58 ns, the diode is forward biased, but the current through the diode is opposite, going from cathode to anode.

Problem 2.10

For 5μm × 2000μm nwell, the capacitance C is simply the product of the bottom area of the resistor with the zero-bias depletion capacitance.

$$C = 100aF \times 5^2 \times 400 = 1pF,\ R = 1M\Omega$$

Therefore, the delay is given by

$$t_d = 0.35RC = 0.35 \times 1pF \times 1\ M\Omega = 0.35\mu s$$

Use SPICE to verify.

(Problem 2.10 continued)

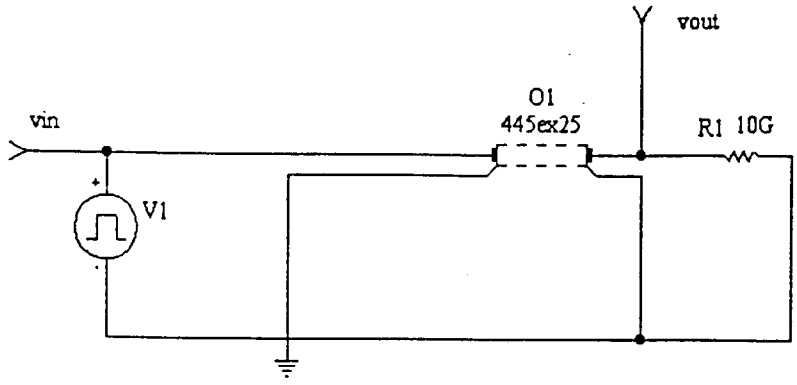


Figure: SPICE circuit for problem 2.10

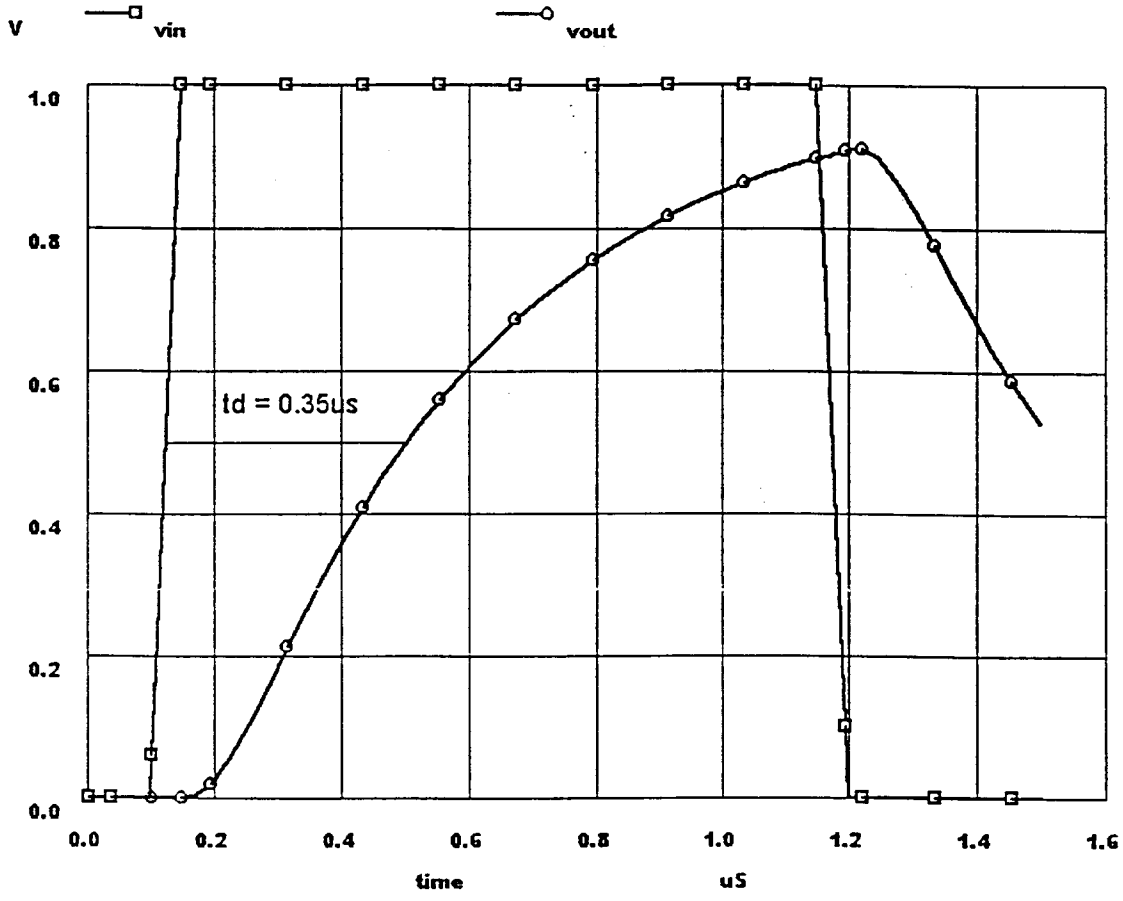
***** (TurboSim V 1.87) Netlist for Problem 2.10**

```
*** Top Level Netlist ***
O1      vin 0 vout 0 445ex25
R1      vout 0 10G
V1      vin 0   DC 0 AC 0 0 PULSE(0 1 100ns 0 0 1us 2us)

***** Spice models and macro models *****
.Model 445ex25 LTRA
+ R=1MEG C=1p LEN=1

***** End of spice models and macro models *****

.tran 50ns 1.5us 0
.end
```



From above simulation results, it can be seen that from 50 percent of input to 50 percent of output voltage signal, the time delay by this transmission line is 0.35μs.

Problem 2.11

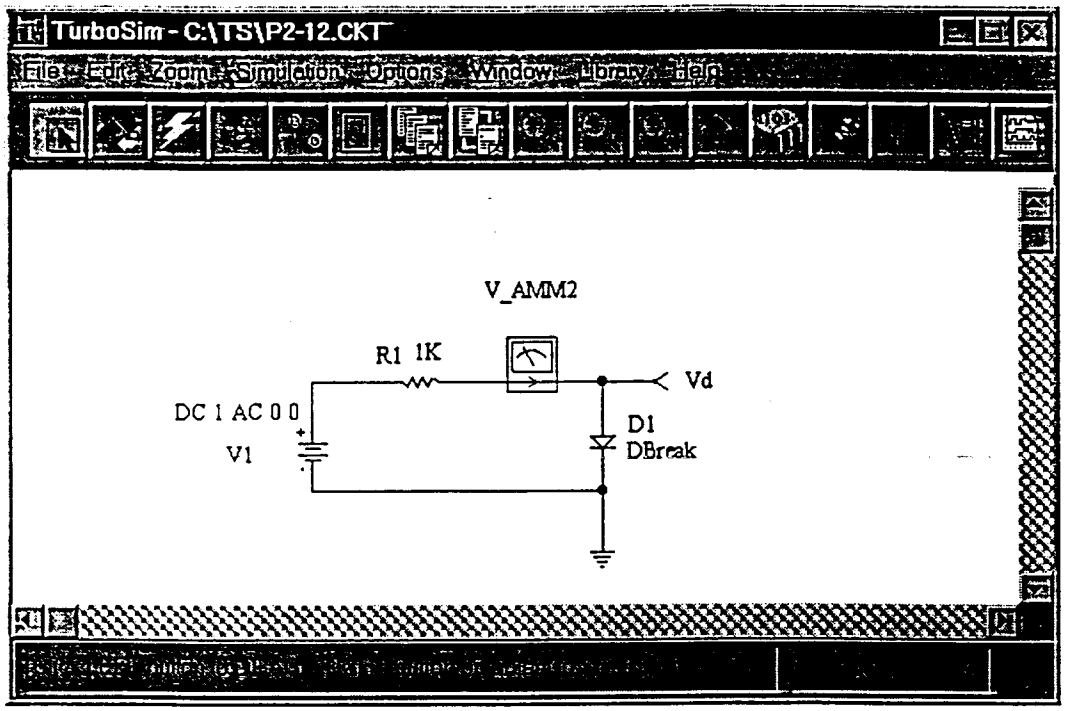
For 5μm × 2000μm nwell, assume that the resisitance does not vary with position along the resistor, the depletion capacitance C between the n-well and the substrate in the middle of the resistor is:

$C_{j0} = 100aF/\mu m^2$, $V_d = 2.5v$

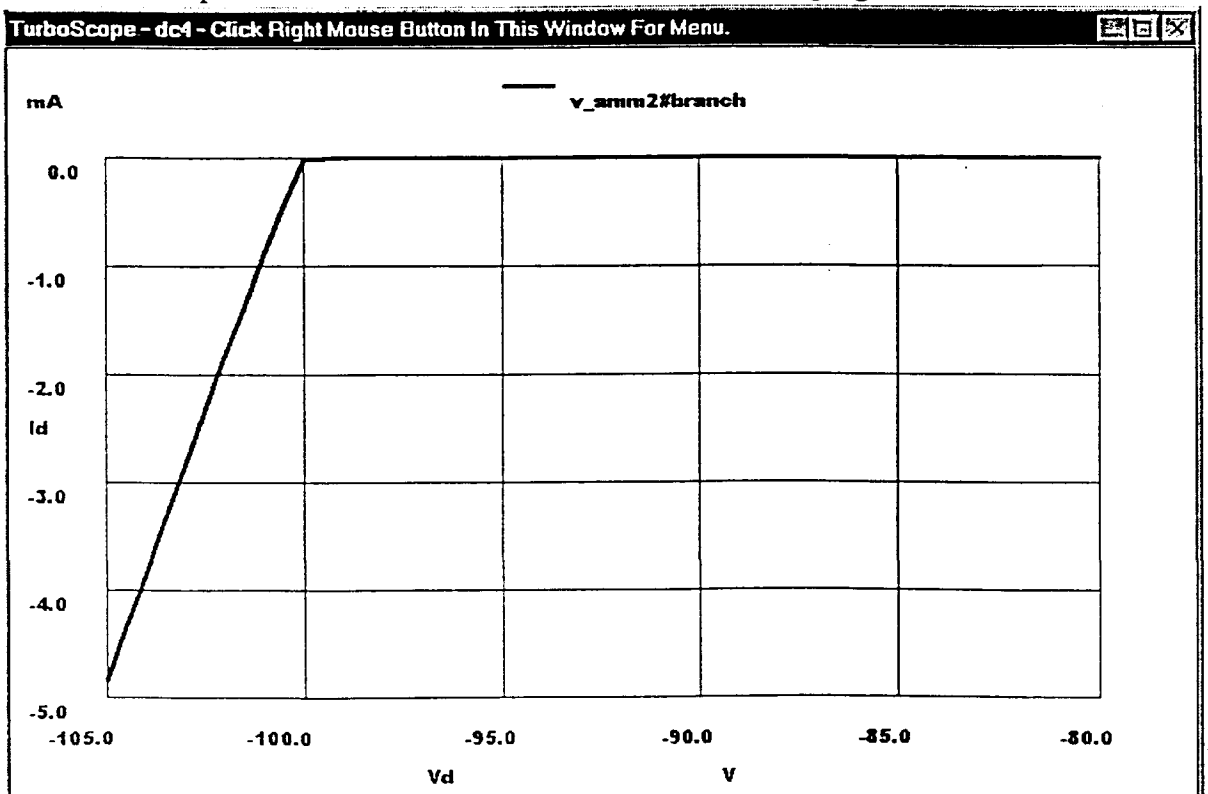
$C_j = C_{j0} / (1-(V_d/0.7))^{0.33} = 100 / (1-(-2.5/0.7))^{0.33} = 60.56aF/\mu m^2$

Problem 2.12

Use SPICE DC sweep to show the reverse breakdown characteristics of diode.

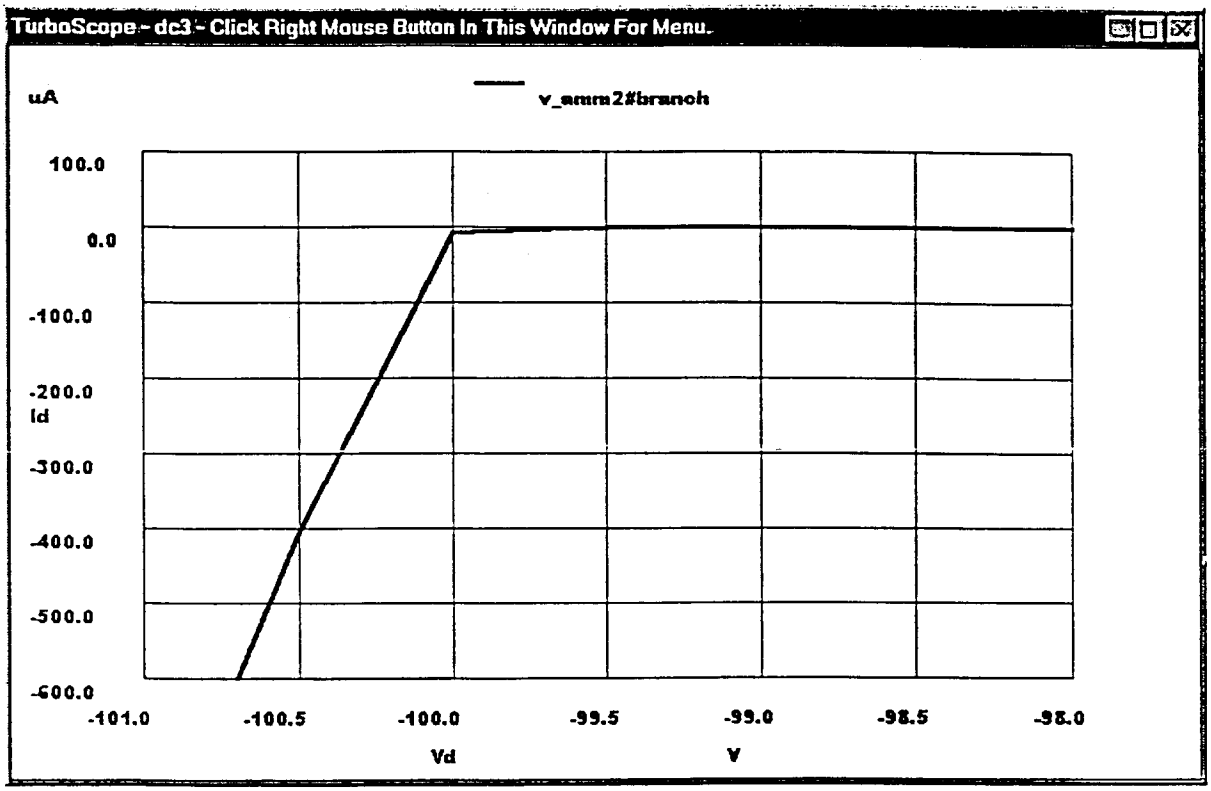


The relationship between Vd and Id is shown in the following figure.



(Problem 2.12 continued)

Zoom in the result curve around breakdown voltage (100v).



Around the breakdown voltage (-100v), the current through the diode is -10uA.

*** Netlist for C:\TS\P2-12.CKT, Problem 2.12

*** Top Level Netlist ***
D1 Vd 0 DBreak
R1 3 4 1K
V_AMM2 4 Vd 0V
V1 3 0 DC 1 AC 0 0

***** Spice models and macro models *****

.Model DBreak D
+ CJO=1E-12 BV=100 IBV=1E-5

***** End of spice models and macro models *****

.DC v1 -80 -105 -.5
.end

Problem 2.13

The build-in potential

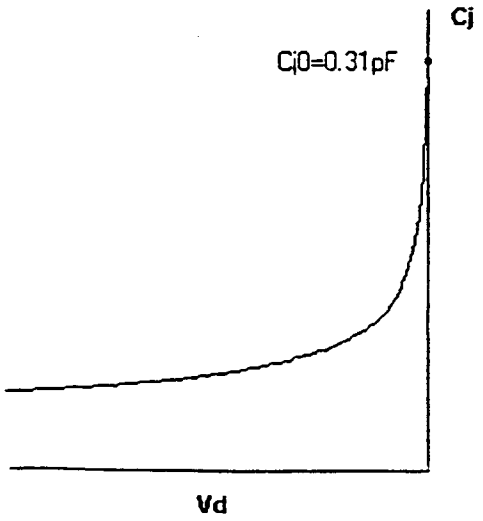
$$\phi_0 = V_T \times \ln (N_A \times N_D / (n_i)^2) = 0.026 \times \ln (10^{15} \times 10^{16} / 14.5^2 \times 10^{18}) = 0.639V$$

$$C_{j0b} = 100aF \times (50 \times 50) = 0.25pF$$

$$C_{j0s} = 100aF \times (3 \times 4 \times 50) = 0.06pF$$

Therefore, the total depletion capacitance

$$Cj = (C_{j0b} + C_{j0s}) / (1 - V_d / \phi_0)^{0.333} = 0.31pF / (1 - V_d/0.693)^{0.333}$$



Problem 2.14.

The diode storage time is given by

$$t_s = \tau_T \cdot \ln ((i_F - i_R)/(-i_R)) ,$$

$$i_F = V_F / R = (5\text{-}0.7)V / 1K\Omega = 4.3mA, \quad i_R = V_R / R = (-5\text{-}0.7)V / 1K\Omega = -5.7mA$$

Therefore,

$$t_s = 5ns \times \ln (10/5.7) \approx 2.81ns$$

Using problem 2.9 SPICE circuit, change input voltage v(1) from +5V to -5V, C_{j0} = 0.5pF, R = 1k. The simulation results are shown in Figure P2.14.

(Problem 2.14 continued)

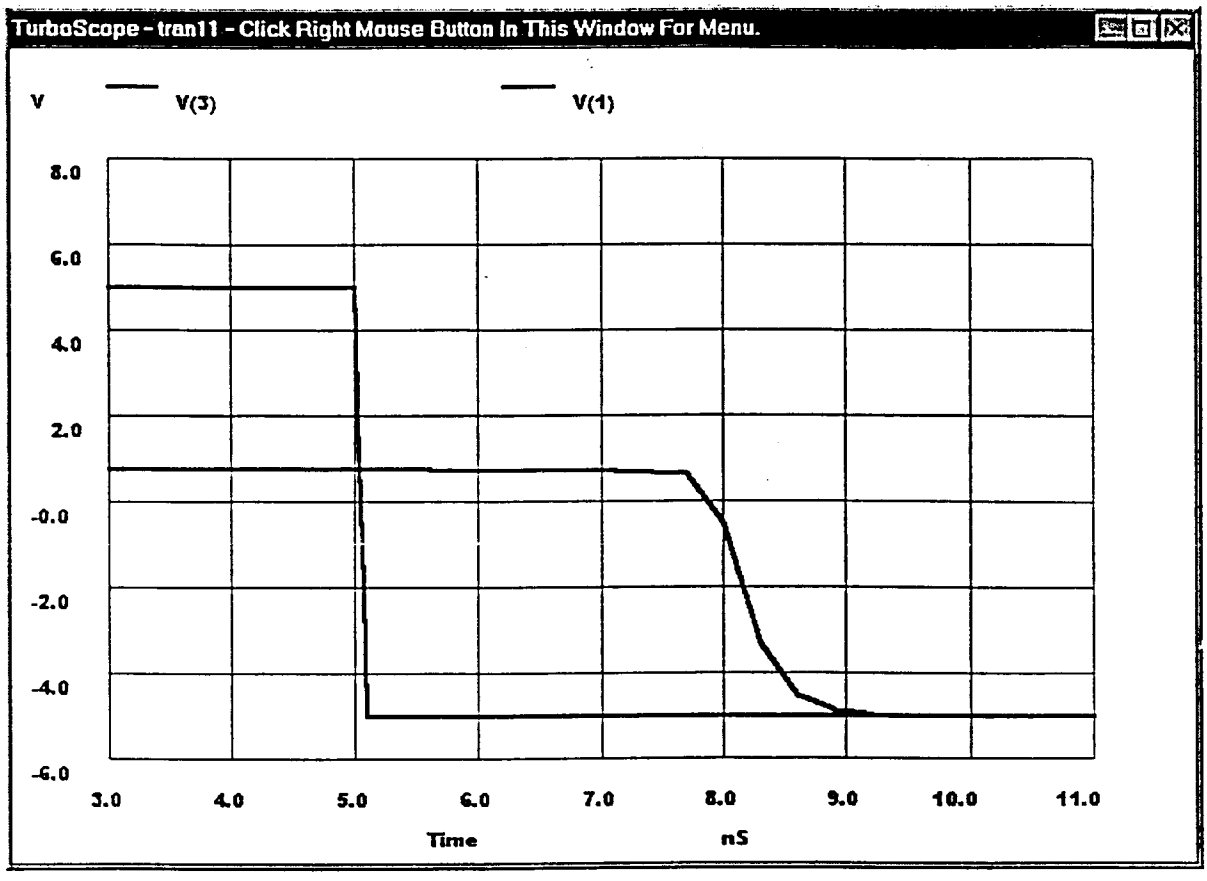


Figure P2.14 SPICE simulation results for problem 2.14

From above simulation results, we can find the storage time is about 2.8ns.

*** Netlist for problem 2.14

```
*** Top Level Netlist ***
D1      1 0 DNwell
R1      3 1 1k
Vin     3 0     DC 0 AC 5v 0 PULSE(5 -5 5ns 0.1ns 0.1ns 10ns 20ns)

***** Spice models and macro models *****

.Model DNwell D
+ IS=1.0E-15 TT=5n CJO=0.5p VJ=.7 M=.333

***** End of spice models and macro models *****

.tran .5ns 15ns 0
```