UNIVERSITY OF CALIFORNIA AT BERKELEY
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1. Consider the structure shown in Figure 1. This two-transistor structure can be considered a new type of single device (the "Cal-sistor") with the drain, source, and gate nodes as given. For this problem, assume that $\lambda=\gamma=0$.

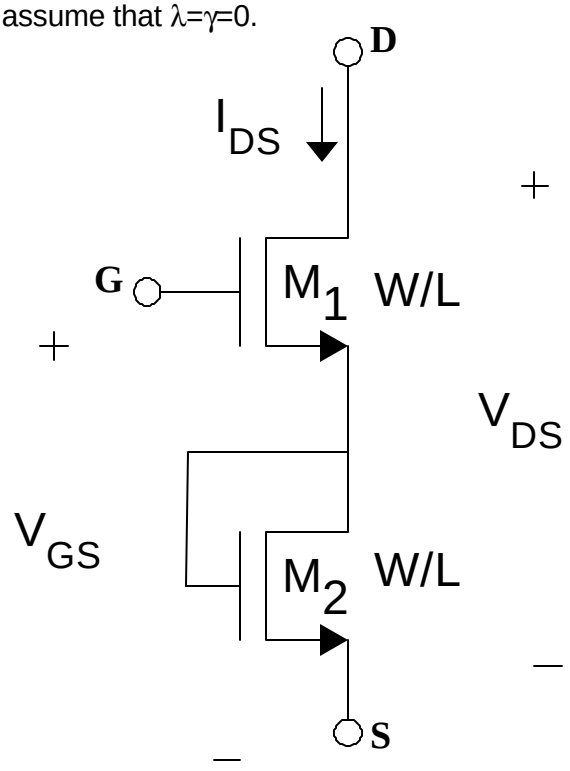

Figure 1

a) Determine the V_{DS} and V_{GS} conditions for each of the 3 operating modes (cutoff, saturation, and linear) for the Cal-sistor.

b) Determine I_{DS} as a function of V_{GS} and V_{DS} for each of these 3 modes.

2. For each of the two circuits in figure 2, perform the calculations for (a) and (b) by hand. Assume V_{T0}=0.5V, k'W/L = 8mA/V^2, λ=0.1V^{-1}, γ=0.2V$^{1/2}$, R_1=10kohm, R_2=2kohm, R_3=10kohm, R_4=10kohm, V_{DD}=3V.

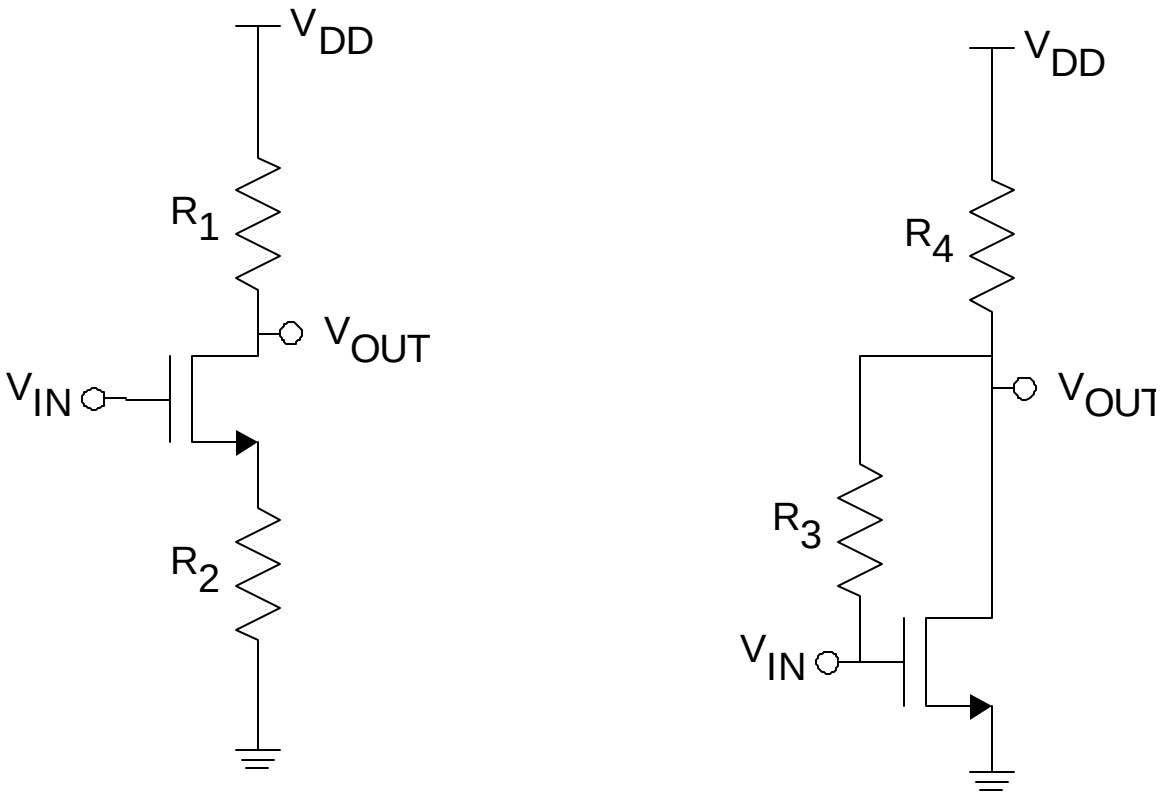

Figure 2

a) Determine the dc voltage V_{IN} so that V_{OUT} is at 1.5V. Assume that V_{IN} is between 0 and VDD.
b) Calculate the operating point parameters I_{DS}, V_T and V_{DSAT}, and the small signal-paramters g_m, g_{mbs}, and r_o.

3. Razavi, problem 2.5, parts a-d. Some notes on the problems are below
    a. Table 2-1 w/ the required device parameters is on p. 37
    b. Be sure to numerically label the voltages breakpoints at which the transistor changes modes (i.e. from linear to saturation and so forth).
    c. Remember that the notation for a drain vs. source node is only notation! For an NMOS device, the drain is determined by which of these two nodes has a higher voltage. Therefore, as voltages are swept, the drain and source nodes can become interchanged!