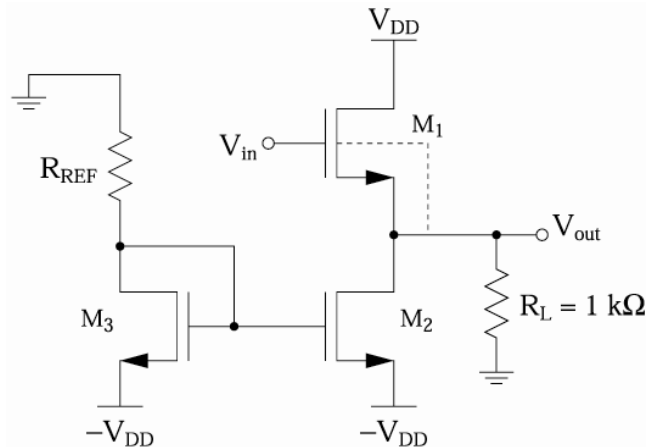


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**Homework #4  
(Due 10/13/04)**

**EECS140  
Fall 2004**



1) For the circuit above, assume all wells are tied to their respective sources.  $V_{DD}=1.8$  V,  $L_{min}=0.18$   $\mu\text{m}$ .  $V_{in}$  is referenced to ground.

a) Choose  $R_{REF}$  and the  $W/L$ s so that the output ranges from  $-1.0$  to  $1.0$  volts with the highest efficiency and smallest area. All devices should be in saturation over the range of operation. You may choose your own value for the DC level at the input.

b) Plot  $V_{out}$  vs.  $V_{in}$  for  $-1.8 < V_{in} < 1.8$  V to demonstrate the output range.

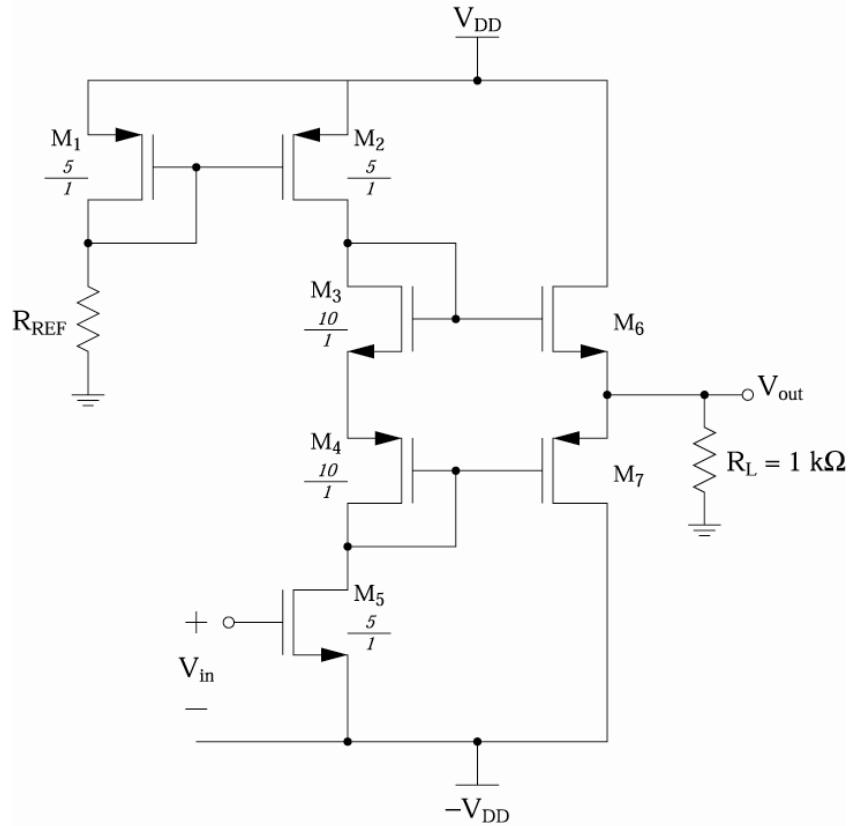
c) Calculate the sine wave efficiency (power into load/total power) for a sine wave output with an amplitude of 1 V.

d) Check the efficiency\* with SPICE.

Use the following NMOS and PMOS transistor models for all parts of the homework.

```
.model nch nmos LEVEL=1 TOX=2.5n VTO=0.5 KP=140.0e-6 LAMBDA=0.1
+GAMMA=0.5 PHI=0.6
```

```
.model pch pmos LEVEL=1 TOX=2.5n VTO=-0.5 KP=65.0e-6 LAMBDA=0.15
+GAMMA=0.5 PHI=0.6
```



2) For the circuit above, assume all wells are tied to their respective sources.  $V_{DD}=1.8$  V. Use the same device models as in P#1.  $L_{min}=0.18$   $\mu\text{m}$ .  $V_{in}$  is referenced to the negative supply rail.

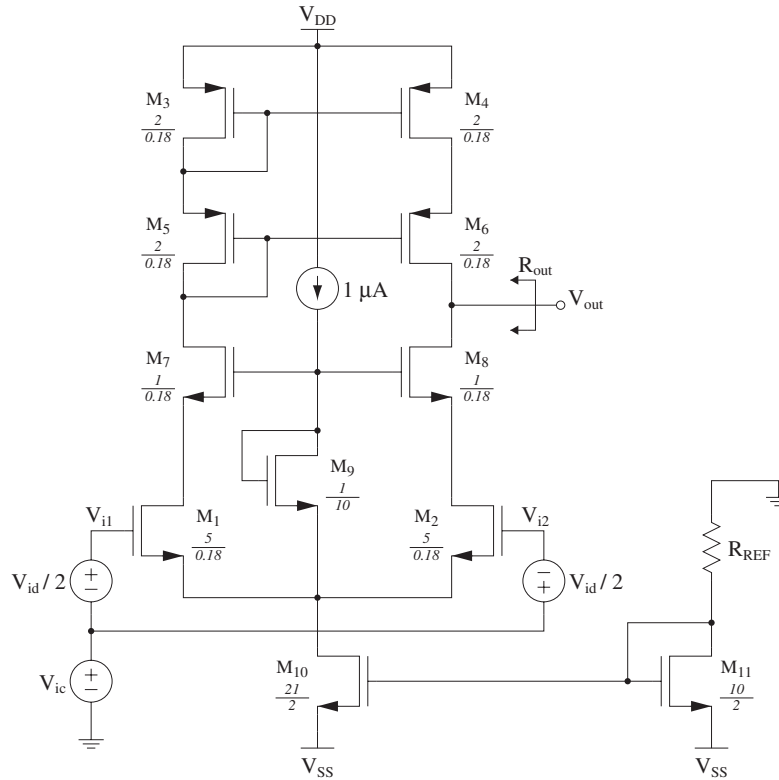
a) Choose  $R_{REF}$  such that the bias current through  $M_2$ - $M_5$  is  $1$   $\mu\text{A}$ .

b) Choose the  $W/L$ s of  $M_6$  and  $M_7$  so that the output ranges from  $-1.0$  to  $1.0$  volts with the highest efficiency and smallest area. All devices should be in saturation over the range of operation. You may choose your own value for the DC level at the input.

c) Plot  $V_{out}$  vs.  $V_{in}$  only in the high gain region to demonstrate the output range.

d) Calculate the sine wave efficiency (power into load/total power) for a sine wave output with an amplitude of  $1$  V.

e) Check the efficiency\* with SPICE.



3) Do the following for the circuit above. Assume that the wells of all NMOS transistors are tied to the sources of those devices, while all PMOS transistors have their bulk terminals tied to  $V_{DD}$ . Assume dual supplies of  $V_{DD}=1.8$  V and  $V_{SS}=-1.8$  V. Use the same device models as in P#1.

a) Choose  $R_{REF}$  so that the  $I_{DS}$  of M1-M8 is  $10 \mu\text{A}$  when  $V_{IC}=0$  V.

b) Use SPICE to plot  $V_{out}$  vs.  $V_{id}$ , with  $V_{IC}=0$  over the range  $-10 \text{ mV} < V_{id} < 10 \text{ mV}$ .

Explain what causes the breakpoints in the graph and calculate the values of  $V_{out}$  at the breakpoints by hand. (Hint: there are four breakpoints.)

c) Use SPICE to plot  $V_{out}$  vs.  $V_{ic}$ , with  $V_{ID}=0$  over the range  $-1.8 < V_{ic} < 1.8$  V.

Explain what causes the breakpoints in the graph and calculate the values of  $V_{ic}$  at the breakpoints by hand. (Hint: there are three breakpoints.)

d) Calculate  $A_{dm}=v_{out}/v_{in}$  with  $V_{IC}=V_{ID}=0$ .

e) Calculate  $R_{out}$  with  $V_{IC}=V_{ID}=0$ .

Verify (d) and (e) with SPICE using the .TF analysis option and explain any differences greater than 10%.

\* Hint: How to verify the efficiency with HSPICE?

i) Make your input voltage source a sine wave source:

```
vin in1 in2 sin(<dc-voltage> <amplitude> <freq>)
```

ii) Do a transient analysis (time domain analysis) for one period of the sine wave (ex. f=1kHz) and measure the power into the load and the total supply power:

```
.meas tran p_load avg p(rload)
.meas tran p_supply_p avg p(vddp)
.meas tran p_supply_n avg p(vddn)
.meas tran p_supply param='-p_supply_p-p_supply_n'
.meas tran p_eff param='100*p_load/p_supply'
.tran 1u 1m
```

where 'rload' is the load resistance, 'vddp' is the positive supply and 'vddn' is the negative supply. The measured values will be listed in your output file. 'p\_eff' is the efficiency.