CMOS Operational Amplifier (1)

Lesson 1

pp. 1-50

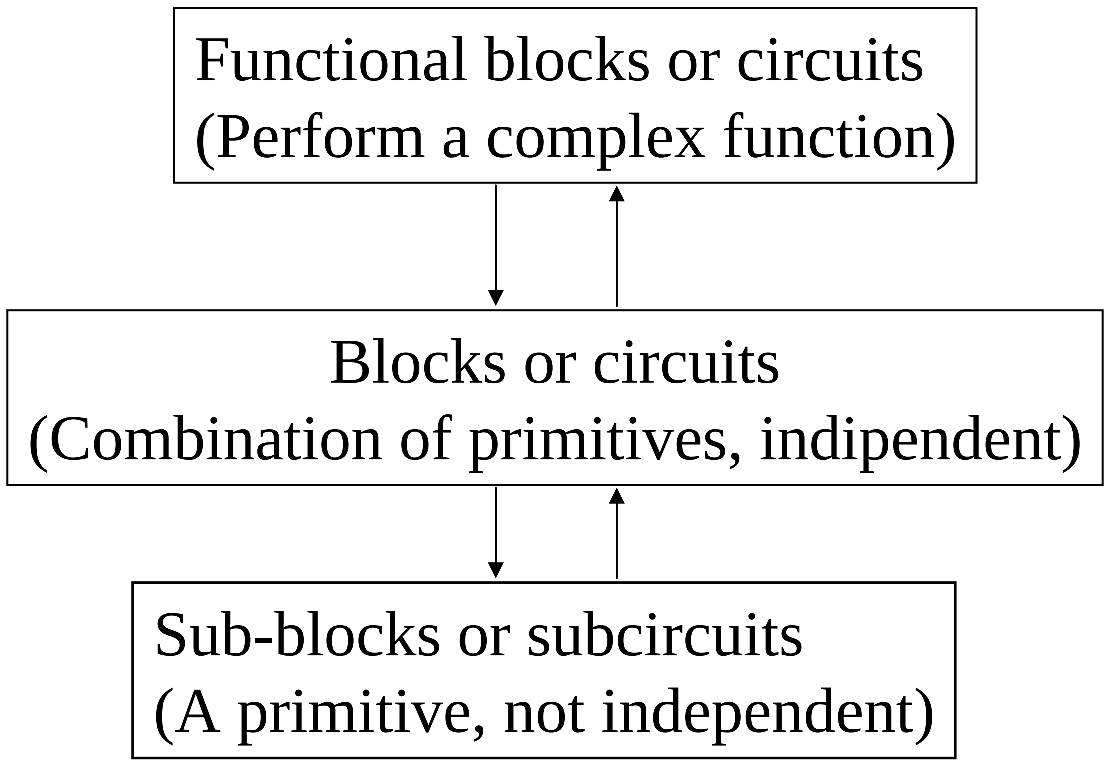
Outline

- Design of CMOS Op Amps
- Compensation of Op Amps
- Two-Stage Operational Amlifier Design
- Power Supply rejection Ratio of the Two-Stage Op Amp
- Cascode Op Amps
- Simulation and Measurement of Op Amps
- Macromodels for Op Amp

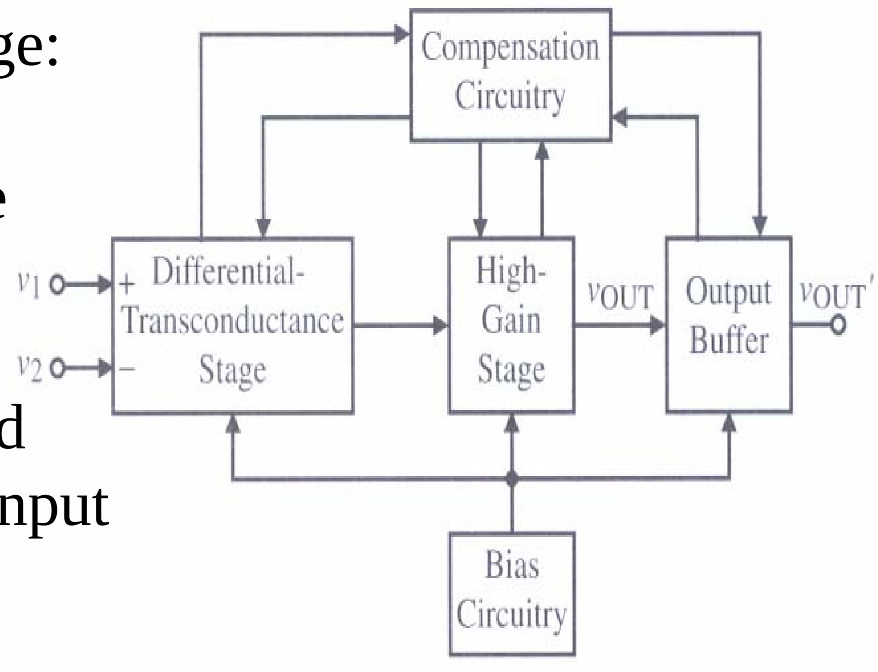
Goal

Understand the analysis, design and measurement of simple CMOS op amps

Design Hierarchy



Design of CMOS Operational Amplifiers: High level viewpoint of an Op Amp



- Differential transconductance stage:
  Forms the input and sometimes provides the differential-to-single ended conversion
- High gain stage:
  Provides the voltage gain required by the op amp together with the input stage
- Output buffer:
  Used if the op amp must drive a low resistance
- Compensation:
  Necessary to keep the op amp stable when resistive negative feedback is applied

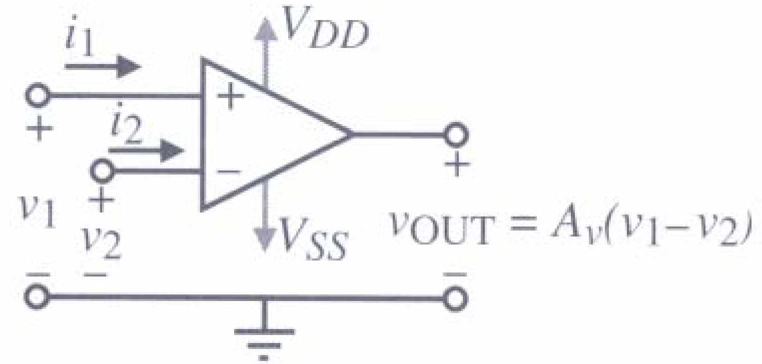
Ideal Op Amp

Null port:
If the differential gain of the op amp is large enough then input terminal pair becomes a null port.
A null port is a pair of terminals where the voltage is zero and the current is zero.
I.e.,

$$v_1 - v_2 = v_i = 0$$

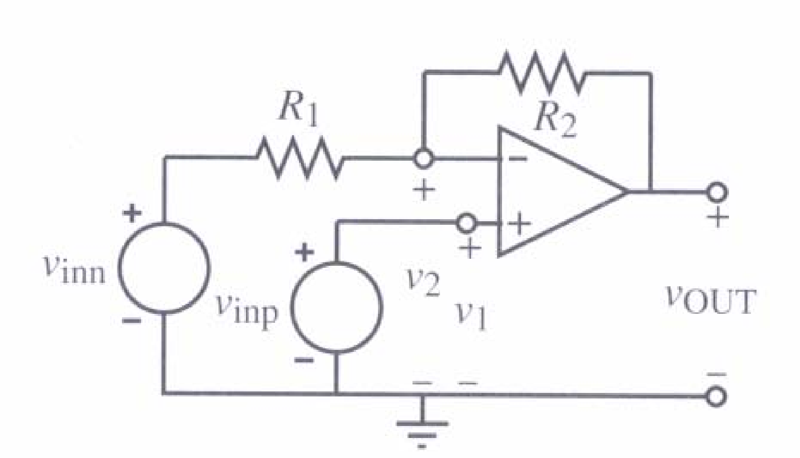
And

$$i_1 = 0 \text{ and } i_2 = 0$$



Therefore, ideal op amps can be analyzed by assuming the differential input voltage is zero and that no current flows into or out of the differential inputs

General Configuration of the Op Amp as a Voltage Amplifier



Non inverting voltage amplifier:

$v_{inn}=0$ →

$$v_{out} = \left(\frac{R_1 + R_2}{R_1}\right) v_{inp}$$

Inverting voltage amplifier:

$v_{inp}=0$ →

$$v_{out} = -\left(\frac{R_2}{R_1}\right) v_{inn}$$

Example- Simplified Analysis of an Op Amp Circuit

The circuit shown below is an inverting voltage amplifier using an op amp.
Find the voltage transfer function, v_{out}/v_{in}.

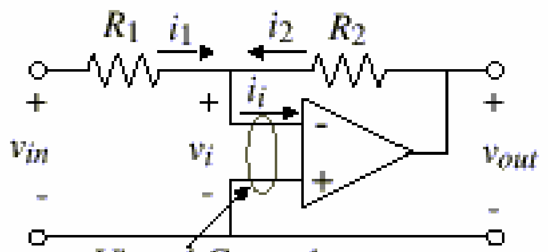


Fig. 110-04

Solution

If Av→∞, then vi→0 because of the negative feedback path through R2. (The op amp with –fb makes its input terminal voltages equal)

$$v_i=0 \text{ and } i_i=0$$

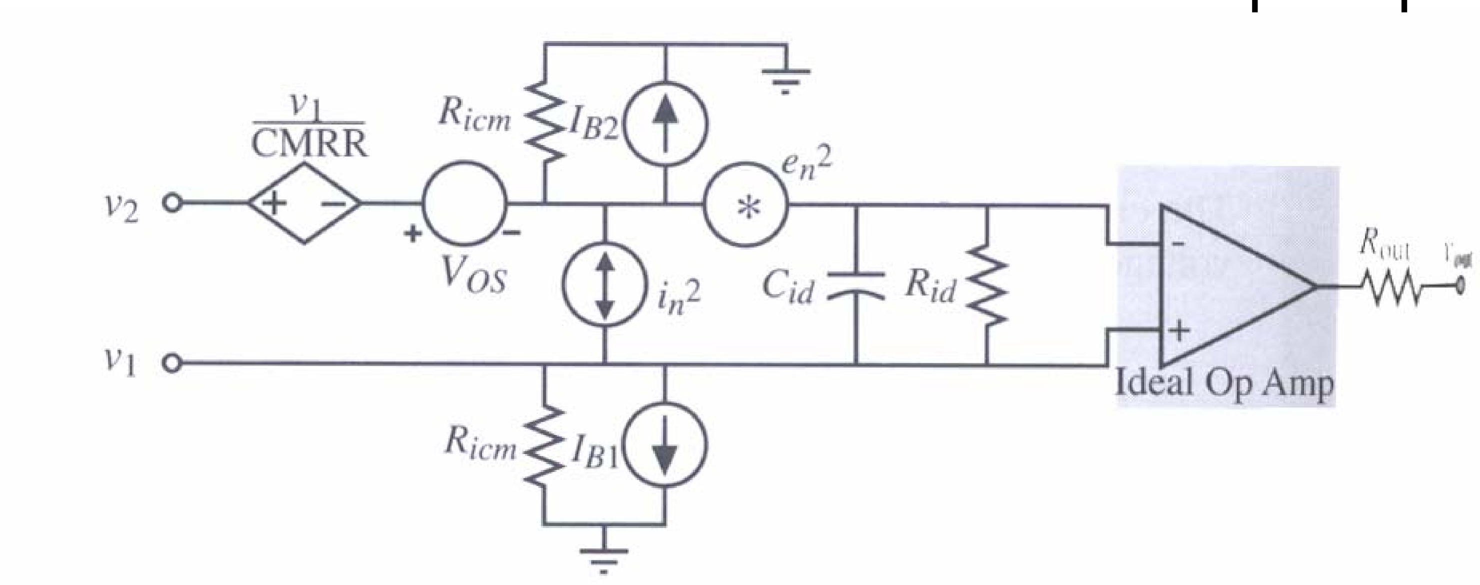
Note that the null port becomes the familiar virtual ground if one of the op amp input terminals is on ground. If this is the case, then we can write that

$$i_1 = \frac{v_{in}}{R_1} \quad \text{and} \quad i_2 = \frac{v_{out}}{R_2}$$

Since, $i_1=0$ then $i_1+i_2=0$ giving the desired result as

$$\frac{v_{out}}{v_{in}} = -\frac{R_2}{R_1}$$

Linear and Static Characterization of the Op Amp



- R_{id}, C_{id}=finite differential input impedance
- R_{out}= output resistance
- R_{icm}=common-mode input resistance
- V_{os}=input-offset
- I_{os}(not shown)= input-offset=I_{B1}-I_{B2}
- e^2_n, i^2_n rms voltage- and current-noise source, spectral density (mean-square volts/Hertz)
- v_1/CMRR= CMRR model

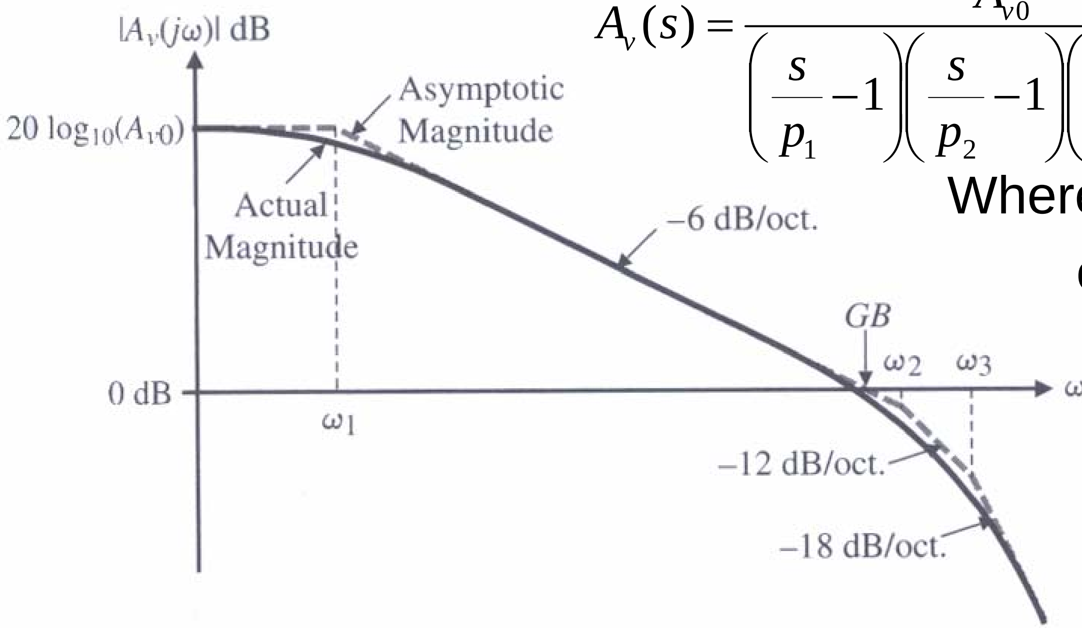
Linear and Dynamic Characteristics of the Op Amp

Differential and Common-mode frequency response is:

$$V_{out}(s) = A_v(s)\left[V_1(s) - V_2(s)\right] \pm A_c(s)\left(\frac{V_1(s) + V_2(s)}{2}\right)$$

Differential-frequency response:

$$A_v(s) = \frac{A_{v0}}{\left(\frac{s}{p_1} - 1\right)\left(\frac{s}{p_2} - 1\right)\left(\frac{s}{p_3} - 1\right)\ldots} = \frac{A_{v0}\, p_1 p_2 p_3}{(s - p_1)(s - p_2)(s - p_3)\ldots}$$



Where p_1, p_2, … are poles of the op-amp open-loop differential-frequency response (i.e.: transfer function) (ignoring zeros).

Other Characteristics of the Op Amp

Power Supply Rejection Ratio (PSRR):

$$PSRR = \frac{\Delta V_{DD}}{\Delta V_{OUT}} A_V(s) = \frac{V_O / V_{in}(V_{dd} = 0)}{V_O / V_{dd}(V_{in} = 0)}$$

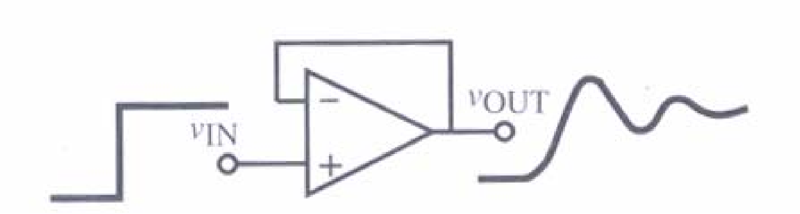
Input common mode range (ICMR):

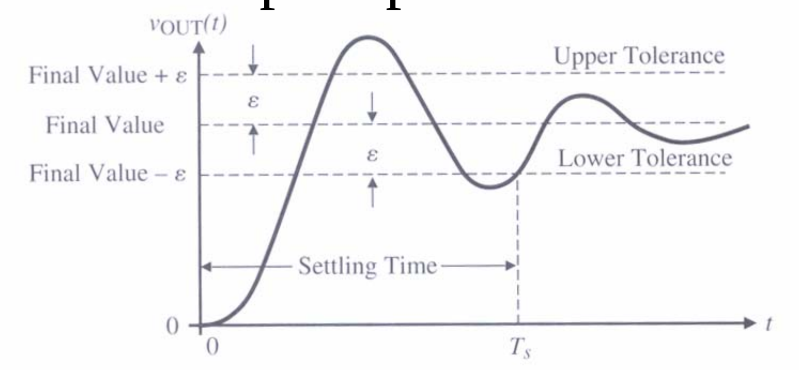
ICMR=the voltage range over which the input common-mode signal can vary without influence the differential performance

Slew rate (SR):

SR= output voltage rate limit of the op amp

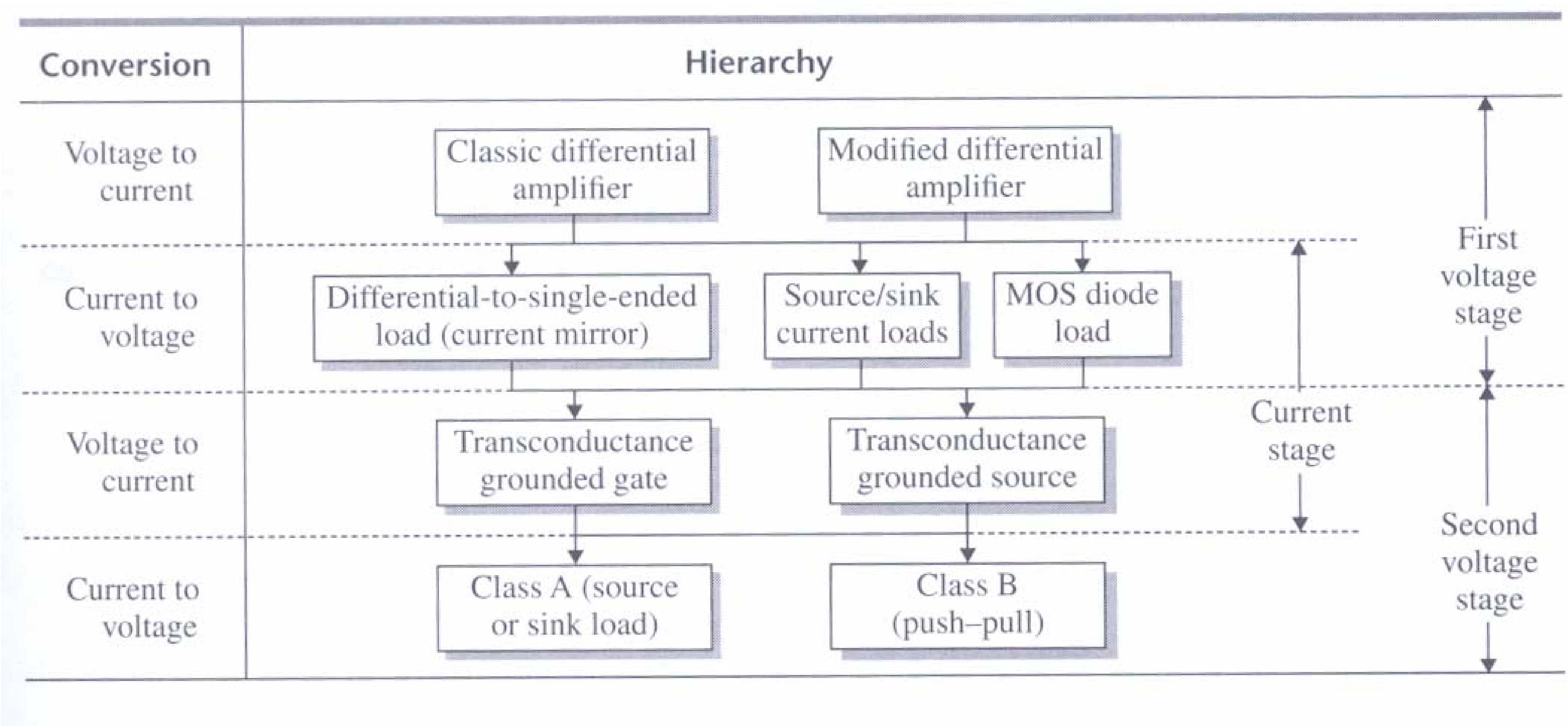
Settling time (T_S):





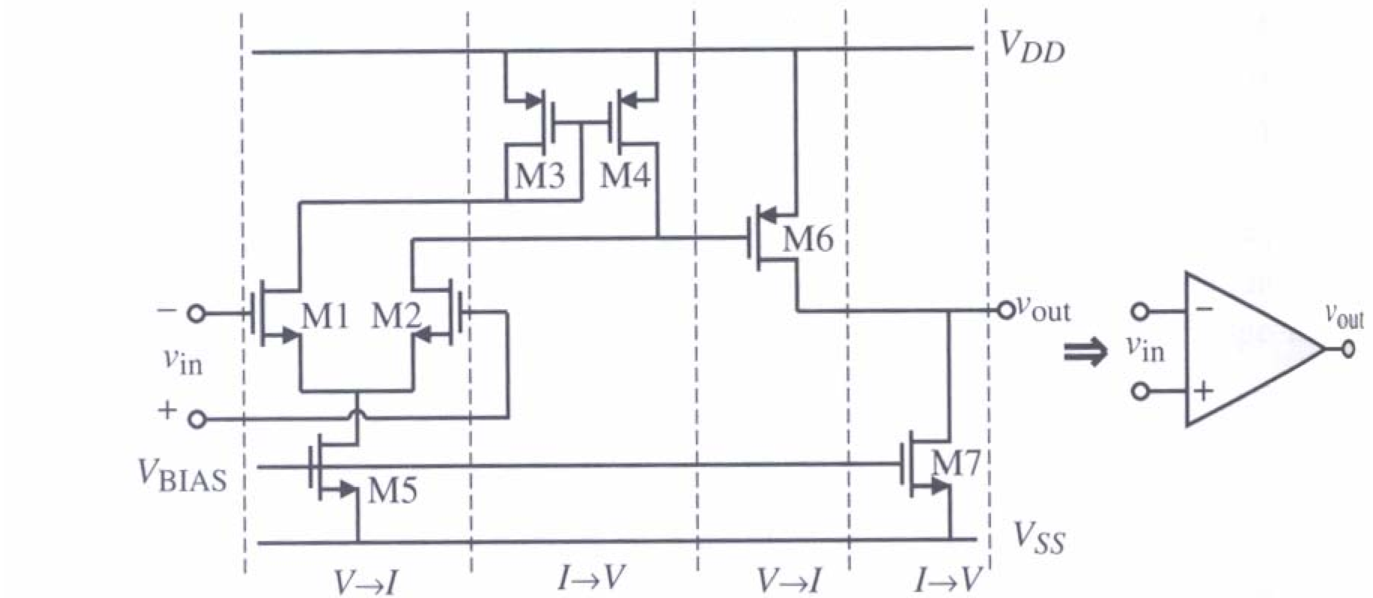
Classification of CMOS Op Amps

Categorization of CMOS Op Amps:



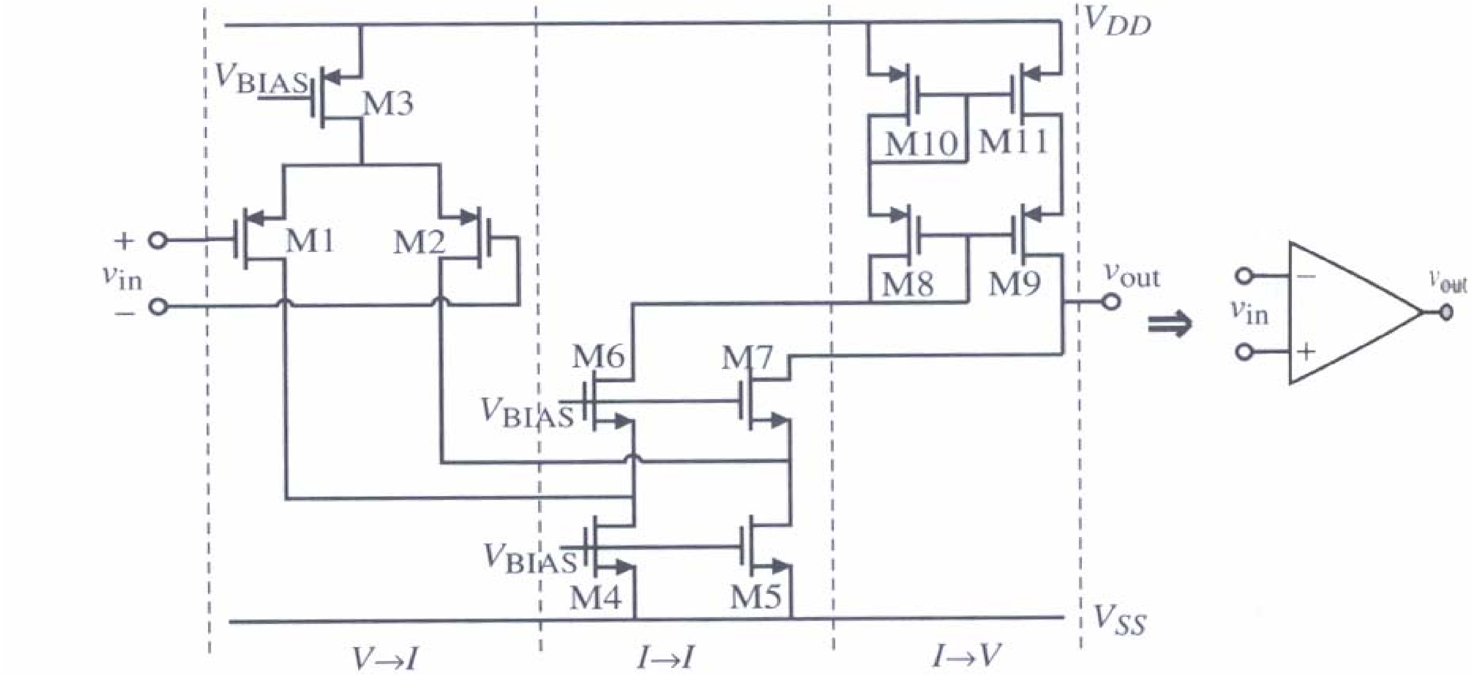
Classical two stage CMOS Op Amp

- The first stage consists of a differential amplifier converting the differential input voltage to differential currents. This differential currents are applied to a current mirror load recovering the differential voltage.
- The second stage is a common source converting the second stage input voltage to current. This transistor is loaded by a current-sink load, which converts the current to voltage at the output.



Folded-Cascode CMOS Op Amp

- This architecture was developed in part to improve the input common-mode range and the PSRR.
- One of the advantage is that it has a push-pull output: the op amp can actively sink or source current from the load. (the output stage of the previous two-stage op amp is Class A, which means that either its sinking or sourcing capability is fixed.)



Design of CMOS Op Amps
Steps:

1. Choosing or creating the basic structure of the op amp.

   This step results in a schematic showing the transistors and their interconnections. The diagram does not change throughout the remainder of the design unless the specifications cannot be met, then a new or modified structure must be developed.
2. Selecting dc currents and transistors size.

   Most of the effort of design is in this category.

   Simulators are used to aid the designer in this phase. The general performance of the circuit should be known a priori.
3. Physical implementation of the design

   Layout of the transistors

   Floorplanning the connections, pin-outs power supply buses and grounds

   Extraction of the physical parasitics and resimulation

   Verification that the layout is a physical representation of the circuit.
4. Fabrication
5. Measurement (prototyping test)

   Verification of the specifications

   Modification of the design as necessary

Boundary conditions and requirements

- **Boundary conditions:**

1. Process specification (VT, K’, Cox, etc.)
2. Supply voltage and range
3. Supply current and range
4. Operating temperature and range

- **Requirements**

1. Gain
2. Gain Bandwidth
3. Settling time
4. Slew rate
5. Input common-mode range, ICMR
6. Common-mode rejection ratio CMRR
7. Power-supply rejection ratio, PSRR
8. Output-voltage swing
9. Output resistance
10. Offset
11. Noise
12. Layout area

Specifications for a Typical Unbuffered CMOS Op Amp

Boundary Conditions	Requirement
Process Specification	
Supply Voltage	±2.5 V ±10%
Supply Current	100 μA
Temperature Range	0 to 70°C

Specifications	Value
Gain	≥ 70 dB
Gainbandwidth	≥ 5 MHz
Settling Time	≤ 1 μsec
Slew Rate	≥ 5 V/μsec
Input *CMR*	≥ ±1.5 V
CMRR	≥ 60 dB
PSRR	≥ 60 dB
Output Swing	≥ ±1.5 V
Output Resistance	N/A, capacitive load only
Offset	≤ ±10 mV
Noise	≤ 100nV/$\sqrt{\text{Hz}}$ at 1KHz
Layout Area	≤ 10,000 min. channel length^2

Some Practical Thoughts on Op Amp Design

1. Decide upon a suitable topology
   - Experience is a great help
   - Topology should be the one capable of meeting most of the specifications
   - Try to avoid "inventing" a new topology but start with an existing topology
2. Determine the type of compensation needed to meet the specifications
   - Consider the load and stability requirements
   - Use some form of Miller compensation or a self-compensated approach (shown later)
3. Design dc currents and device size for proper dc, ac, and transient performance
   - This begins with hand calculations based upon approximate design equations
   - Compensation components are also sized in this step of the procedure
   - After each device is sized by hand, a circuit simulator is used to fine tune the design

Two basic steps of design:

1. "First –cut" – this step is to use hand calculations to propose a design that has potential of satisfying the specifications. Design robustness is developed in this step
2. Optimization – this step uses the computer to refine and optimize the design

Compensation of op amps

Objective

Objective of compensation is to achieve stable operation when negative feedback is applied around the op amp.

Types of Compensation

1. Miller – Use of a capacitor feeding back around a high-gain, inverting stage.

   - Miller capacitor only

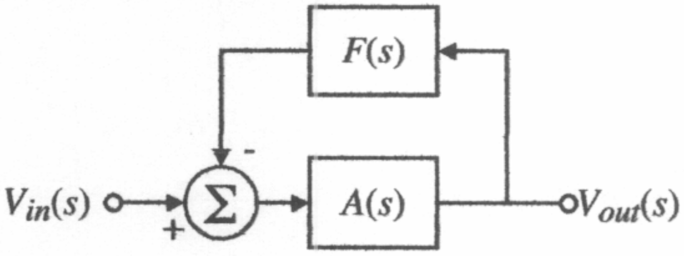
   - Miller capacitor with an unity-gain buffer to block the forward path through the compensation capacitor. Can eliminate the RHP zero.

   - Miller with a nulling resistor. Similar to Miller but with an added series resistance to gain control over the RHP zero

2. Self compensation – Load capacitor compensates the op amp

3. Feedforward – Bypassing a positive gain amplifier resulting in phase lead. Gain can be less than unity.

Single-loop, Negative Feedback System



Block diagram:

$A(s)$ = differential-mode voltage gain of the op amp

$F(s)$ = feedback transfer function from the output of op amp back to the input.

Definitions:

- Open-loop gain $= L(s) = -A(s)F(s)$
- Closed-loop gain $= \dfrac{V_{out}(s)}{V_{in}(s)} = \dfrac{A(s)}{1+A(s)F(s)}$

Stability Requirements:

The requirements for stability for a single-loop, negative feedback system is,

$$|A(j\omega_{0°})F(j\omega_{0°})| = |L(j\omega_{0°})| < 1$$

where $\omega_{0°}$ is defined as

$$\text{Arg}[-A(j\omega_{0°})F(j\omega_{0°})] = \text{Arg}[L(j\omega_{0°})] = 0°$$

Another convenient way to express this requirement is

$$\text{Arg}[-A(j\omega_{0dB})F(j\omega_{0dB})] = \text{Arg}[L(j\omega_{0dB})] > 0°$$

where ω_{0dB} is defined as

$$|A(j\omega_{0dB})F(j\omega_{0dB})| = |L(j\omega_{0dB})| = 1$$

Stability Requirement using Bode Plots

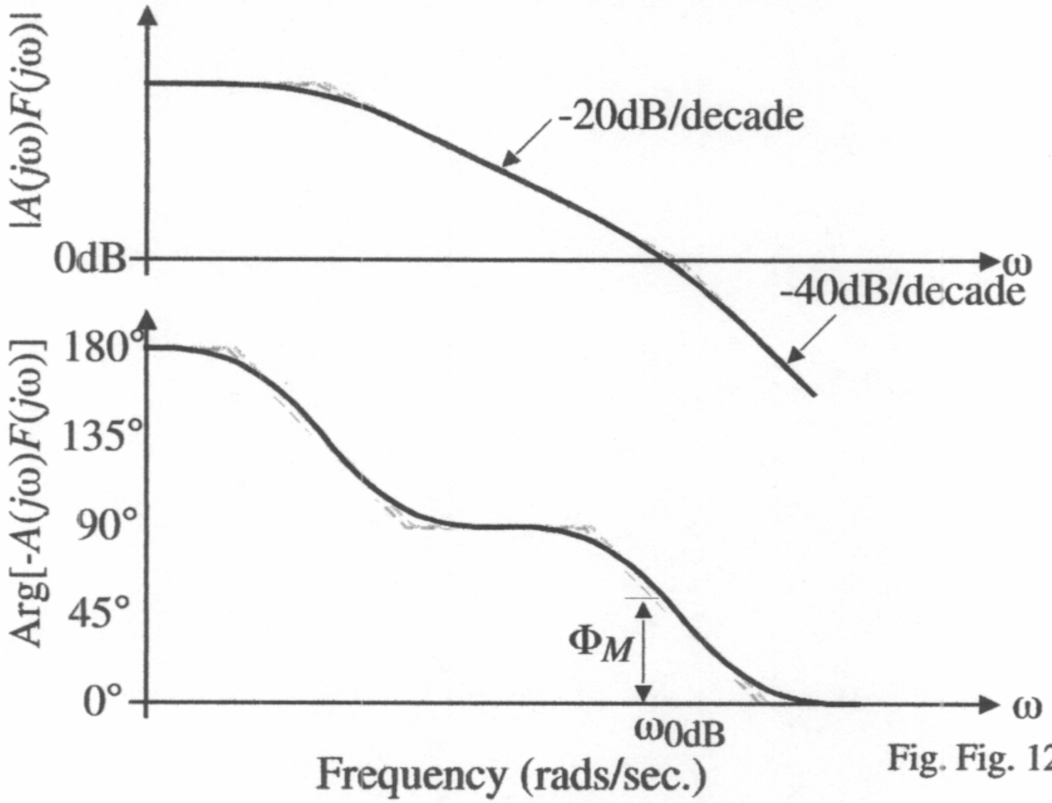


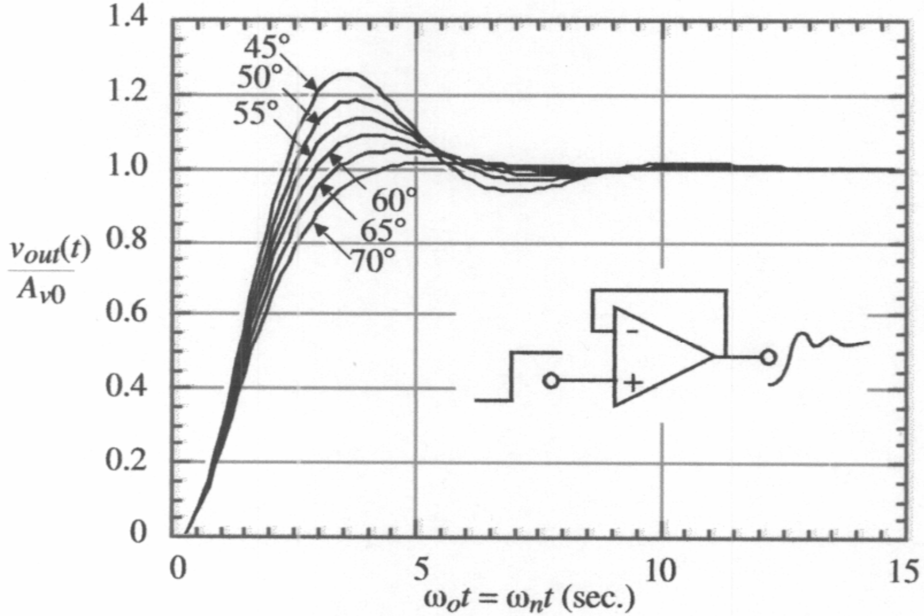
Fig. Fig. 120-02

A measure of stability is given by the phase when $|A(j\omega)F(j\omega)| = 1$. This phase is called *phase margin*.

$$\text{Phase margin} = \Phi_M = \text{Arg}[-A(j\omega_{0dB})F(j\omega_{0dB})] = \text{Arg}[L(j\omega_{0dB})]$$

Why do we want good Stability?

Consider the step response of second-order system which closely models the closed-loop gain of the op amp.



A "good" step response is one that quickly reaches its final value.

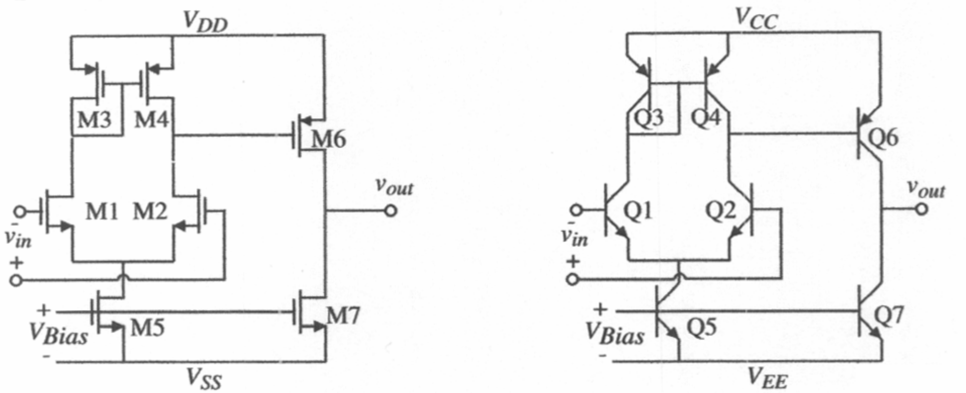
Therefore, we see that phase margin should be at least 45° and preferably 60° or larger.

(A rule of thumb for satisfactory stability is that there should be less than three rings.)

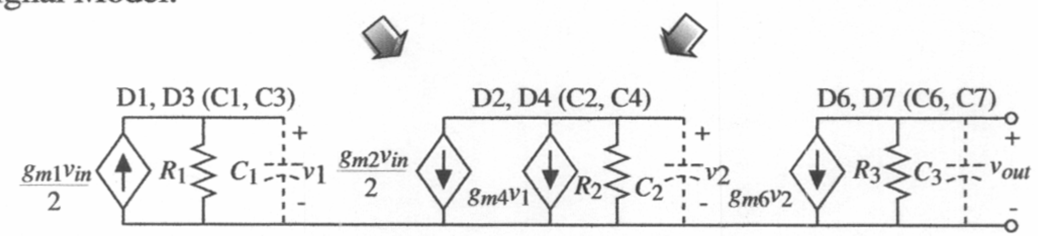
Note that good stability is not necessarily the quickest risetime.

Uncompensated Frequency Response of two-stage op amps (1)

Two-Stage Op Amps:



Small-Signal Model:



Note that this model neglects the base-collector and gate-drain capacitances for purposes of simplification.

Uncompensated Frequency Response of two-stage op amps (2)

For the MOS two-stage op amp:

$$R_1 \approx \frac{1}{g_{m3}} \| r_{ds3} \| r_{ds1} \approx \frac{1}{g_{m3}} \qquad R_2 = r_{ds2} \| r_{ds4} \qquad \text{and} \qquad R_3 = r_{ds6} \| r_{ds7}$$

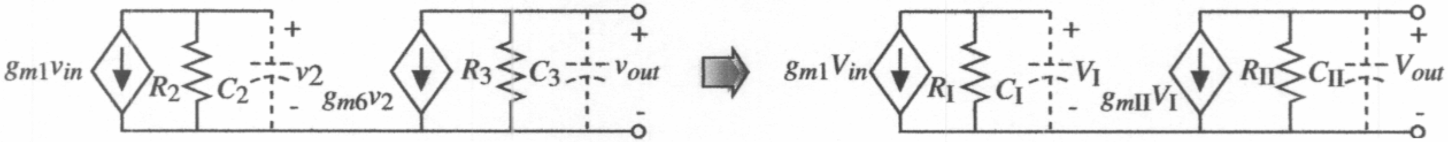
$$C_1 = C_{gs3} + C_{gs4} + C_{bd1} + C_{bd3} \qquad C_2 = C_{gs6} + C_{bd2} + C_{bd4} \qquad \text{and } C_3 = C_L + C_{bd6} + C_{bd7}$$

For the BJT two-stage op amp:

$$R_1 = \frac{1}{g_{m3}} \| r_{\pi 3} \| r_{\pi 4} \| r_{o1} \| r_{o3} \approx \frac{1}{g_{m3}} \quad R_2 = r_{\pi 6} \| r_{o2} \| r_{o4} \approx r_{\pi 6} \quad \text{and} \quad R_3 = r_{o6} \| r_{o7}$$

$$C_1 = C_{\pi 3} + C_{\pi 4} + C_{cs1} + C_{cs3} \qquad C_2 = C_{\pi 6} + C_{cs2} + C_{cs4} \qquad \text{and} \quad C_3 = C_L + C_{cs6} + C_{cs7}$$

Assuming the pole due to C_1 is much greater than the poles due to C_2 and C_3 gives,

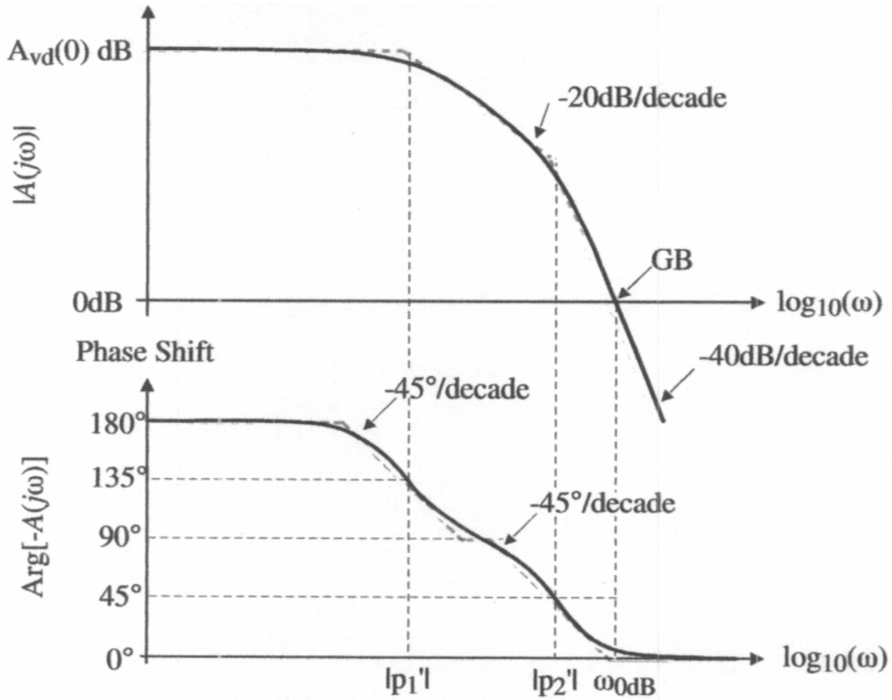


The locations for the two poles are given by the following equations

$$p'_1 = \frac{-1}{R_I C_I} \quad \text{and } p'_2 = \frac{-1}{R_{II} C_{II}}$$

where R_I (R_{II}) is the resistance to ground seen from the output of the first (second) stage and C_I (C_{II}) is the capacitance to ground seen from the output of the first (second) stage.

Uncompensated Frequency Response of an op amps

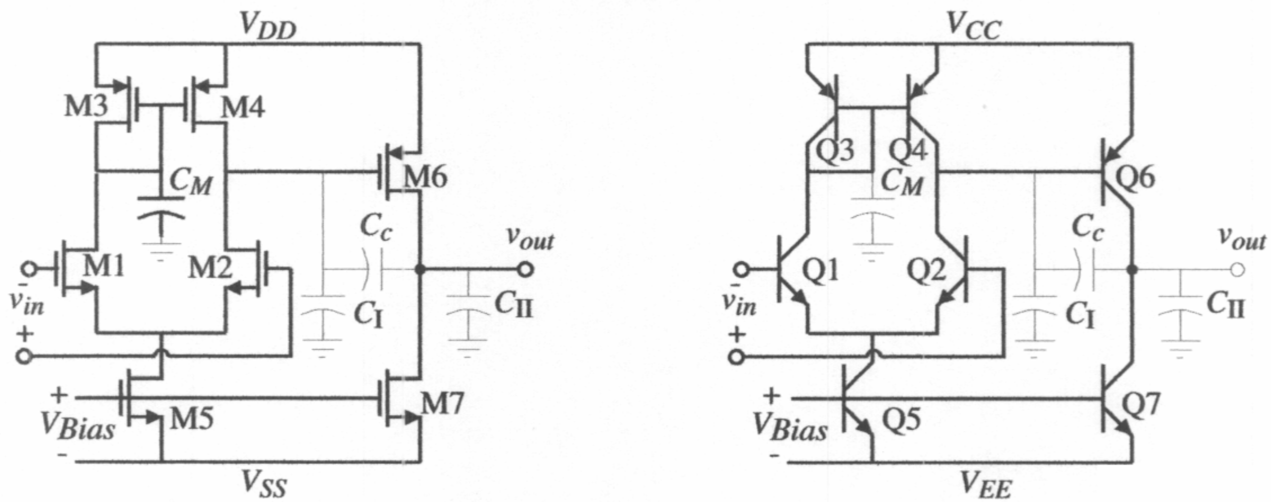


If we assume that $F(s) = 1$ (this is the worst case for stability considerations), then the above plot is the same as the loop gain.

Note that the phase margin is much less than 45°.

Therefore, the op amp must be compensated before using it in a closed-loop configuration.

Miller Compensation of the Two-Stage Op Amp



The various capacitors are:

C_c = accomplishes the Miller compensation

C_M = capacitance associated with the first-stage mirror (mirror pole)

C_I = output capacitance to ground of the first-stage

C_{II} = output capacitance to ground of the second-stage

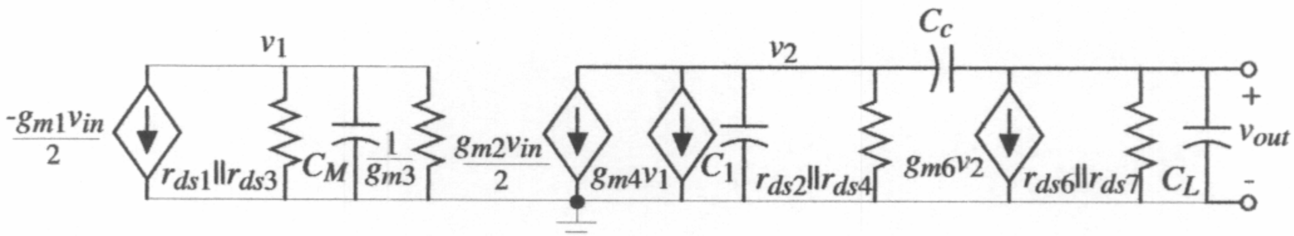
Compensated Two-Stage, Small-Signal Frequency Response Model Simplified

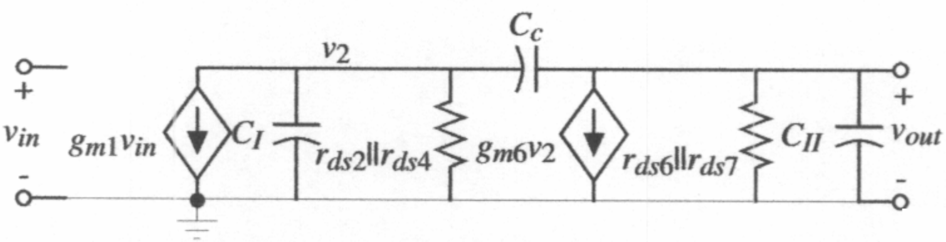
Use the CMOS op amp to illustrate:

1.) Assume that $g_{m3} >> g_{ds3} + g_{ds1}$

2.) Assume that $\frac{g_{m3}}{C_M} >> GB$

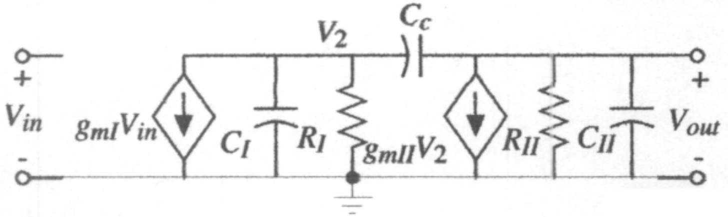
Therefore,





Same circuit holds for the BJT op amp with different component relationships.

General Two-Stage Frequency Response Analysis



where

$$g_{mI} = g_{m1} = g_{m2},\ R_I = r_{ds2} || r_{ds4},\ C_I = C_1$$

and

$$g_{mII} = g_{m6},\ R_{II} = r_{ds6} || r_{ds7},\ C_{II} = C_2 = C_L$$

Nodal Equations:

$$-g_{mI}V_{in} = [G_I + s(C_I + C_c)]V_2 - [sC_c]V_{out} \quad \text{and} \quad 0 = [g_{mII} - sC_c]V_2 + [G_{II} + sC_{II} + sC_c]V_{out}$$

Solving using Cramer's rule gives,

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{g_{mI}(g_{mII} - sC_c)}{G_IG_{II} + s\,[G_{II}(C_I+C_{II}) + G_I(C_{II}+C_c) + g_{mII}C_c] + s^2[C_IC_{II} + C_cC_I + C_cC_{II}]}$$

$$= \frac{A_o[1 - s\,(C_c/g_{mII})]}{1 + s\,[R_I(C_I+C_{II}) + R_{II}(C_2+C_c) + g_{mII}R_IR_{II}C_c] + s^2[R_IR_{II}(C_IC_{II} + C_cC_I + C_cC_{II})]}$$

where, $A_o = g_{mI}g_{mII}R_IR_{II}$

In general, $D(s) = \left(1-\frac{s}{p_1}\right)\left(1-\frac{s}{p_2}\right) = 1 - s\left(\frac{1}{p_1} + \frac{1}{p_2}\right) + \frac{s^2}{p_1p_2} \rightarrow D(s) \approx 1 - \frac{s}{p_1} + \frac{s^2}{p_1p_2}$, if $|p_2| >> |p_1|$

$$\therefore \quad \boxed{p_1 = \frac{-1}{R_I(C_I+C_{II}) + R_{II}(C_{II}+C_c) + g_{mII}R_IR_{II}C_c} \approx \frac{-1}{g_{mII}R_IR_{II}C_c}},\ \boxed{z = \frac{g_{mII}}{C_c}}$$

$$\boxed{p_2 = \frac{-[R_I(C_I+C_{II}) + R_{II}(C_{II}+C_c) + g_{mII}R_IR_{II}C_c]}{R_IR_{II}(C_IC_{II} + C_cC_I + C_cC_{II})} \approx \frac{-g_{mII}C_c}{C_IC_{II} + C_cC_I + C_cC_{II}} \approx \frac{-g_{mII}}{C_{II}}},\ C_{II} > C_c > C_I$$

Summary of Results for Miller Compensation of the Two-Stage Op Amp

There are three roots of importance:

1.) Right-half plane zero:

$$z_1 = \frac{g_{mII}}{C_c} = \frac{g_{m6}}{C_c}$$

This root is very undesirable- it boosts the magnitude while decreasing the phase.

2.) Dominant left-half plane pole (the Miller pole):

$$p_1 \approx \frac{-1}{g_{mII}R_I R_{II} C_c} = \frac{-(g_{ds2}+g_{ds4})(g_{ds6}+g_{ds7})}{g_{m6}C_c}$$

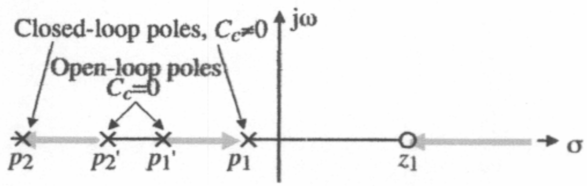
This root accomplishes the desired compensation.

3.) Left-half plane output pole:

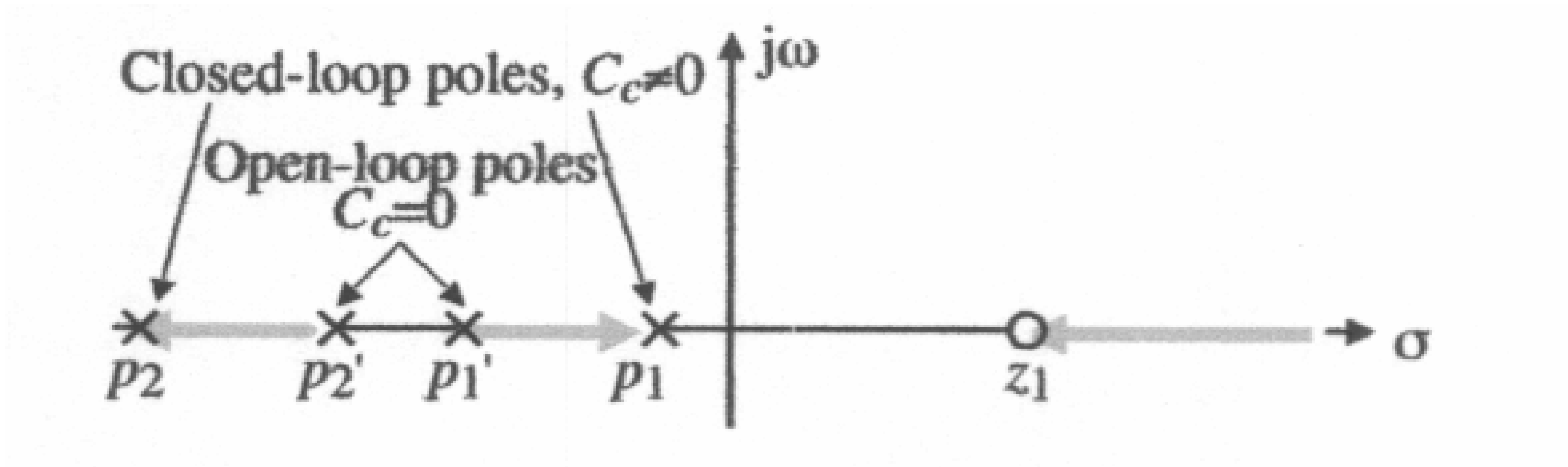
$$p_2 \approx \frac{-g_{mII}}{C_{II}} \approx \frac{-g_{m6}}{C_L}$$

This pole must be ≥ unity-gainbandwidth or the phase margin will not be satisfied.

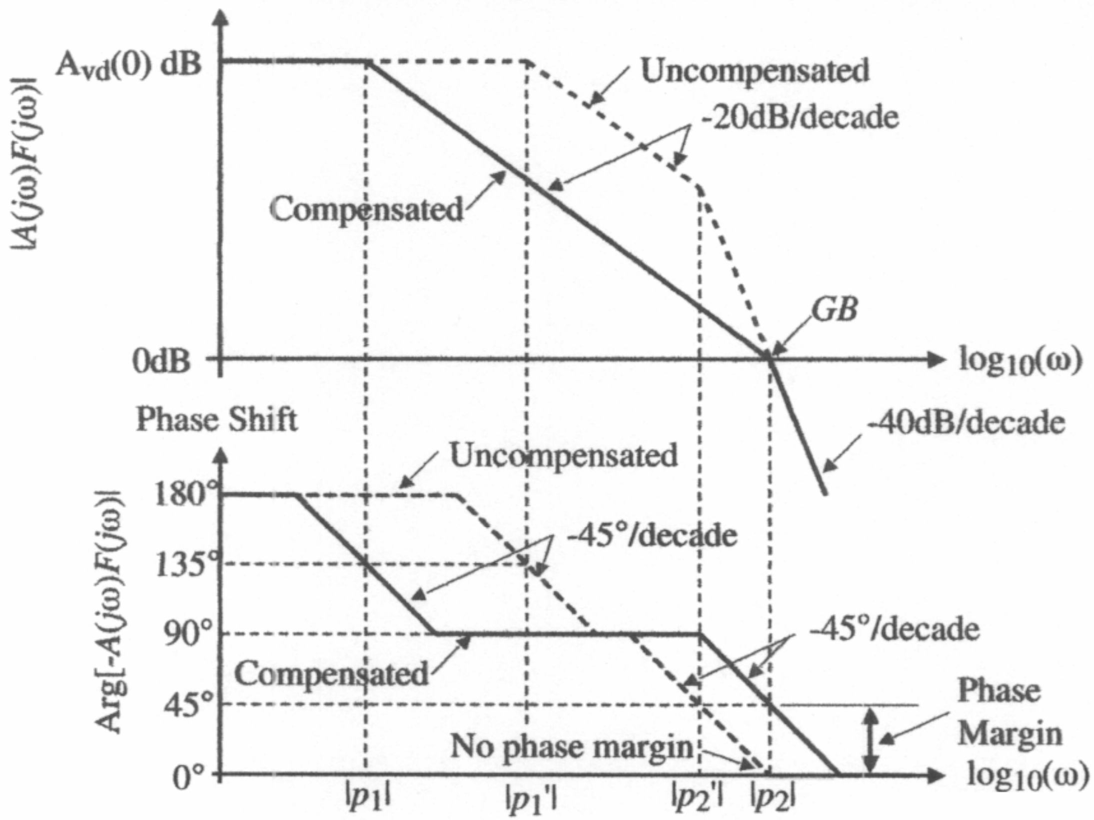
Root locus plot of the Miller compensation:



Miller compensation



Compensated Open-Loop Frequency Response of the two-Stage Op Amp



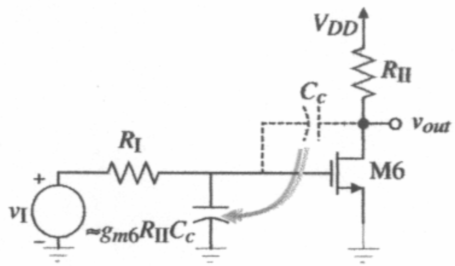
Note that the unity-gainbandwidth, GB, is

$$GB = A_{vd}(0)\cdot|p_1| = (g_{mI}g_{mII}R_IR_{II})\frac{1}{g_{mII}R_IR_{II}C_c} = \frac{g_{mI}}{C_c} = \frac{g_{m1}}{C_c} = \frac{g_{m2}}{C_c}$$

Conceptually, where do these roots come from?

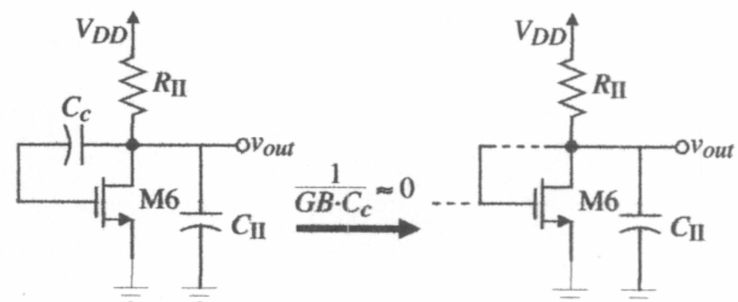
1.) The Miller pole:

$$|p_1| \approx \frac{1}{R_I(g_{m6}R_{II}C_c)}$$



2.) The left-half plane output pole:

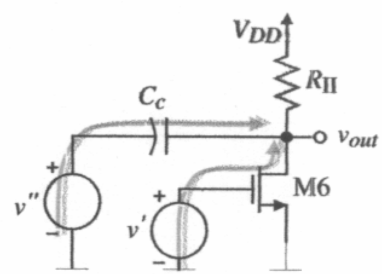
$$|p_2| \approx \frac{g_{m6}}{C_{II}}$$



3.) Right-half plane zero (*One source of zeros is from multiple paths from the input to output*):

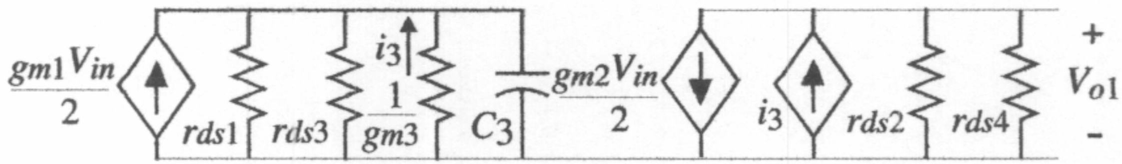
$$v_{out} = \left(\frac{-g_{m6}R_{II}(1/sC_c)}{R_{II} + 1/sC_c}\right) v' + \left(\frac{R_{II}}{R_{II} + 1/sC_c}\right) v'' = \frac{-R_{II}\left(\frac{g_{m6}}{sC_c} - 1\right)}{R_{II} + 1/sC_c}\, v$$

where $v = v' = v''$.



Influence of the Mirror Pole

Up to this point, we have neglected the influence of the pole, p_3, associated with the current mirror of the input stage. A small-signal model for the input stage that includes C_3 is shown below:



The transfer function from the input to the output voltage of the first stage, $V_{o1}(s)$, can be written as

$$\frac{V_{o1}(s)}{V_{in}(s)} = \frac{-g_{m1}}{2(g_{ds2}+g_{ds4})}\left[\frac{g_{m3}+g_{ds1}+g_{ds3}}{g_{m3}+g_{ds1}+g_{ds3}+sC_3}+1\right] \approx \frac{-g_{m1}}{2(g_{ds2}+g_{ds4})}\left[\frac{sC_3+2g_{m3}}{sC_3+g_{m3}}\right]$$

We see that there is a pole and a zero given as

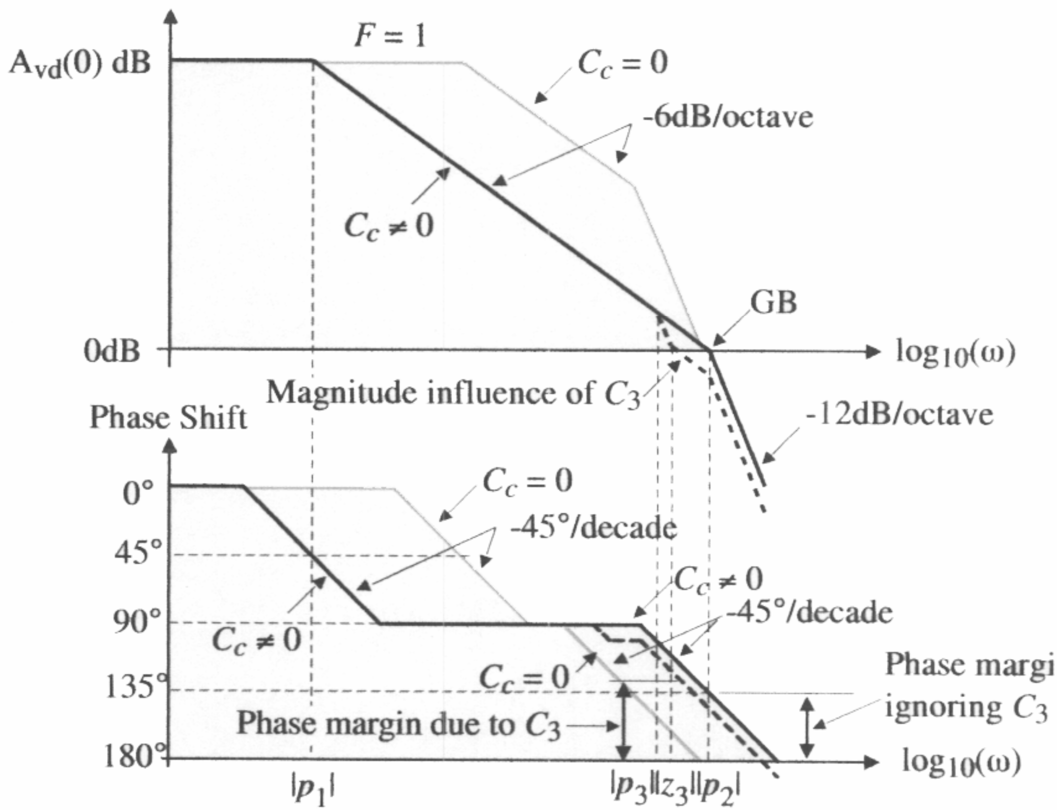
$$p_3 = -\frac{g_{m3}}{C_3} \quad \text{and } z_3 = -\frac{2g_{m3}}{C_3}$$

Influence of the Mirror Pole

Fortunately, the presen e of the zero tends to negate the effect of the pole. Generally, the pole and zero due to C_3 is greater than GB and will have very little influence on the stability of the two-stage op amp.

The plot shown illustrates the case where these roots are less than GB and even then they have little effect on stability.

In fact, they actually increase the phase margin slightly because GB is decreased.



Summary of the Condition for Stability of the two stage op amp

- Unity-gainbandwith is given as:

$$GB = A_v(0)\cdot|p_1| = (g_{mI}g_{mII}R_IR_{II})\cdot\left(\frac{1}{g_{mII}R_IR_{II}C_c}\right) = \frac{g_{mI}}{C_c} = (g_{m1}g_{m2}R_1R_2)\cdot\left(\frac{1}{g_{m2}R_1R_2C_c}\right) = \frac{g_{m1}}{C_c}$$

- The requirement for 45° phase margin is:

$$\pm180° - \text{Arg}[AF] = \pm180° - \tan^{-1}\left(\frac{\omega}{|p1|}\right) - \tan^{-1}\left(\frac{\omega}{|p2|}\right) - \tan^{-1}\left(\frac{\omega}{z}\right) = 45°$$

Let $\omega = GB$ and assume that $z \geq 10GB$, therefore we get,

$$\pm180° - \tan^{-1}\left(\frac{GB}{|p1|}\right) - \tan^{-1}\left(\frac{GB}{|p2|}\right) - \tan^{-1}\left(\frac{GB}{z}\right) = 45°$$

$$135° \approx \tan^{-1}(A_v(0)) + \tan^{-1}\left(\frac{GB}{|p2|}\right) + \tan^{-1}(0.1) = 90° + \tan^{-1}\left(\frac{GB}{|p2|}\right) + 5.7°$$

$$39.3° \approx \tan^{-1}\left(\frac{GB}{|p2|}\right) \Rightarrow \frac{GB}{|p2|} = 0.818 \Rightarrow \boxed{|p2| \geq 1.22GB}$$

- The requirement for 60° phase margin:

$$\boxed{|p2| \geq 2.2GB \text{ if } z \geq 10GB}$$

- If 60° phase margin is required, then the following relationships apply:

$$\frac{g_{m6}}{C_c} > \frac{10g_{m1}}{C_c} \Rightarrow \boxed{g_{m6} > 10g_{m1}} \quad \text{and} \quad \frac{g_{m6}}{C_2} > \frac{2.2g_{m1}}{C_c} \Rightarrow \boxed{C_c > 0.22C_2}$$

Controlling the right-half plane (RHP) zero

Why is the RHP zero a problem?

Because it boosts the magnitude but lags the phase - the worst possible combination for stability.

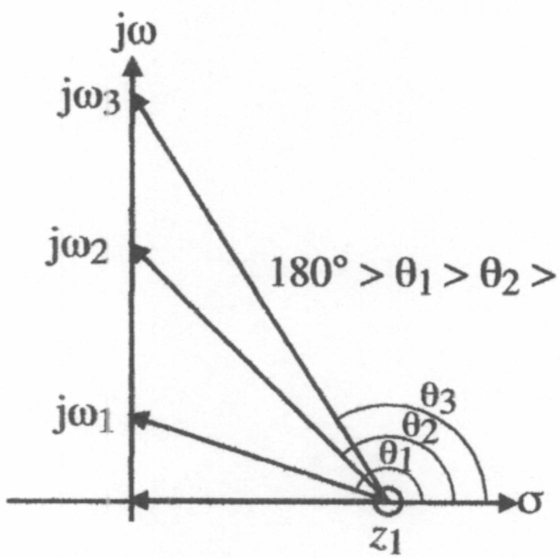


Fig. 430-01

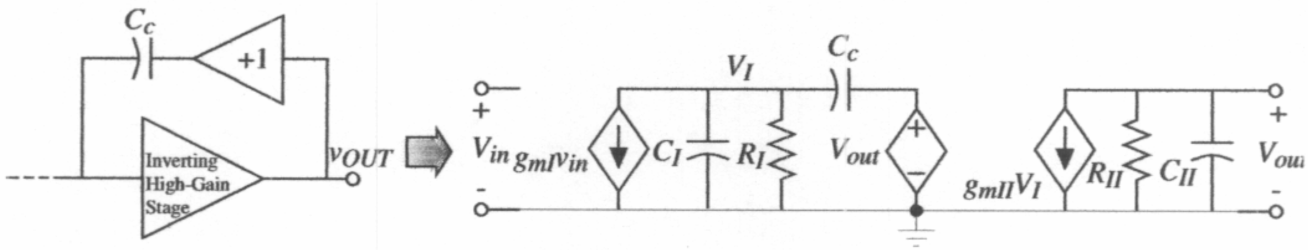
Solution of the problem:

If a zero is caused by two paths to the output, then eliminate one of the paths.

Use of buffer to eliminate the feedforward path through the Miller Capacitor

Model:

The transfer function is given by the following equation,



$$\frac{V_o(s)}{V_{in}(s)} = \frac{(g_{mI})(g_{mII})(R_I)(R_{II})}{1 + s[R_IC_I + R_{II}C_{II} + R_IC_c + g_{mII}R_IR_{II}C_c] + s^2[R_IR_{II}C_{II}(C_I + C_c)]}$$

Using the technique as before to approximate p_1 and p_2 results in the following

$$p_1 \cong \frac{-1}{R_IC_I + R_{II}C_{II} + R_IC_c + g_{mII}R_IR_{II}C_c} \cong \frac{-1}{g_{mII}R_IR_{II}C_c}$$

and

$$p_2 \cong \frac{-g_{mII}C_c}{C_{II}(C_I + C_c)}$$

Comments:

Poles are approximately what they were before with the zero removed.

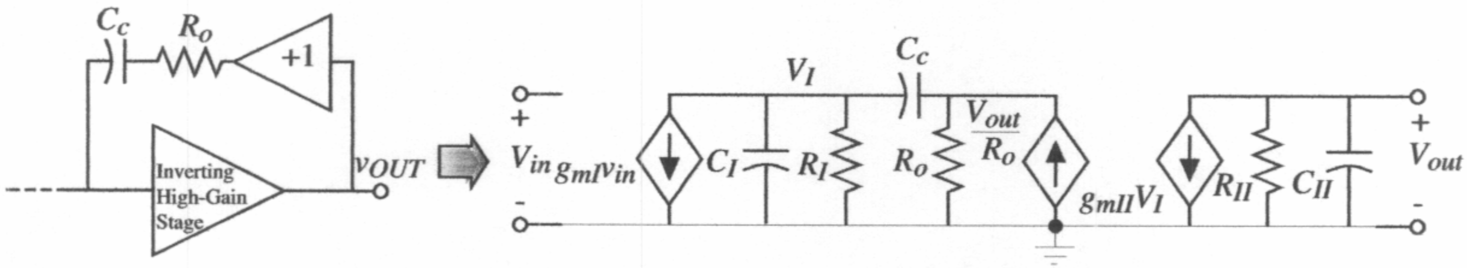
For 45° phase margin, $|p_2|$ must be greater than GB

For 60° phase margin, $|p_2|$ must be greater than $1.73GB$

Use of Buffer with Finite Output Resistance to Eliminate the RHP Zero

Assume that the unity-gain buffer has an output resistance of R_o.

Model:



It can be shown that if the output resistance of the buffer amplifier, R_o, is not neglected that another pole occurs at,

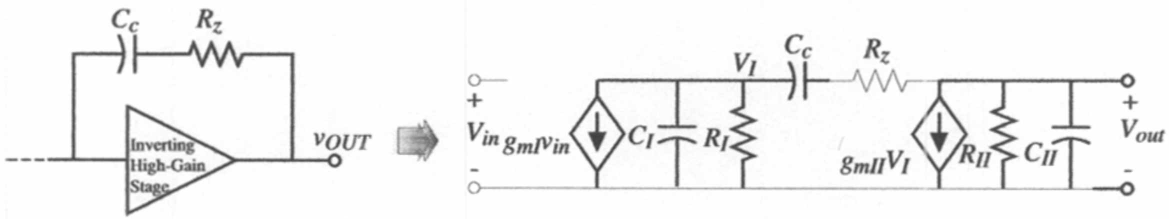
$$p_4 \cong \frac{-1}{R_o[C_I C_c/(C_I + C_c)]}$$

and a LHP zero at

$$z_2 \cong \frac{-1}{R_o C_c}$$

Closer examination shows that if a resistor, called a *nulling resistor*, is placed in series with C_c that the RHP zero can be eliminated or moved to the LHP.

Use of nulling Resistor to Eliminate the RHP Zero (or turn it into a LHP zero)



Nodal equations:

$$g_{mI}V_{in} + \frac{V_I}{R_I} + sC_IV_I + \left(\frac{sC_c}{1 + sC_cR_z}\right)(V_I - V_{out}) = 0$$

$$g_{mII}V_I + \frac{V_o}{R_{II}} + sC_{II}V_{out} + \left(\frac{sC_c}{1 + sC_cR_z}\right)(V_{out} - V_I) = 0$$

Solution:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{a\{1 - s[(C_c/g_{mII}) - R_zC_c]\}}{1 + bs + cs^2 + ds^3}$$

where

$$a = g_{mI}g_{mII}R_IR_{II}$$
$$b = (C_{II} + C_c)R_{II} + (C_I + C_c)R_I + g_{mII}R_IR_{II}C_c + R_zC_c$$
$$c = [R_IR_{II}(C_IC_{II} + C_cC_I + C_cC_{II}) + R_zC_c(R_IC_I + R_{II}C_{II})]$$
$$d = R_IR_{II}R_zC_IC_{II}C_c$$

Use of nulling Resistor to Eliminate the RHP Zero

If R_z is assumed to be less than R_I or R_{II} and the poles widely spaced, then the roots of the above transfer function can be approximated as

$$p_1 \cong \frac{-1}{(1+g_{mII}R_{II})R_I C_c} \cong \frac{-1}{g_{mII}R_{II}R_I C_c}$$

$$p_2 \cong \frac{-g_{mII}C_c}{C_I C_{II} + C_c C_I + C_c C_{II}} \cong \frac{-g_{mII}}{C_{II}}$$

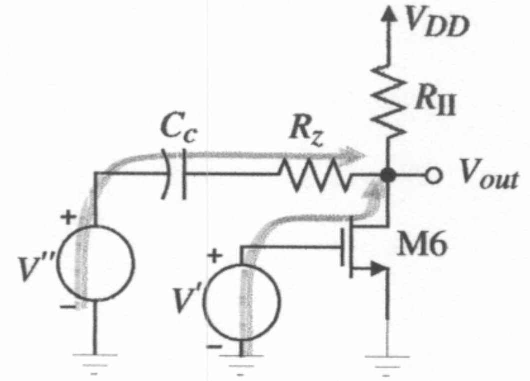
$$p_4 = \frac{-1}{R_z C_I}$$

and

$$z_1 = \frac{1}{C_c(1/g_{mII} - R_z)}$$

Note that the zero can be placed anywhere on the real axis.

Conceptual Illustration of the Nulling Resistor Approach



The output voltage, V_{out}, can be written as

$$V_{out} = \frac{-g_{m6}R_{II}\left(R_z + \frac{1}{sC_c}\right)}{R_{II} + R_z + \frac{1}{sC_c}} V' + \frac{R_{II}}{R_{II} + R_z + \frac{1}{sC_c}} V'' = \frac{-R_{II}\left[g_{m6}R_z + \frac{g_{m6}}{sC_c} - 1\right]}{R_{II} + R_z + \frac{1}{sC_c}} V$$

when $V = V' = V''$.

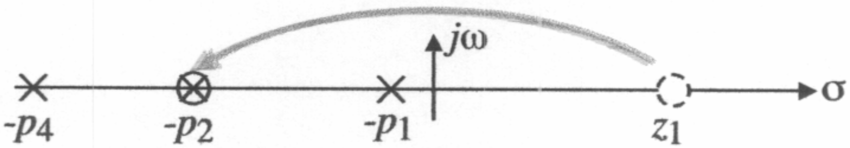
Setting the numerator equal to zero and assuming $g_{m6} = g_{mII}$ gives,

$$z_1 = \frac{1}{C_c(1/g_{mII} - R_z)}$$

A Design Procedure that Allows the RHP Zero to Cancel the Output Pole, p2

We desire that $z_1 = p_2$ in terms of the previous notation.
Therefore,

$$\frac{1}{C_c(1/g_{mII} - R_z)} = \frac{-g_{mII}}{C_{II}}$$



The value of R_z can be found as

$$R_z = \left(\frac{C_c + C_{II}}{C_c}\right)(1/g_{mII})$$

With p_2 canceled, the remaining roots are p_1 and p_4(the pole due to R_z) . For unity-gain stability, all that is required is that

$$|p_4| > A_v(0)|p_1| = \frac{A_v(0)}{g_{mII}R_{II}R_IC_c} = \frac{g_{mI}}{C_c}$$

and

$$(1/R_zC_I) > (g_{mI}/C_c) = GB$$

Substituting R_z into the above inequality and assuming $C_{II} >> C_c$ results in

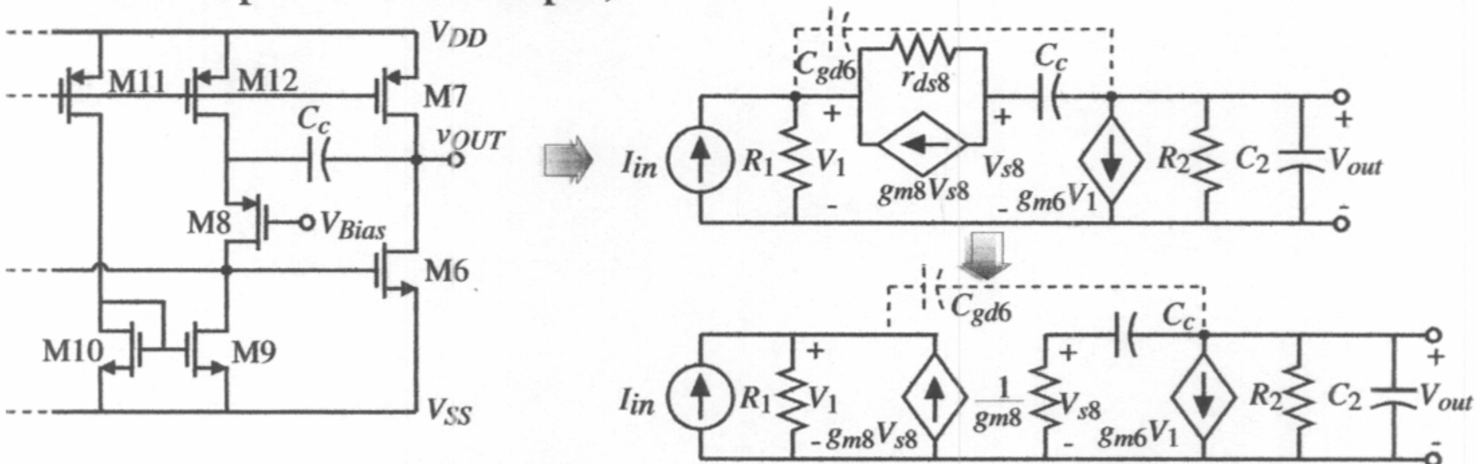
$$C_c > \sqrt{\frac{g_{mI}}{g_{mII}}C_IC_{II}}$$

This procedure gives excellent stability for a fixed value of C_{II} ($\approx C_L$).

Unfortunately, as C_L changes, p_2 changes and the zero must be readjusted to cancel p_2.

Increasing the magnitude of the output pole

The magnitude of the output pole , p_2, can be increased by introducing gain in the Miller capacitor feedback path. For example,



The resistors R_1 and R_2 are defined as

$$R_1 = \frac{1}{g_{ds2} + g_{ds4} + g_{ds9}} \quad \text{and} \quad R_2 = \frac{1}{g_{ds6} + g_{ds7}}$$

where transistors M2 and M4 are the output transistors of the first stage.

Nodal equations:

$$I_{in} = G_1V_1 - g_{m8}V_{s8} = G_1V_1 - \left(\frac{g_{m8}sC_c}{g_{m8} + sC_c}\right) V_{out} \quad \text{and} \quad 0 = g_{m6}V_1 + \left[G_2 + sC_2 + \frac{g_{m8}sC_c}{g_{m8} + sC_c}\right] V_{out}$$

Increasing the magnitude of the output pole

Solving for the transfer function V_{out}/I_{in} gives,

$$\frac{V_{out}}{I_{in}} = \left(\frac{-g_{m6}}{G_1 G_2}\right)\left[\frac{\left(1+\frac{sC_c}{g_{m8}}\right)}{1+s\left[\frac{C_c}{g_{m8}}+\frac{C_2}{G_2}+\frac{C_c}{G_2}+\frac{g_{m6}C_c}{G_1G_2}\right]+s^2\left(\frac{C_cC_2}{g_{m8}G_2}\right)}\right]$$

Using the approximate method of solving for the roots of the denominator gives

$$p_1 = \frac{-1}{\frac{C_c}{g_{m8}}+\frac{C_c}{G_2}+\frac{C_2}{G_2}+\frac{g_{m6}C_c}{G_1G_2}} \approx \frac{-6}{g_{m6}r_{ds}{}^2C_c}$$

and

$$p_2 \approx \frac{-\frac{g_{m6}r_{ds}{}^2C_c}{6}}{\frac{C_cC_2}{g_{m8}G_2}} = \frac{g_{m8}r_{ds}{}^2G_2}{6}\left(\frac{g_{m6}}{C_2}\right) = \left(\frac{g_{m8}r_{ds}}{3}\right)|p_2'|$$

where all the various channel resistance have been assumed to equal r_{ds} and p_2' is the output pole for normal Miller compensation.

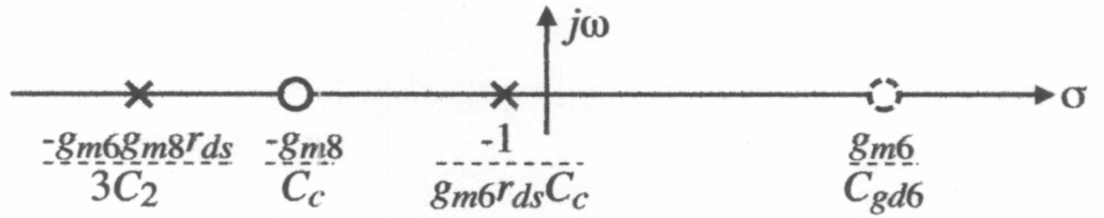
Result:

Dominant pole is approximately the same and the output pole is increased by $\approx g_m r_{ds}$.

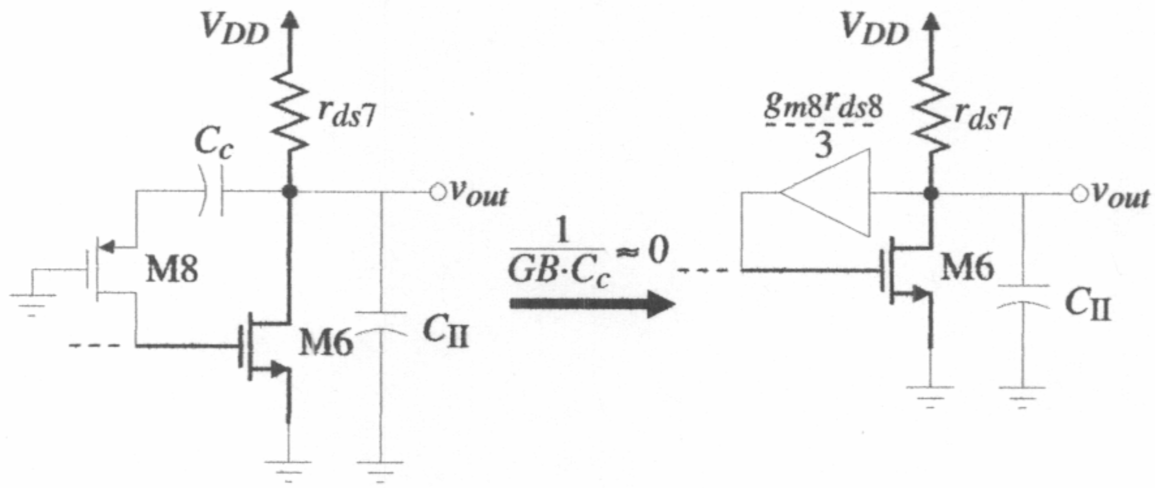
Increasing the magnitude of the output pole

In addition there is a LHP zero at $-g_{m8}/sC_c$ and a RHP zero due to C_{gd6} (shown dashed in the model) at $g_{m6}/Cgd6$.

Roots are:



Concept behind the increasing of magnitude of the output pole



$$R_{out} = r_{ds7} \| \left(\frac{3}{g_{m6} g_{m8} r_{ds8}} \right) \approx \frac{3}{g_{m6} g_{m8} r_{ds8}}$$

Therefore, the output pole is approximately,

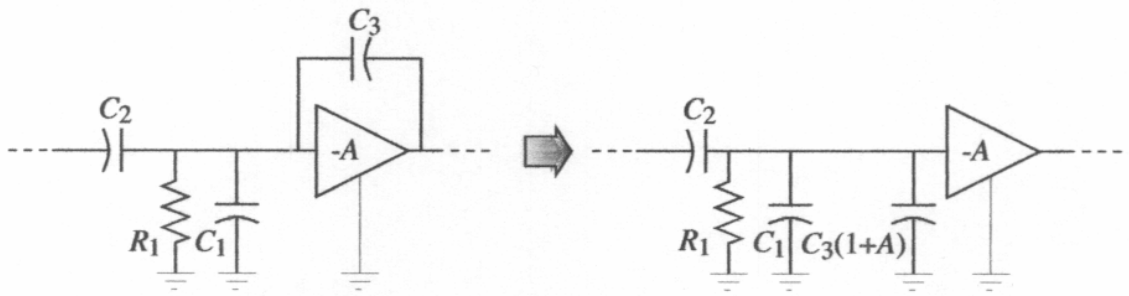
$$|p_2| \approx \frac{g_{m6} g_{m8} r_{ds8}}{3C_{II}}$$

Identification of poles from a schematic

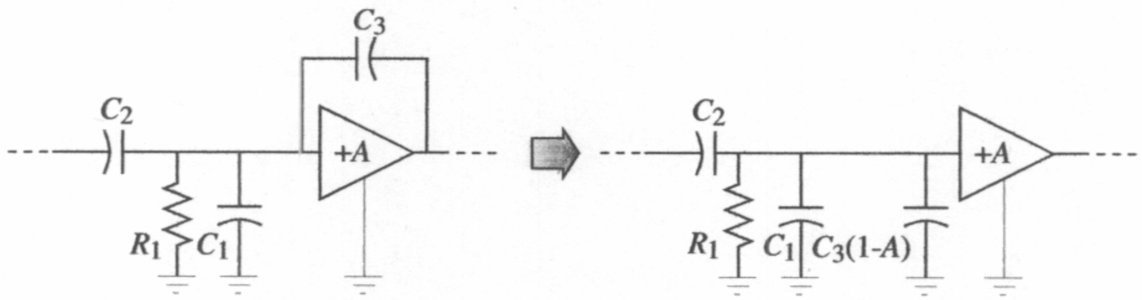
1.) Most poles are equal to the reciprocal product of the resistance from a node to ground and the capacitance connected to that node.

2.) Exceptions (generally due to feedback):

a.) Negative feedback:

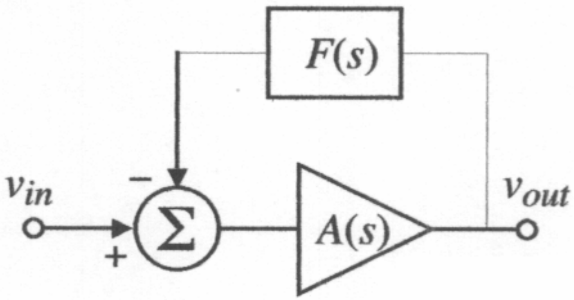


b.) Positive feedback (A<1):



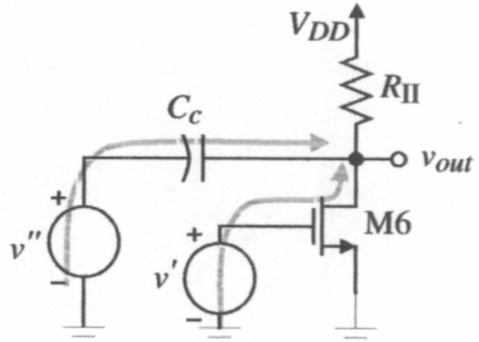
Identification of zeros from a schematic

1.) Zeros arise from poles in the feedback path.



$$\text{If } F(s) = \frac{1}{\frac{s}{p_1}+1}, \text{ then } \frac{V_{out}}{V_{in}} = \frac{A(s)}{1+A(s)F(s)} = \frac{A(s)}{1+A(s)\frac{1}{\frac{s}{p_1}+1}} = \frac{A(s)\left(\frac{s}{p_1}+1\right)}{\frac{s}{p_1}+1+A(s)}$$

2.) Zeros are also created by two paths from the input to the output and one of more of the paths is frequency dependent.



Feedforward compensation

Use two parallel paths to achieve a LHP zero for lead compensation purposes.

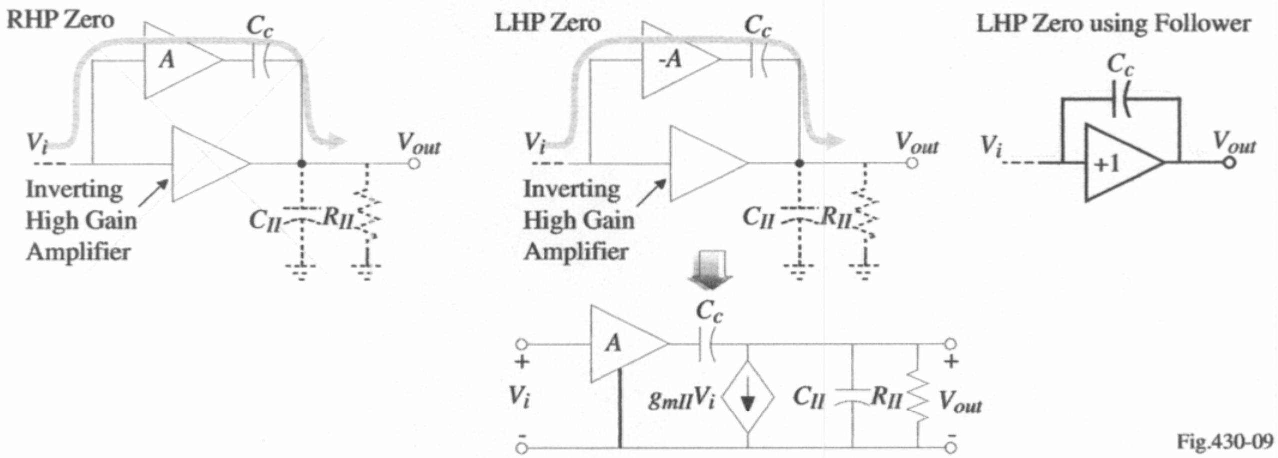


Fig.430-09

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{AC_c}{C_c + C_{II}}\left(\frac{s + g_{mII}/AC_c}{s + 1/[R_{II}(C_c + C_{II})]}\right)$$

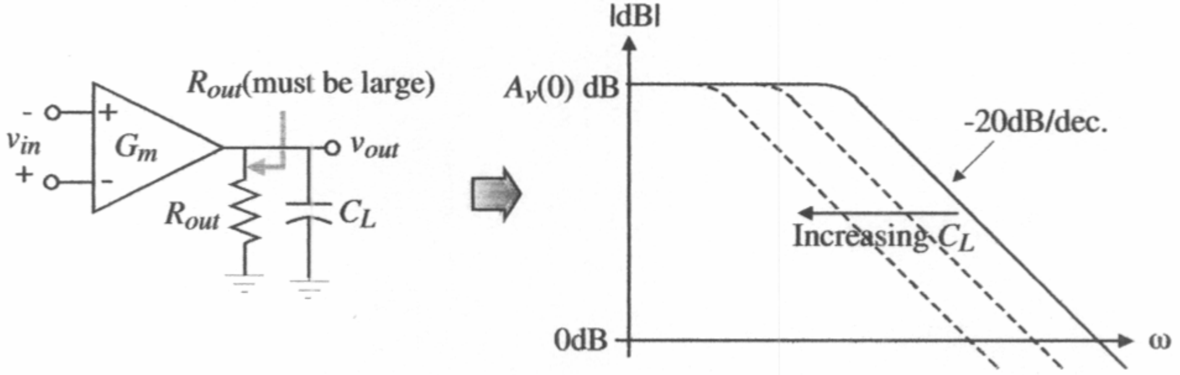
To use the LHP zero for compensation, a compromise must be observed.

- Placing the zero below *GB* will lead to boosting of the loop gain that could deteriorate the phase margin.
- Placing the zero above *GB* will have less influence on the leading phase caused by the zero.

Note that a source follower is a good candidate for the use of feedforward compensation.

Self-compensated Op Amp

Self compensation occurs when the load capacitor is the compensation capacitor (can never be unstable for resistive feedback)



Voltage gain:

$$\frac{v_{out}}{v_{in}} = A_v(0) = G_m R_{out}$$

Dominant pole:

$$p_1 = \frac{-1}{R_{out} C_L}$$

Unity-gainbandwidth:

$$GB = A_v(0) \cdot |p_1| = \frac{G_m}{C_L}$$

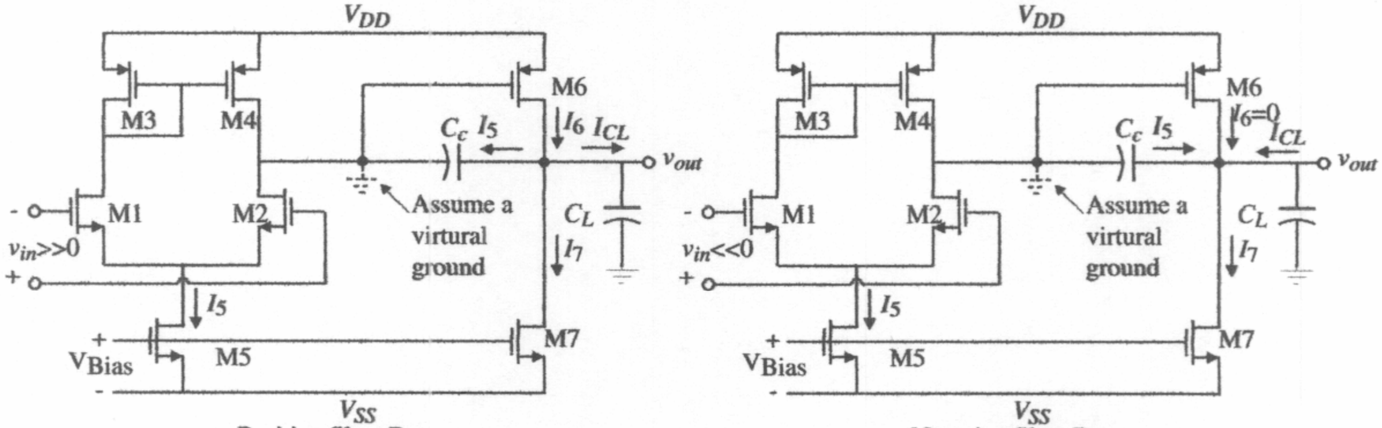
Stability:

Large load capacitors simply reduce *GB* but the phase is still 90° at *GB*.

Slew Rate of a two-stage CMOS Op Amp

Remember that slew rate occurs when currents flowing in a capacitor become limited and is given as

$$I_{lim} = C\frac{dv_C}{dt}$$ where v_C is the voltage across the capacitor C.



Positive Slew Rate

Negative Slew Rate

$$SR^{+} = \min\left[\frac{I_5}{C_c}, \frac{I_6\text{-}I_5\text{-}I_7}{C_L}\right] = \frac{I_5}{C_c} \text{ because } I_6{>>}I_5 \qquad SR^{-} = \min\left[\frac{I_5}{C_c}, \frac{I_7\text{-}I_5}{C_L}\right] = \frac{I_5}{C_c} \text{ if } I_7{>>}I_5.$$

Therefore, if C_L is not too large and if I_7 is significantly greater than I_5, then the slew rate of the two-stage op amp should be,

$$SR = \frac{I_5}{C_c}$$