# 5. CMOS Operational Amplifiers

## Analog Design for CMOS VLSI Systems

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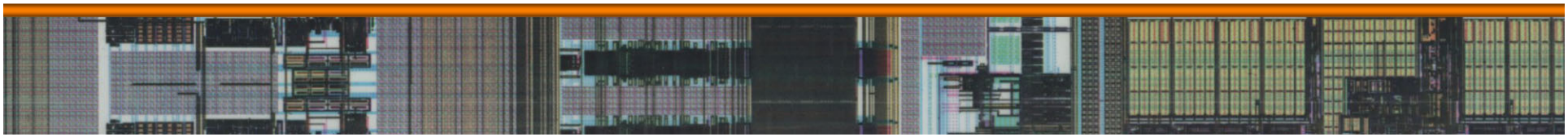
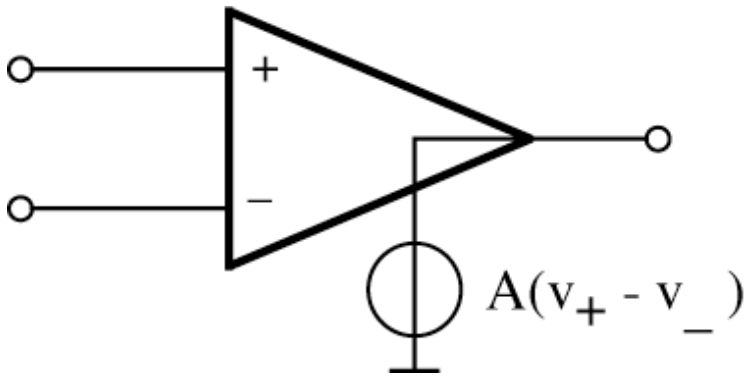


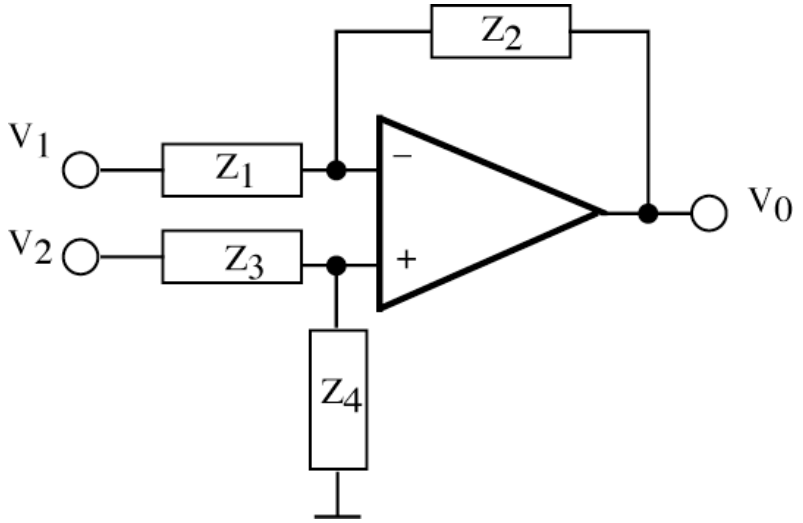
# Basic op-amp

The ideal operational amplifier is a voltage controlled voltage source with infinite gain, infinite input impedance and zero output impedance.




The op-amp is always used in feedback configuration.

# Typical feedback configuration




$$V_0 = V_2 \frac{Z_4}{Z_3 + Z_4} \frac{Z_1 + Z_2}{Z_1} - V_1 \frac{Z_2}{Z_1}$$

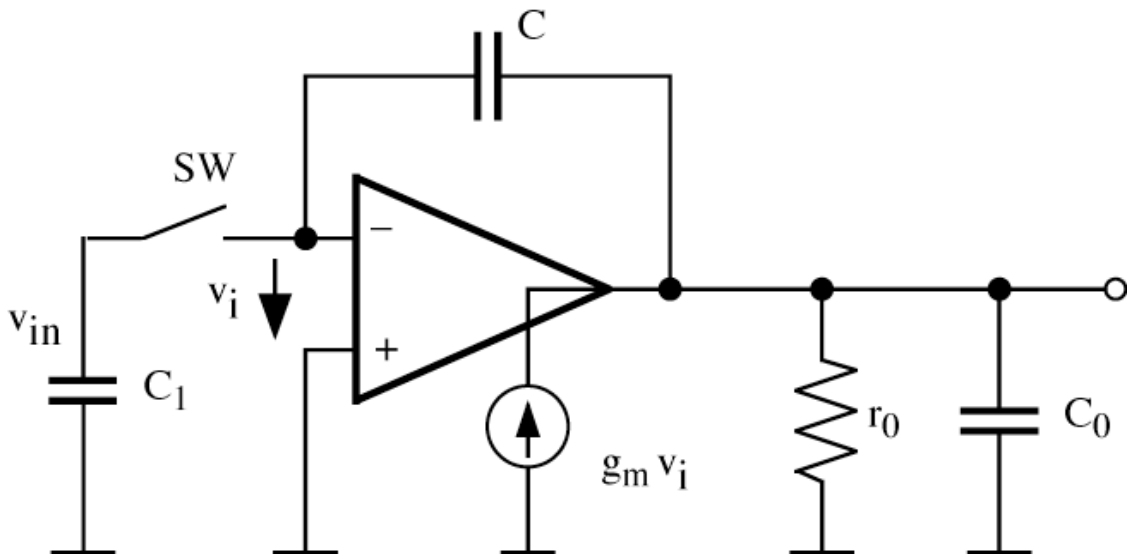
Finite gain effect:

$$V_0 = \left( V_2 \frac{Z_4}{Z_3 + Z_4} \frac{Z_1 + Z_2}{Z_1} - V_1 \frac{Z_2}{Z_1} \right) \Bigg/ \left( 1 + \frac{Z_1 + Z_2}{A_0 Z_1} \right)$$

The error due to the finite gain is proportional to 1 / $A_0$. This error must be smaller than the error due to impedance mismatch.

## OTA

If impedances are implemented with capacitors and switches, after a transient, the load of the op-amp is made of pure capacitors. The behavior of the circuit does not depend on the output resistance of the op-amp and stages with high output resistance (operational transconductance amplifiers) can be used.



## Transient

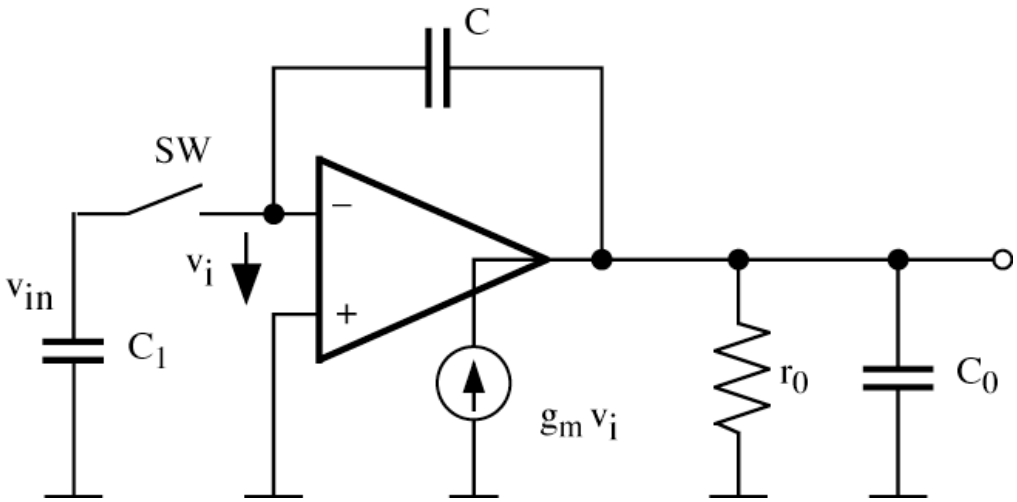
$$V_i(0^+) = V_{in}\frac{C_1}{C_1 + C \,//\, C_0}$$

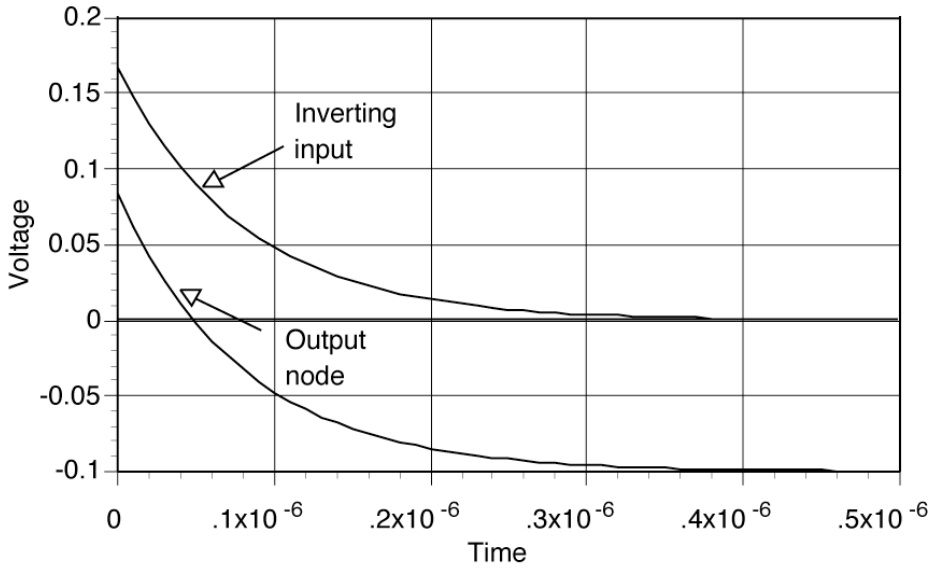
$$V_o(0^+) = V_i(0^+)\frac{C}{C_0 + C}$$

$$V_i(\infty) = V_{in}\frac{C_1 + C}{C_1 + C(1 + g_m r_0)}$$

$$V_o(\infty) = -V_i(\infty)\, g_m\, r_0$$

$$\tau \approx \frac{C_0}{g_m}$$



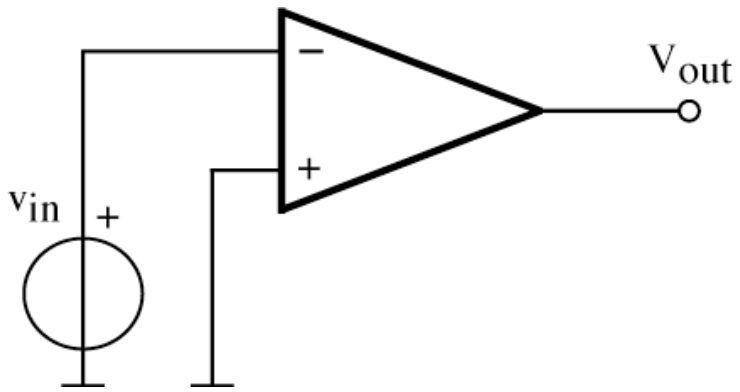



# Performance characteristics

Actual op-amps deviate from the ideal behavior. The differences are described by the performance characteristics.

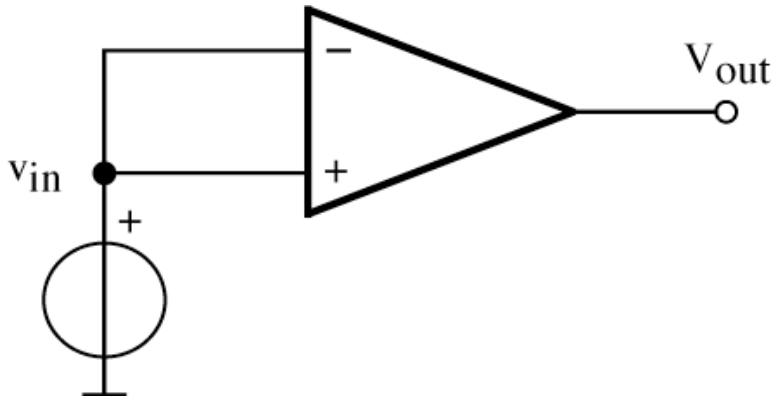
## DC differential gain:

It is the open-loop voltage gain measured at DC with a small differential input signal. Typically $A_d$ = 80 ÷ 100 dB.



## Common mode gain:

It is the open-loop voltage gain with a small signal applied to both the input terminals. $A_{cm}$ = 20 ÷ 40 dB.



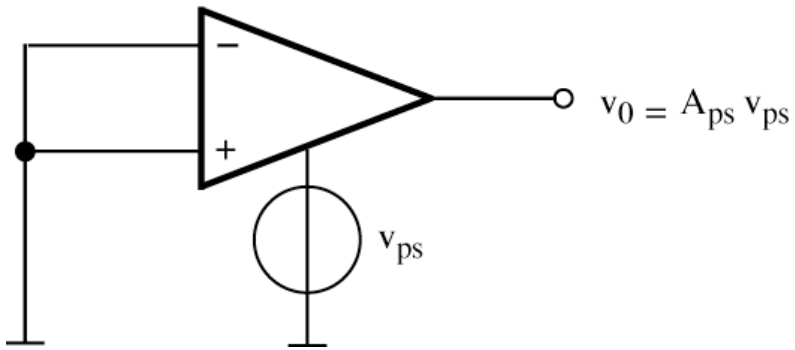

## Common mode rejection ratio:

It is defined as the ratio between the differential gain and the common mode gain. Typically CMRR = 40 ÷ 80 dB.

## Power supply rejection ratio:

If a small signal is applied in series with the positive (or negative) power supply, it is transferred to the output with a given gain $A_{ps+}$ (or $A_{ps-}$).

The ratios between differential gain and power supply gains furnish the two PSRRs.



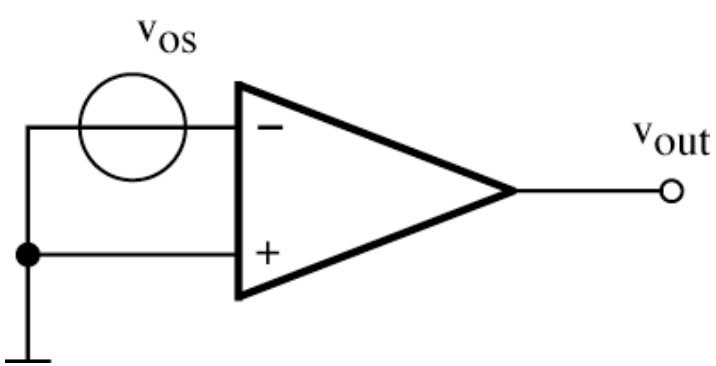

Typically: PSRR = 90 dB (DC)

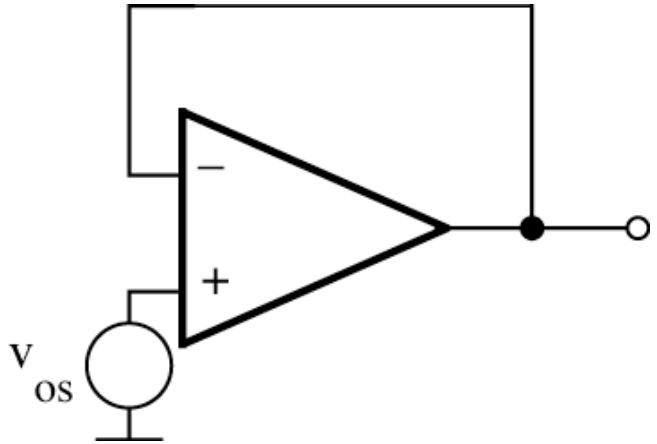
PSRR = 60 dB (1 kHz)

PSRR = 30 dB (100 kHz)

## Input offset voltage:

In real circuits if the two input terminals are set at the same voltage the output saturates close to $V_{DD}$ or to $V_{SS}$.




Typically $|V_{os}| = 4 \div 6$ mV.

## Input common mode range:

It is the maximum range of the common-mode input voltage which do not produce a significant variation of the differential gain.

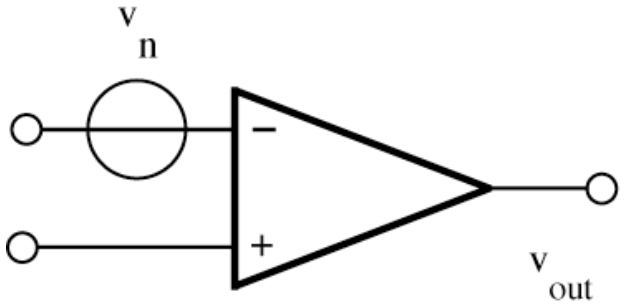
## Output voltage swing:

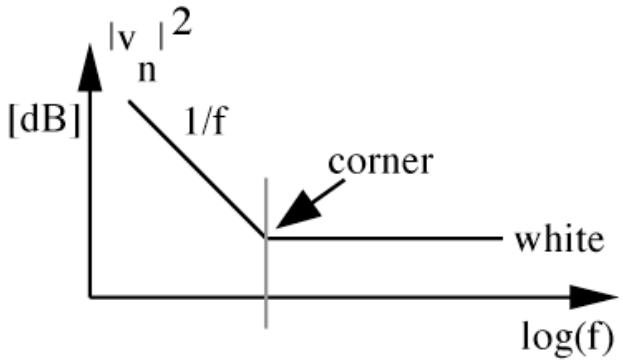
It is the swing of the output node without generating a defined amount of harmonic distortion.

## Equivalent input noise:

The noise performances can be described in terms of an equivalent voltage source at the input of the op-amp.

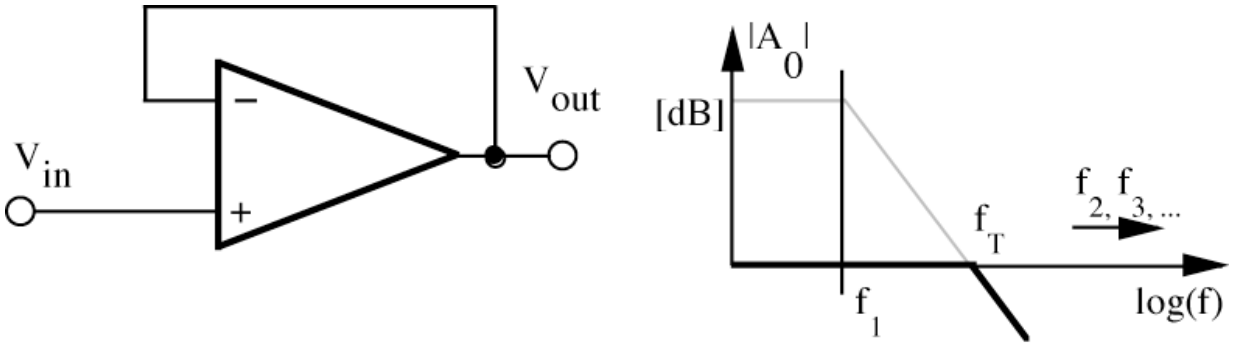
Typically $v_n$ = 40 ÷ 50 nV/√Hz at 1 kHz,
in a wide band (1 MHz) it results 10 ÷ 50 μV RMS.



## Unity gain frequency:

It is the frequency where the open-loop gain is zero. It is also the -3 dB bandwidth in unity-gain closed loop conditions. Typically $f_T$ = 200 MHz.

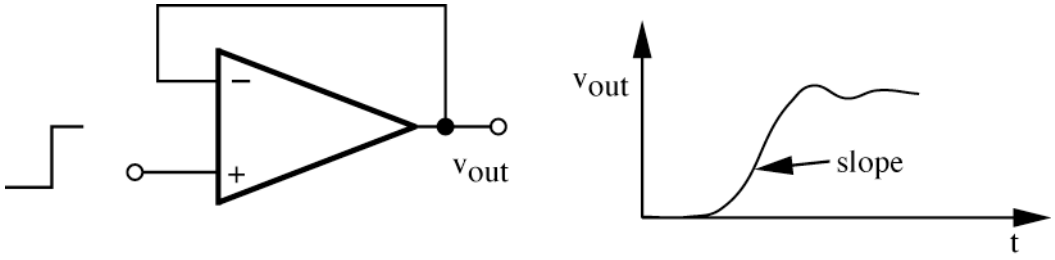



## Phase margin:

It is the phase shift of the small-signal differential gain measured at the unity gain frequency. A phase margin smaller than 60° causes ringing in the output response.

## Slew rate:

It is the maximum slope of the output voltage. Usually it is measured in the buffer configuration. The positive slew rate can be different from the negative slew rate. Typically SR = 50 ÷ 200 V/μs (lower values for micropower operation).




## Settling time:

The settling time is the time required to settle the output within a given range (usually ± 0.1%) of the final value.

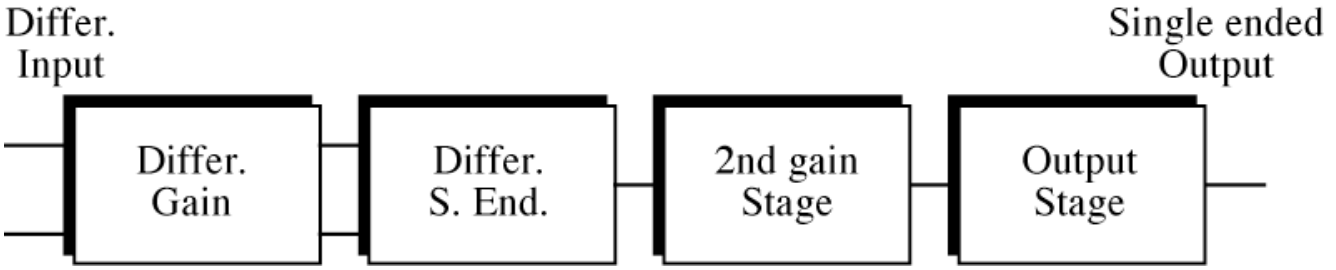
## Power dissipation:

It depends on speed and bandwidth requirements. Typically, for 3.3 V supply, it is around 1 mW.

# Typical parameters of a 0.25 µm OTA

| Feature | Value | Unit |
|---|---|---|
| DC gain | 80 | dB |
| CMRR | 40 | dB |
| Offset | 4-6 | mV |
| Bandwidth | 100 | MHz |
| Slew-rate | 3 | V/µs |
| Settling time: 1 V, $C_L$ = 4 pF | 300 | ns |
| PSRR @ DC | 90 | dB |
| PSRR @ 1 kHz | 60 | dB |
| PSRR @ 100 kHz | 30 | dB |
| Input referred noise (white) | 100 | nV/√Hz |
| Corner frequency | 1 | kHz |
| Supply voltage | 3.3 | V |
| Input common mode voltage | 1.5 | V |
| Output dynamic range | 2.2 | $V_{pp}$ |
| Power consumption | 1 | mW |
| Silicon area | 2000 | µm$^2$ |

# Basic architecture

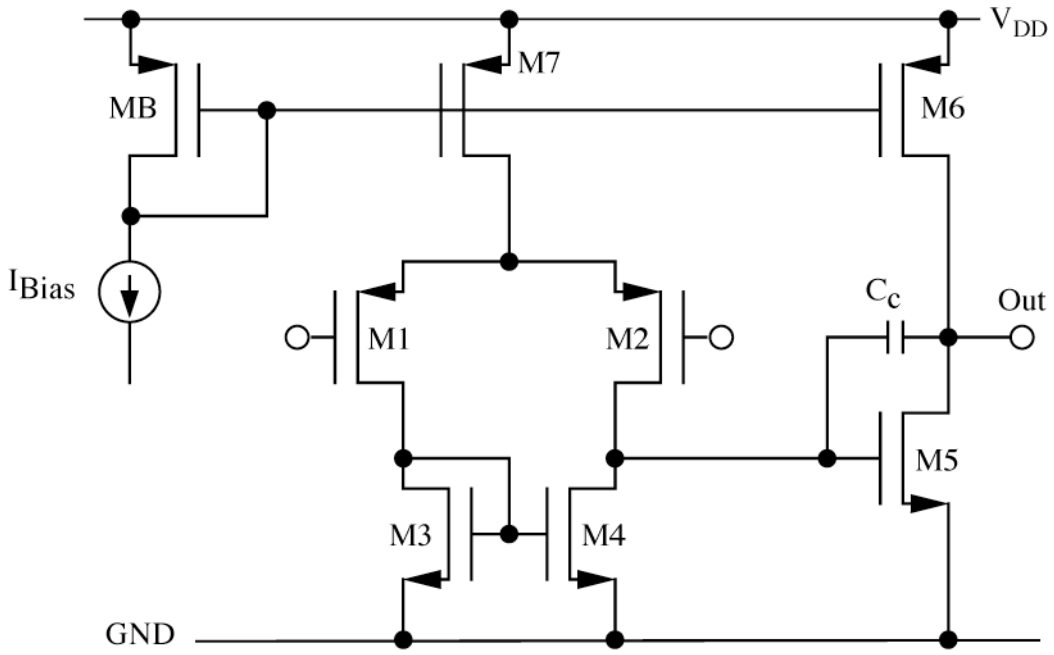



- 1st gain stage
- differential to single-ended converter
- 2nd gain stage
- output stage (to reduce the output impedance)

## Key requirements:

- absolute stability in unity gain closed-loop conditions when driving maximum load.
- minimum number of gain stages.

# Two-stage op-amp




## Key design issues:

- open-loop differential gain
- dc offset
- power supply rejection (PSRR)

## Open-loop differential gain:

The gain is obtained by multiplying the gains of the two stages.

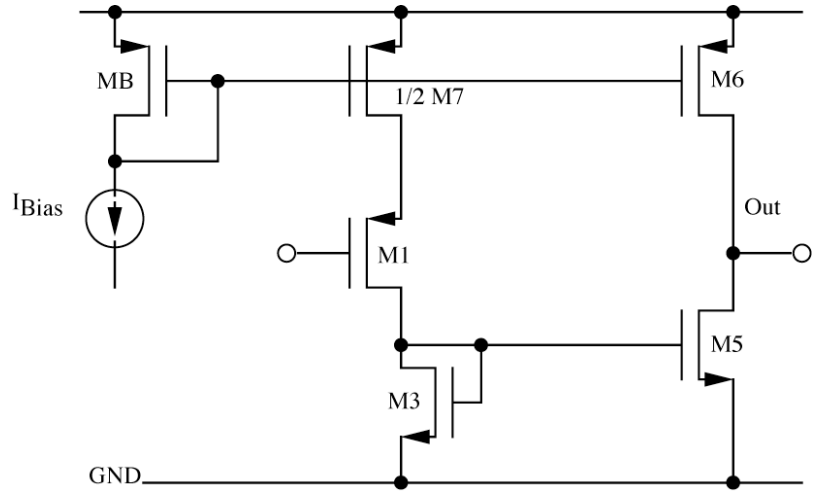
$$A_v = A_1 A_2 = \frac{g_{m1}}{(g_{ds2} + g_{ds4})} \frac{g_{m5}}{(g_{ds5} + g_{ds6})} =$$

$$= \frac{2\sqrt{2\mu_n \mu_p} C_{ox}}{(\lambda_n + \lambda_p)^2} \frac{\sqrt{\left(\frac{W}{L}\right)_1} \sqrt{\left(\frac{W}{L}\right)_5} \left(\frac{W}{L}\right)_B}{\sqrt{\left(\frac{W}{L}\right)_6} \sqrt{\left(\frac{W}{L}\right)_7}} \frac{1}{I_{Bias}}$$

At low frequency the gain is inversely proportional to the bias current.

## Common mode dc gain:

Applying the same signal to both inputs the circuit becomes symmetrical and can be studied considering half circuit.




$$A_{CM} = A_{CM1}A_{CM2} = \left(\frac{-g_{ds7}}{2g_{m1}}\right)\left(\frac{-g_{m5}}{g_{ds5}+g_{ds6}}\right)$$

$$CMRR = \frac{A_v}{A_{CM}} = \frac{2g_{m1}g_{m3}}{g_{ds7}(g_{ds2}+g_{ds4})}$$

## Offset:

The offset is composed of two terms:

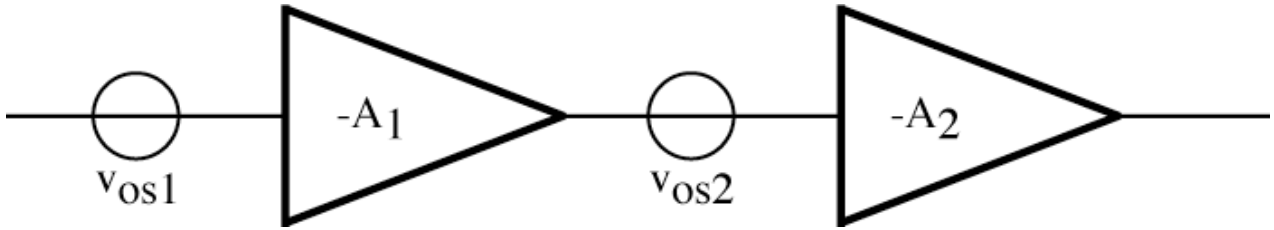
- systematic offset
- random offset

The ***systematic offset*** can be reduced to zero with a careful design. A necessary condition to have zero systematic offset, is that the currents of M5 and M6 are equal, when the inputs are connected to the same voltage. Assuming all the transistors in saturation this condition is:

$$I_{Bias}\frac{(W/L)_6}{(W/L)_B} = I_{Bias}\frac{(W/L)_7}{(W/L)_B}\frac{(W/L)_5}{(W/L)_3}$$

$$(W/L)_3(W/L)_6 = \frac{1}{2}(W/L)_7(W/L)_5$$

The ***random offset*** is due to the geometrical mismatching and process dependent inaccuracies.

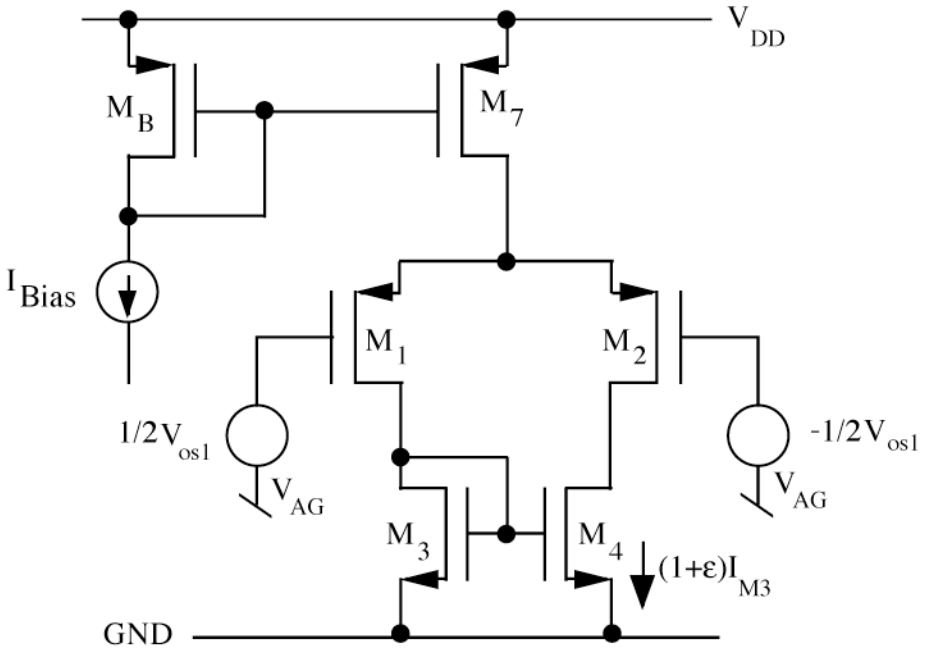



When we refer the offset of the second stage at the input terminal we have to divide it by the gain of the first stage. Since the two offsets are uncorrelated we have:

$$V_{os} = \sqrt{V_{os1}^2 + \left(\frac{V_{os2}}{A_1}\right)^2}$$

The total offset is dominated by the offset of the input stage.

We study the effect of a mismatch between M3 and M4: mirror factor (1 + $\varepsilon$) instead of 1.




$$\left(\frac{I_{Bias}}{2} - g_{m1}\frac{V_{os1}}{2}\right)(1+\varepsilon) = \left(\frac{I_{Bias}}{2} + g_{m2}\frac{V_{os1}}{2}\right)$$

$$V_{os1} \approx \frac{I_1}{g_{m1}}\varepsilon$$

## MOS:

$$\frac{I_1}{g_{m1}} = \frac{V_{GS1} - V_{Th}}{2} = 150 \div 300 \text{ mV} \qquad \text{(in saturation)}$$

$$\frac{I_1}{g_{m1}} = nV_T = \frac{nkT}{q} \qquad \text{(in sub-threshold)}$$

## BJT:

$$\frac{I_1}{g_{m1}} \approx 26 \text{ mV}$$

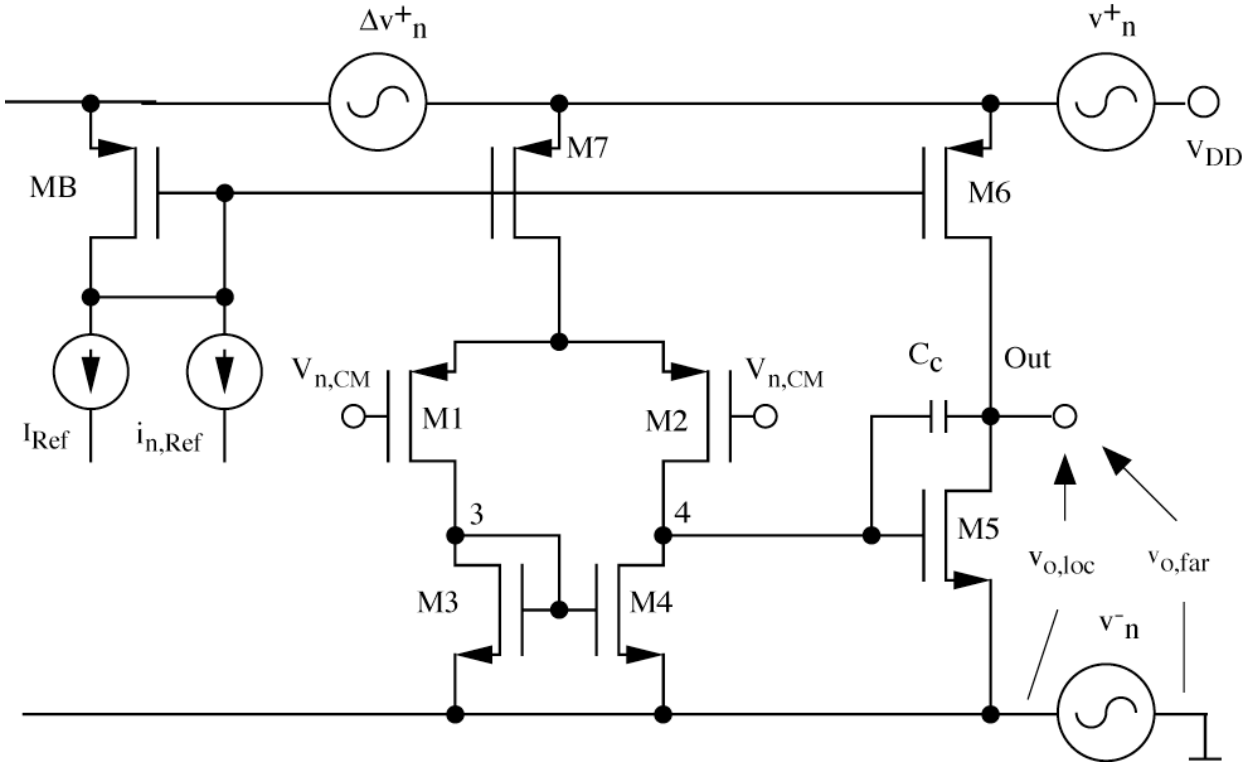
Assuming $\varepsilon = 0.01$:

$V_{os,\text{BJT}} = 0.26$ mV

$V_{os,\text{MOS}} = 1.5 \div 3$ mV

## Power supply rejection:

A signal on the positive bias line determines a modulation in the reference current, which, in turn, gives an equal modulation of the currents in M5 and M6, if the condition of the zero systematic offset is fulfilled.

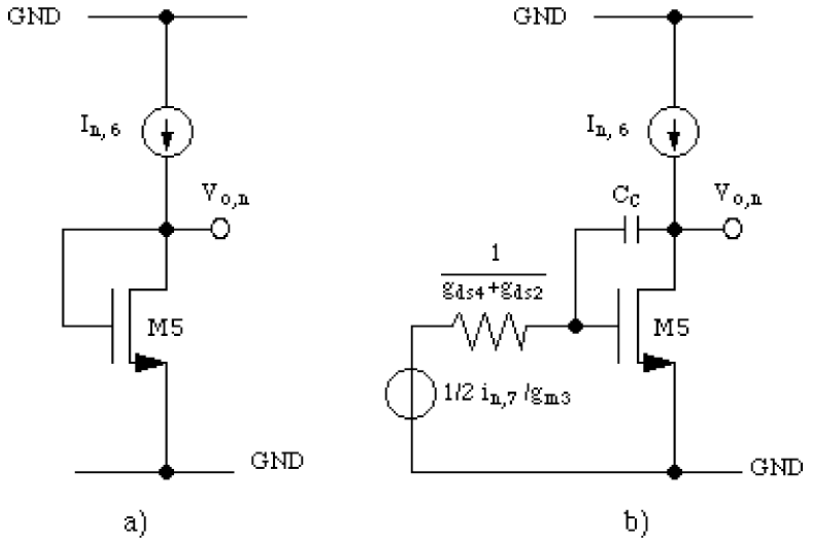


The spur signal $\Delta v^+_n$ affects the currents of M5 and M6.

$$\frac{i_{n,6}}{(W/L)_6} = \frac{i_{n,7}}{(W/L)_7} = \mu C_{ox}\left(V_{GS,MB} - V_{Th}\right)\Delta v_n^+$$

**a)** low frequency:

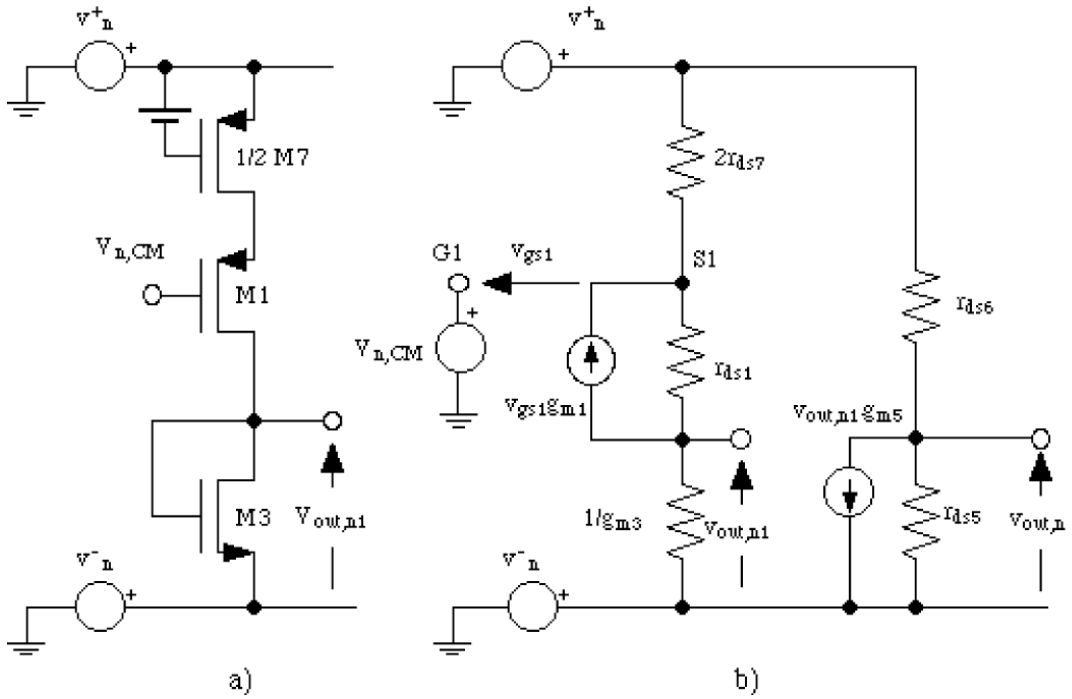
$$v_{o,n,1} = i_{n,tot}\left[\frac{(W/L)_6}{(W/L)_B} - \frac{1}{2}\frac{(W/L)_5(W/L)_7}{(W/L)_4(W/L)_B}\right]\frac{1}{g_{ds6}+g_{ds7}}$$




**b)** high frequency:

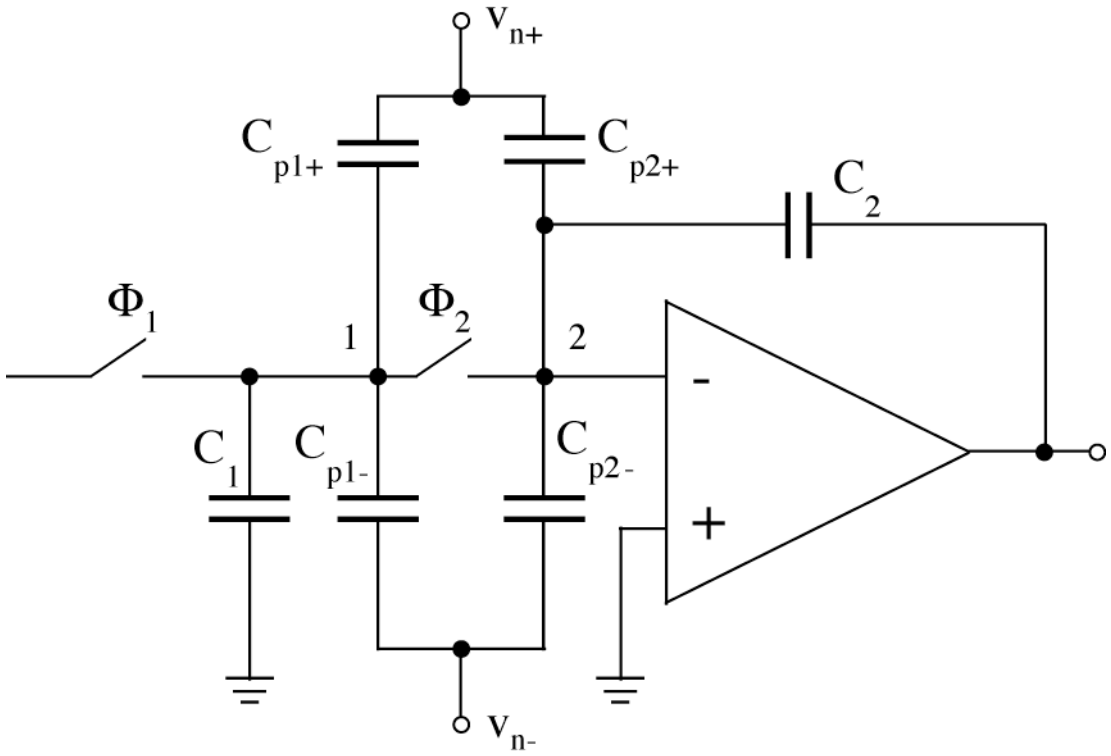
$$v_{o,n,1} = i_{n,Ref}\frac{(W/L)_6}{(W/L)_B}\frac{1}{g_{m5}}$$

# Power supply rejection at low frequency

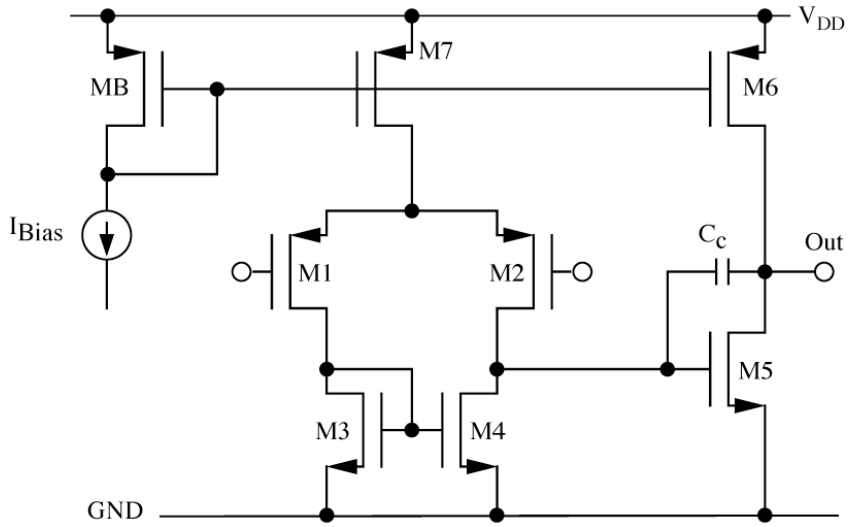



$$\left(v_{o,tot}\right)^2 = \left(\frac{g_{ds6} - \frac{g_{m5}(1-k_+)}{2g_{m3}r_{ds3}}}{g_{ds5}+g_{ds6}}\right)\left(v_n^+\right)^2 + \left(\frac{g_{ds6} - \frac{g_{m5}k_-}{2g_{m3}r_{ds3}}}{g_{ds5}+g_{ds6}}\right)\left(v_n^-\right)^2$$

# Effect of external components on PSRR



# Frequency response and compensation

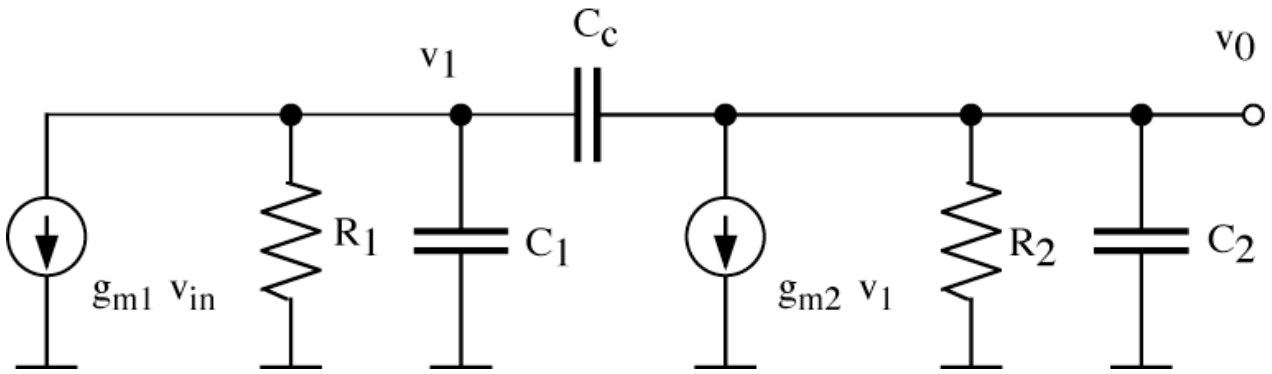



- A two-stage scheme with poles in the same frequency range needs compensation.
- A single pole system is always stable.
- **Strategy**: Approach the single pole performance by splitting the two poles apart.

Miller capacitance moves $p_1$ at lower frequency.

Shunt feedback moves $p_2$ at higher frequency.

Small signal equivalent circuit for two-stage op-amp.




$$\begin{cases} v_1(g_1 + sC_1) + (v_1 - v_0)sC_c + g_{m1}v_{in} = 0 \\ v_0(g_2 + sC_2) + (v_0 - v_1)sC_c + g_{m2}v_1 = 0 \end{cases}$$

$$\frac{v_0}{v_{in}} = g_{m1}R_1R_2 \frac{g_{m2} - sC_c}{1 + sR_1R_2g_{m2}C_c + s^2R_1R_2\left[C_1C_2 + (C_1 + C_2)C_c\right]}$$

The circuit has two poles and a zero in the right half plane.

$$p_1 \approx \frac{-1}{R_1 R_2 g_{m2} C_c} \qquad p_2 \approx \frac{-g_{m2} C_c}{C_1 C_2 + (C_1 + C_2) C_c} \qquad z = \frac{g_{m2}}{C_c}$$

since in practice $C_c > C_1$, $C_c \approx C_2$, $g_{m1} > 1/R_1$, $g_{m2} > 1/R_2$ it results:

$$|p_1| << \frac{1}{R_1 C_1} \qquad |p_2| \approx \frac{g_{m2}}{C_2} >> \frac{1}{R_2 C_2}$$

Assuming $p_1$ as dominant, the unity gain angular frequency is:

$$\omega_T = |p_1| A_0 \approx \frac{1}{R_1 R_2 g_{m2} C_c} g_{m1} g_{m2} R_1 R_2 = \frac{g_{m1}}{C_c}$$

The locations of the second pole $p_2$ and of the zero with respect to $\omega_T$ are derived by considering:

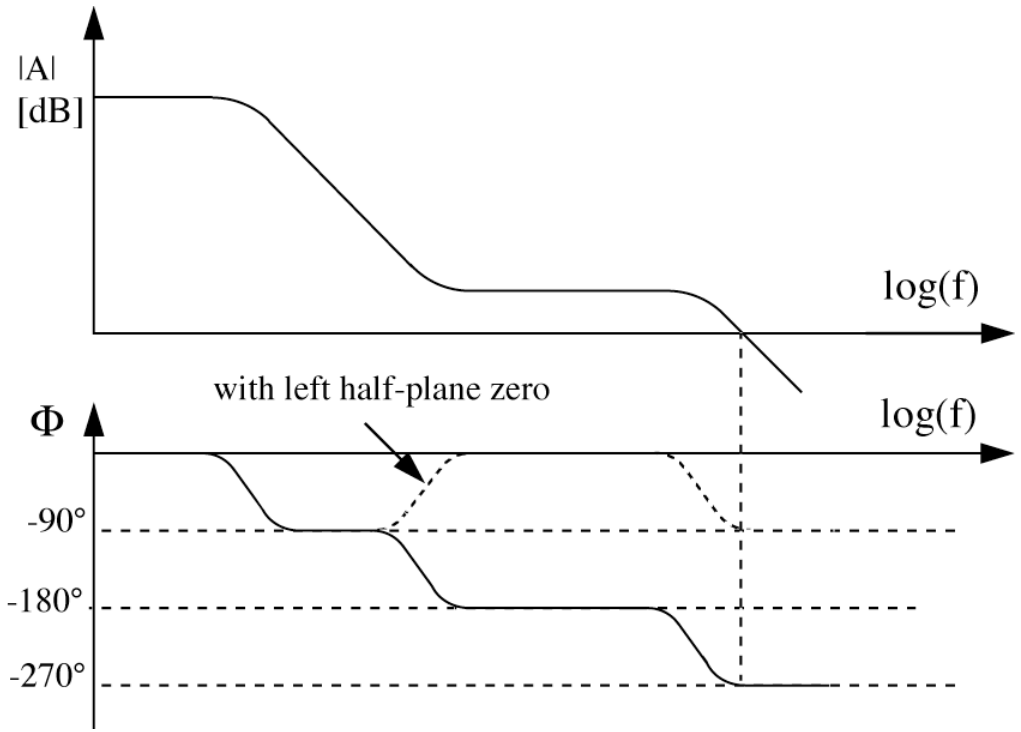
$$\left|\frac{p_2}{\omega_T}\right| = \frac{g_{m2}C_c}{g_{m1}C_2}$$

for stability > 2 to 4

$$\left|\frac{z}{\omega_T}\right| = \frac{g_{m2}}{g_{m1}}$$

The phase shift given by the zero is also negative and can worsen the phase margin. It must be located far from the unity gain frequency.

if $C_c > C_2$ and $g_{m2} > g_{m1}$

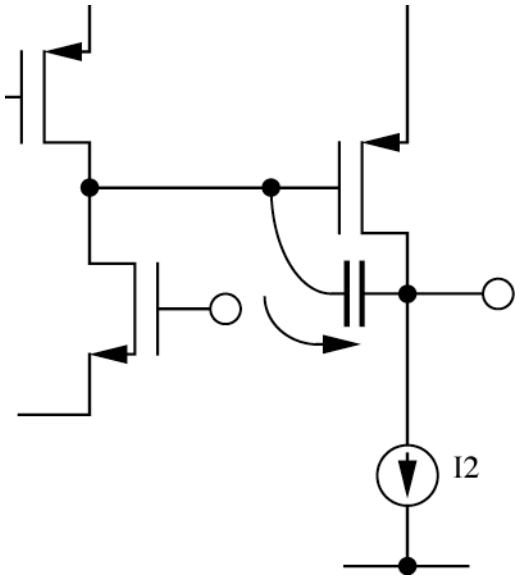



- The right half-plane worsen the phase margin.
- In bipolar technology $g_{m2} >> g_{m1}$ because the current in the second stage is normally higher than the one in the first stage.

- In CMOS technology $g_{m2} \approx g_{m1}$ because they are proportional to the square root of $I$ and $W/L$; moreover, the transconductance of the input pair must be high in order to reduce their thermal noise contribution.
- In real situations the obtainable phase margin does not guarantee stability.

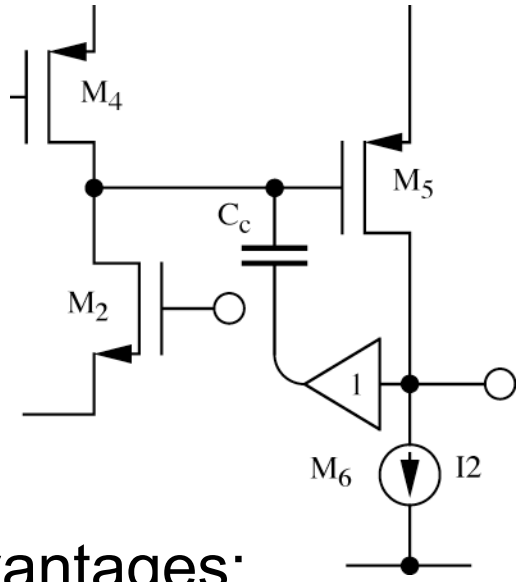
Eliminating the right half-plane zero:

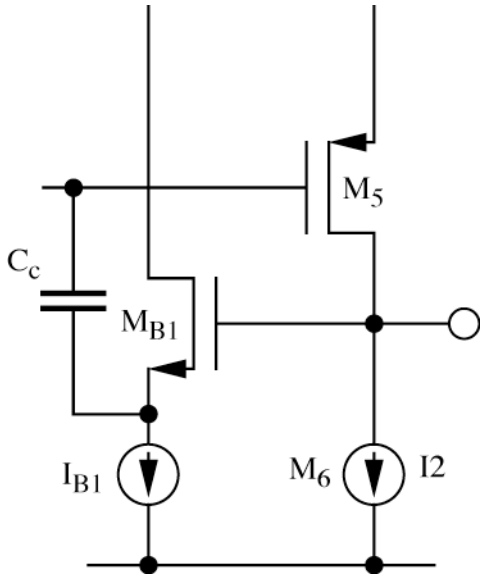
- unity gain buffer
- zero nulling resistor
- unity gain current amplifier




The zero is due to a signal feedforward to a point that is 180° out of phase.

# Solution 1: Eliminate feedforward with source follower

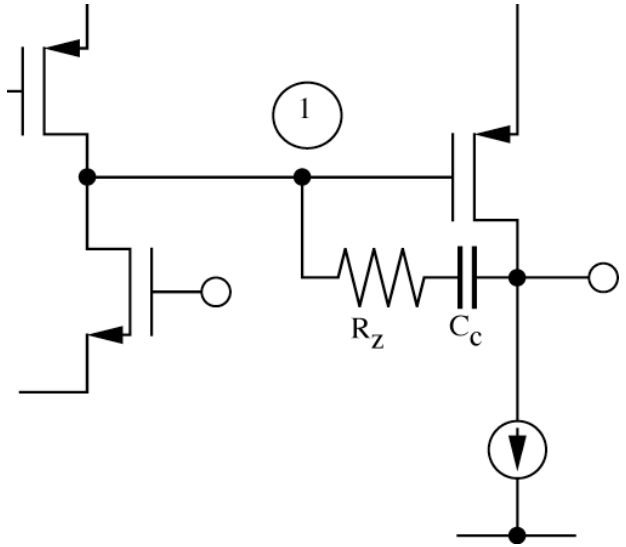



Disadvantages:

- Area
- Power dissipation
- Actually it creates a doublet in the feedback path. Potentially not stable.
- Alternative, a substrate emitter follower may be used. (The bipolar transistor is smaller and has higher $g_m$.)

## Solution 2: Zero nulling resistor




The zero position is pushed away with a resistance in series with $C_c$.

$$\frac{v_0}{v_{in}} \approx A_0 \frac{1+s\left(R_z - 1/g_{m2}\right)C_c}{\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_2}\right)}$$

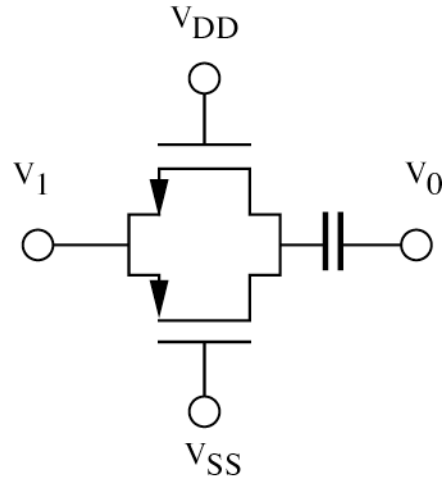
- The pole locations are close to the original.
- The zero is moved depending on $R_z$.

$$z = \frac{1}{\left(1/g_{m2} - R_z\right)C_c}$$

- If $R_z = 1 / g_{m2}$ the zero is moved at infinity
- If $R_z > 1 / g_{m2}$ the zero is located in the left half-plane

Implementation:

$$\frac{1}{R_z} = \frac{1}{R_n} + \frac{1}{R_p}$$



$$\frac{1}{R_n} = k_n'\left(\frac{W}{L}\right)_n \left(V_{DD} - V_1 - V_{Th,n}\right) \qquad \frac{1}{R_p} = k_p'\left(\frac{W}{L}\right)_p \left(V_1 - V_{SS} - V_{Th,p}\right)$$

Choose $(W/L)_n$ and $(W/L)_p$ such that:

$$k_n'\left(\frac{W}{L}\right)_n = k_p'\left(\frac{W}{L}\right)_p$$

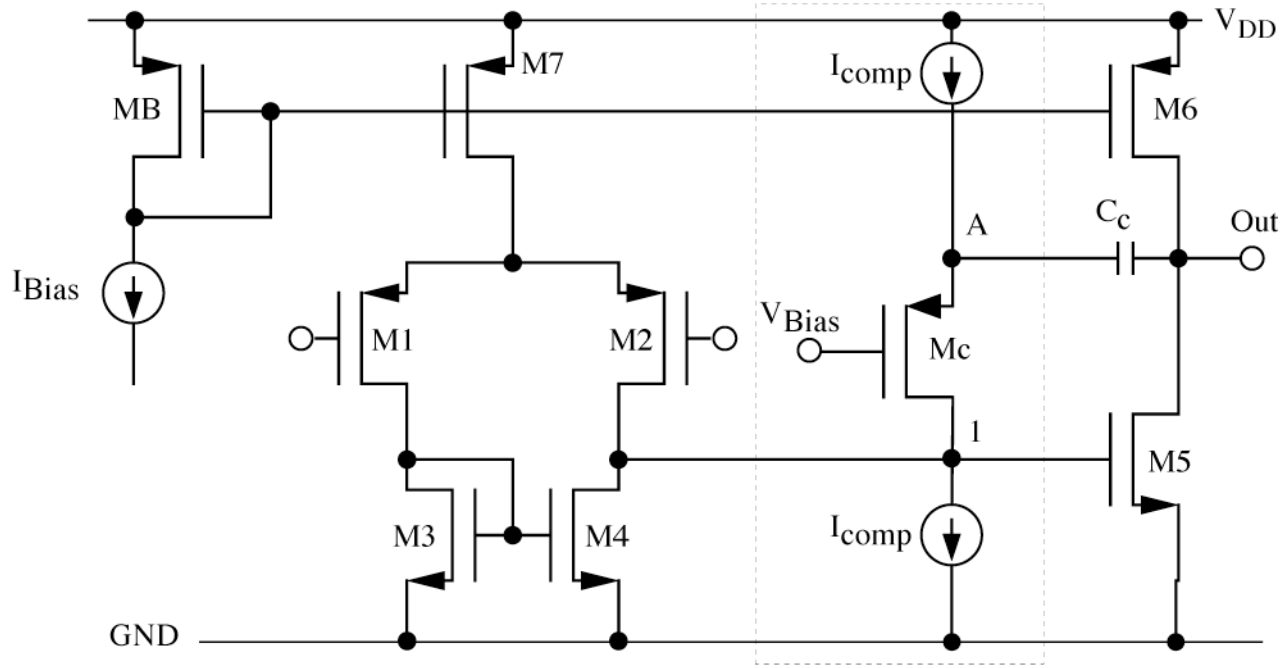
and:

$$\frac{1}{R_z} = k_n'\left(\frac{W}{L}\right)_n \left(V_{DD} - V_{ss} - V_{Th,n} - V_{Th,p}\right)$$

Problem: Supply sensitivity.

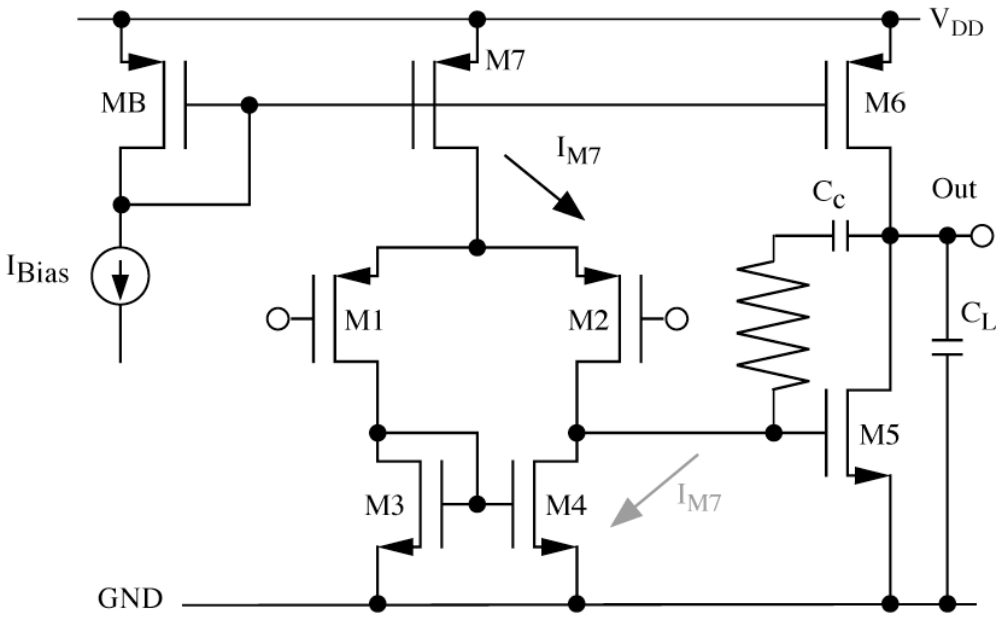
Since the swing of the node 1 is $A_2$ less than the output swing, only one transistor with supply independent bias can be used.

# Solution 3: Unity gain current amplifier




$$\begin{cases} v_1(g_1 + sC_1) + g_{m1}v_{in} - v_0 sC_c = 0 \\ v_0(g_2 + sC_2) + g_{m2}v_1 + v_0 sC_c = 0 \end{cases}$$

# Slew rate




**For large input signal:**

- M1, M4 are off so the current $I_{M7}$ discharges $C_c$ through M2. Assuming M5 able to drive the current request by $C_c$, $C_L$ and $I_{M6}$.

$$SR_- = \left.\frac{\Delta V_-}{\Delta t}\right|_{max} = -\frac{I_{M7}}{C_c}$$

- M2, M5 are off so the current $I_{M7}$ mirrored by M4 charges $C_c$; $C_L$ and $C_c$ are charged by $I_{M6}$. The smaller of these two limits will hold:

$$SR_+ = \left.\frac{\Delta V_+}{\Delta t}\right|_{\max} = \frac{I_{M6}}{C_c + C_L} \qquad SR_+ = \left.\frac{\Delta V_+}{\Delta t}\right|_{\max} = \frac{I_{M7}}{C_c}$$

To have $SR_+ = SR_-$, a condition can be:

$$\frac{I_{M7}}{C_c} = \frac{I_{M6}}{C_c + C_L}$$

Since $\omega_T = g_{m1} / C_c$, the $SR$ is

$$SR = \frac{I_{M7}}{g_{m1}}\omega_T = \left(V_{GS1} - V_{Th}\right)\omega_T$$

For $\omega_T = 2\pi \cdot 40 \cdot 10^6$ rad/s, $(V_{GS1} - V_{Th}) = 300$ mV, $SR \approx$ 75.4 V/μs.

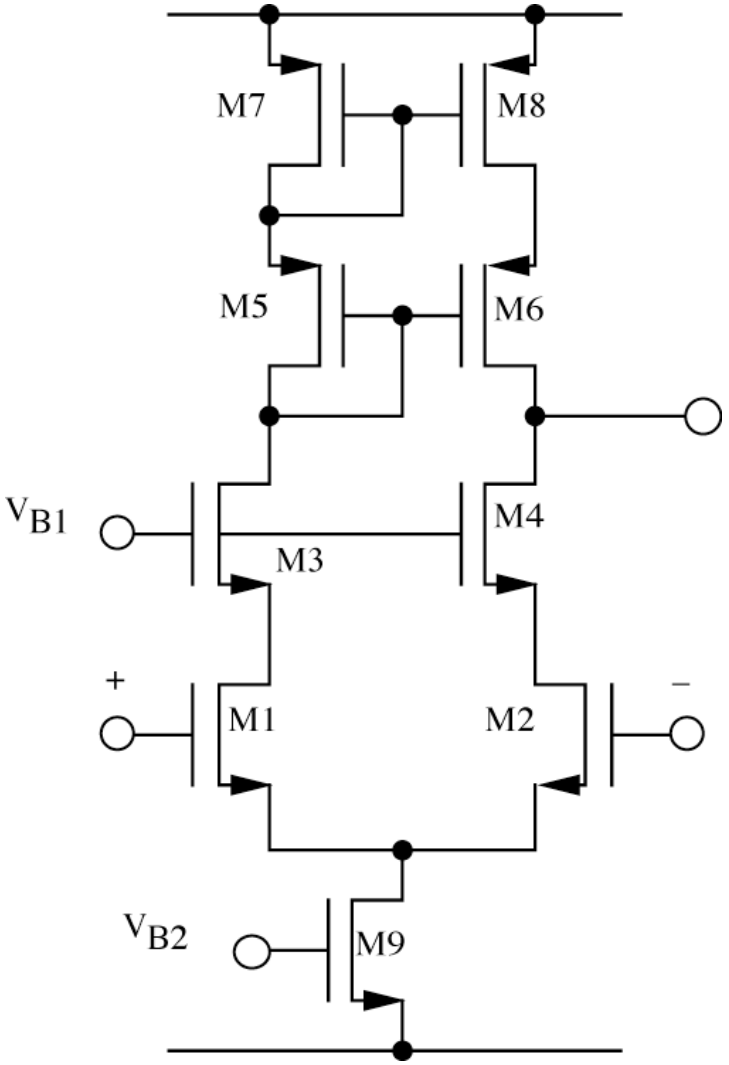
# Single stage schemes

**High gain is get with a cascode scheme.**

- Telescopic cascode
- Mirrored cascode
- Folded cascode

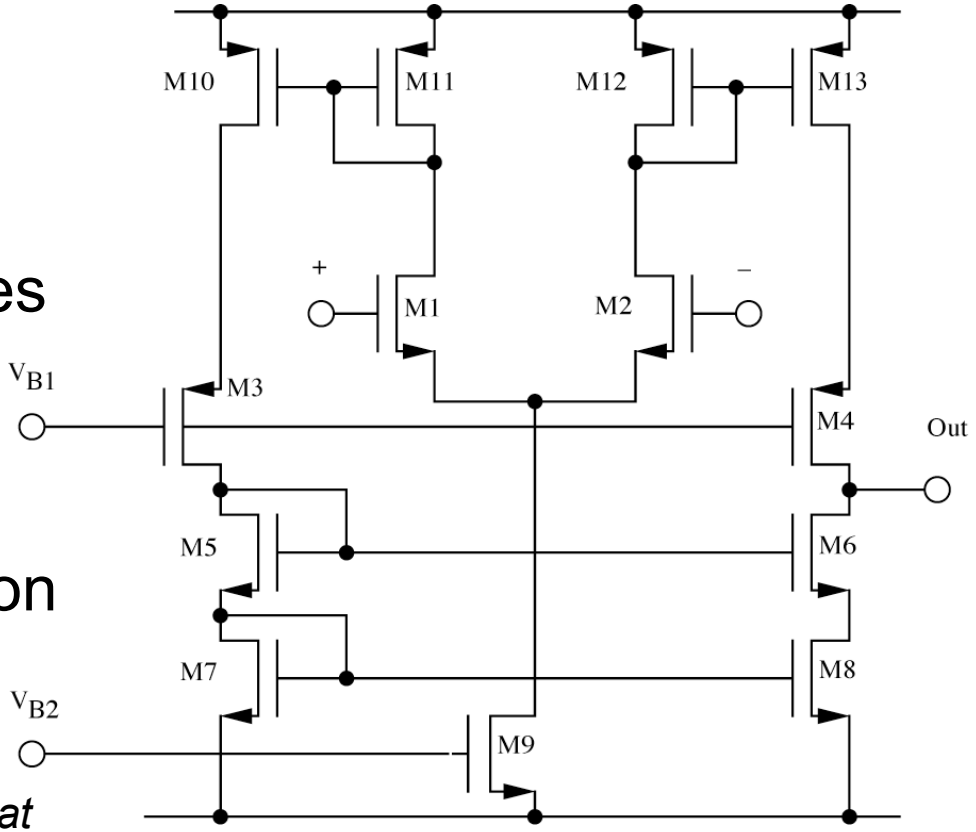
## Telescopic cascode

- DC gain $A_0 \approx (g_m r_{ds})^2$
- low power consumption
- only one high impedance node: compensated with a capacitance load (if necessary)
- low output swing
- reference of the input close to the negative supply
- two bias lines ($V_{B1}$, $V_{B2}$)
- 5 transistors in series



# Mirrored cascode

- optimum input common mode range
- only 4 transistors in series
- improved output swing
- speed of the mirror
- higher power consumption



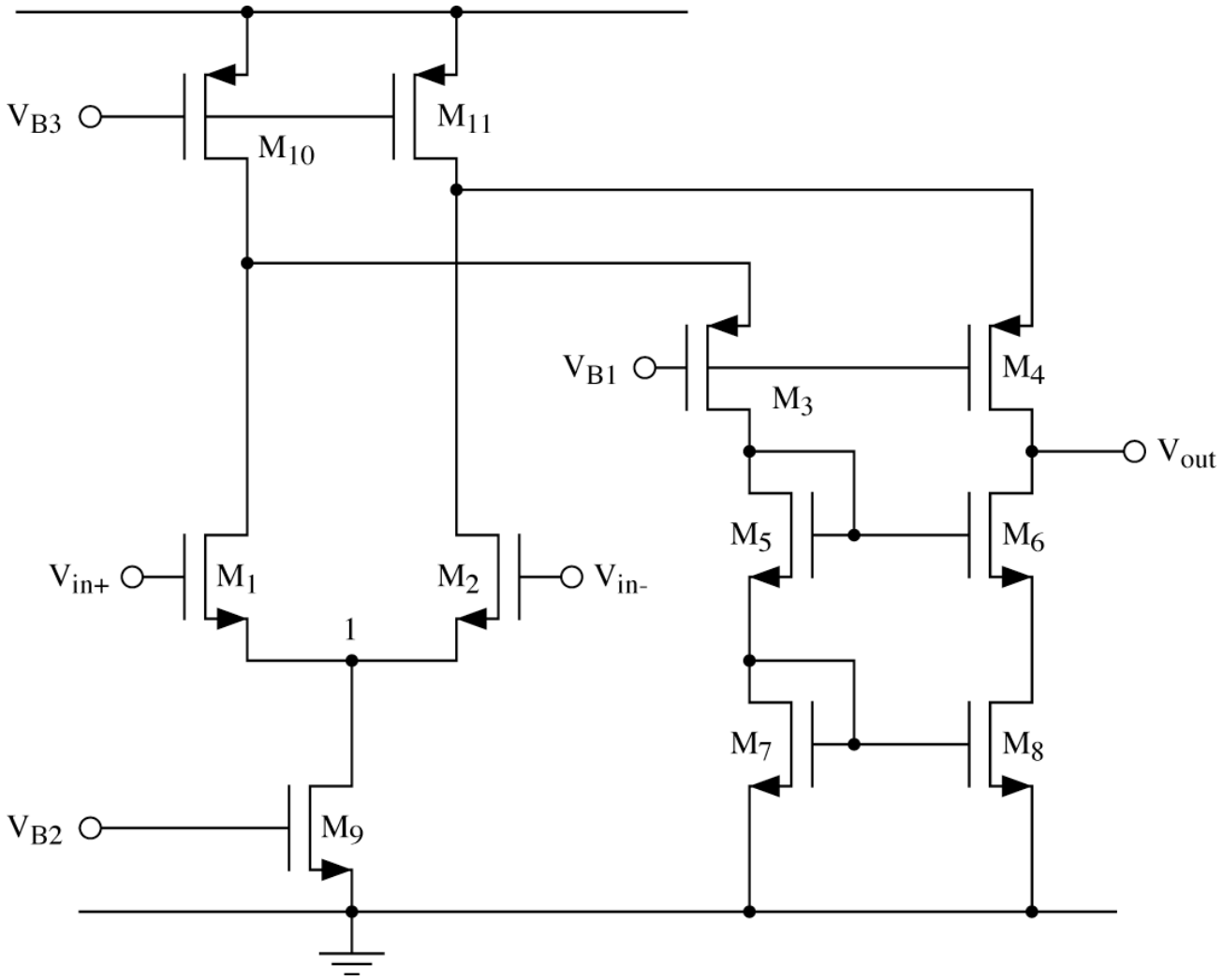

$$V_{outmax} = V_{B1max} + V_{GS4} - V_{sat}$$

$$V_{B1max} = V_{DD} - V_{sat} - V_{GS4}$$

$$V_{outmax} = V_{DD} - 2V_{sat}$$

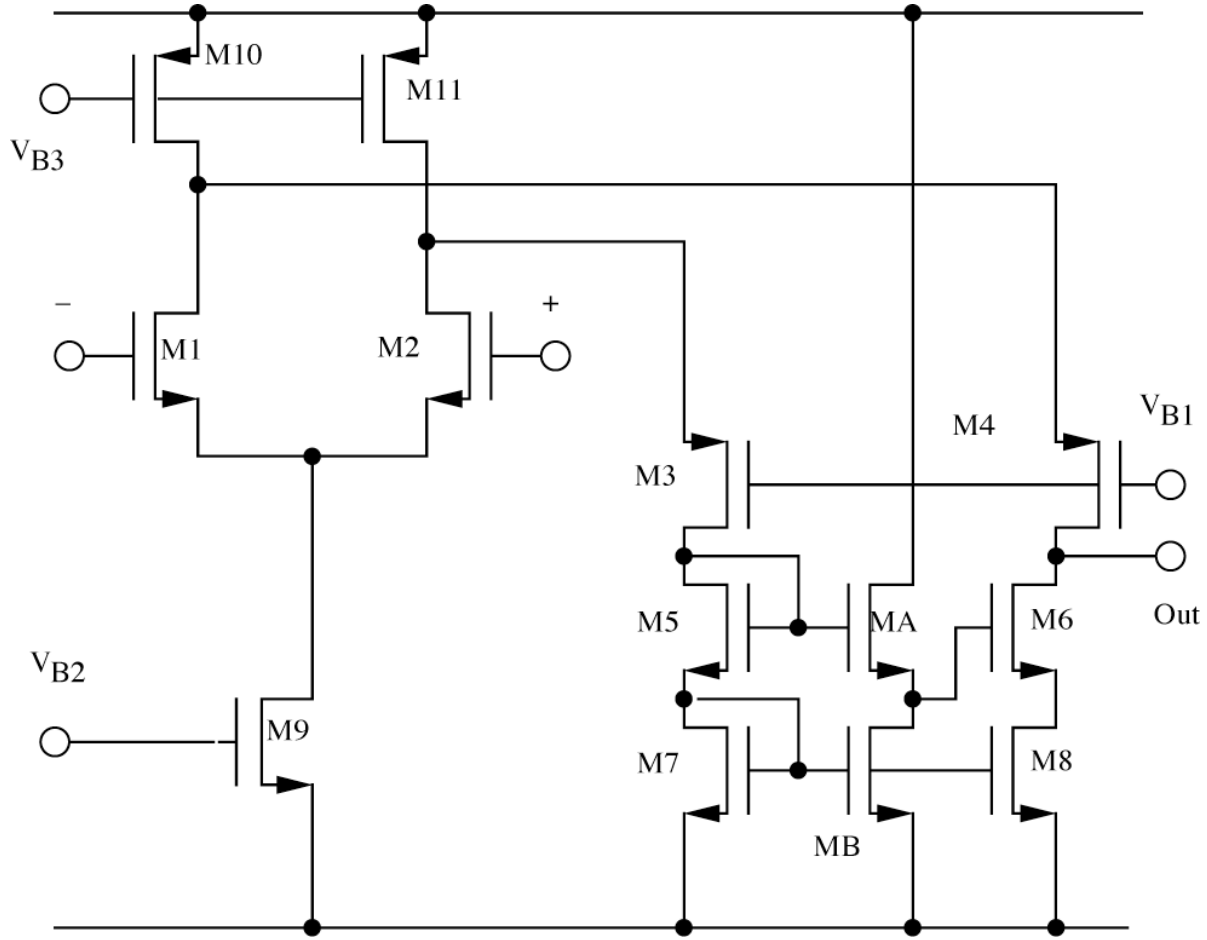
$$V_{outmax} = V_{GS7} + V_{sat}$$

# Conventional folded cascode



# Modified folded cascode

(improved output swing)



## Two stage amplifier vs. single stage amplifier

**Two stages:**

- ➔ Voltage gain less affected by resistive loading
- ➔ Maximum signal swing
- ➔ Less bussing of bias lines
- ➔ Requires an additional capacitor for frequency compensation
- ➔ More power consumption

**Single stage:**

- ➔ No need for additional compensation capacitor
- ➔ Lower power consumption
- ➔ Better CMRR
- ➔ Lower signal swing
- ➔ More bussing of bias lines

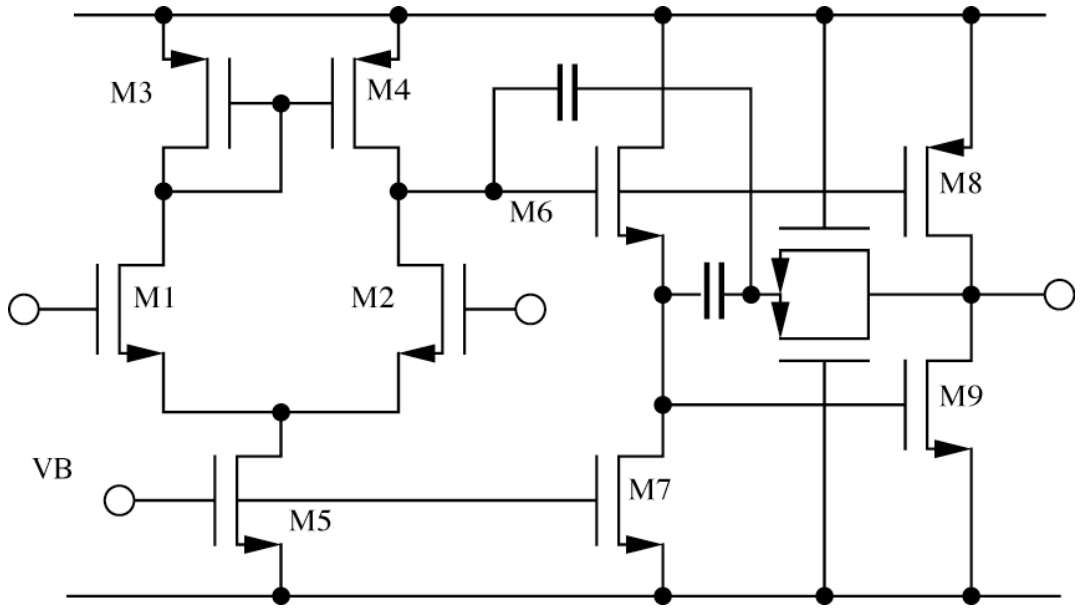
# Class AB op-amps

Class AB: a circuit which can have an output current which is larger than its DC quiescent current.

Two stages amplifier with class AB second stage

M6 and M7 act as a level shifter

M8 and M9 act as a class AB push-pull amplifier




$$A_2 = \frac{g_{m8} + g_{m9}}{g_{ds8} + g_{ds9}}$$

The quiescent current in the output stage is bias voltage and technological variation dependent.

$$V_{DD} = V_{GS8} + V_{GS6} + V_{GS9}$$

neglecting the body effect:

$$V_{DD} = V_{Th,p} + 2V_{Th,n} + \sqrt{\frac{2}{k_n'}\left(\frac{L}{W}\right)_6 I_6} + \sqrt{\frac{2}{k_n'}\left(\frac{L}{W}\right)_8 I_8} + \sqrt{\frac{2}{k_n'}\left(\frac{L}{W}\right)_9 I_9}$$

$$\sqrt{I_9} = \frac{V_{DD} - V_{Th,p} - 2V_{Th,n} - \sqrt{\frac{2}{k_n'}\left(\frac{L}{W}\right)_6 I_6}}{\sqrt{\frac{2}{k_n'}\left(\frac{L}{W}\right)_8} + \sqrt{\frac{2}{k_n'}\left(\frac{L}{W}\right)_9}}$$

Typically with $V_{DD}$ = 5 V the numerator is around 1.6 V; if it is assumed $V_{DD}$ = (5 ± 0.5) V and $\Delta V_{Th}$ = ± 200 mV, it results that the numerator can change from 0.7 V to 2.5 V; hence, $I_{min} = 0.3\ I_{nom}$; $I_{max} = 2.5\ I_{nom}$

# Single stage class AB amplifier (only inverting)

In the input pair M1 and M2 operate as source followers and drive the common gate stage M3 and M4.

$V_B = V_{Th,n} + V_{Th,p} + V_{ov,n} + V_{ov,p}$

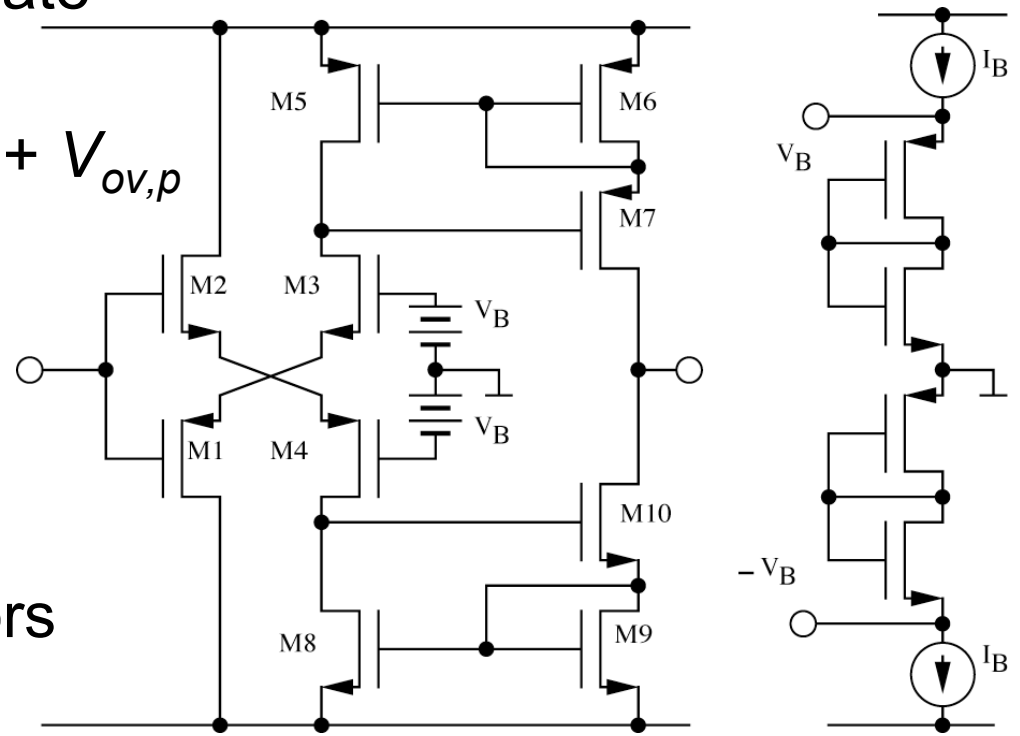
for $V_{in} = 0$

$I_1 = I_2 = I_{Bias}$

for $V_{in} > 0$

$I_{out} = K_{8,9}\, I_1 - K_{5,6}\, I_2$

$K_{8,9}$ and $K_{5,6}$ mirror factors (assumed equal)



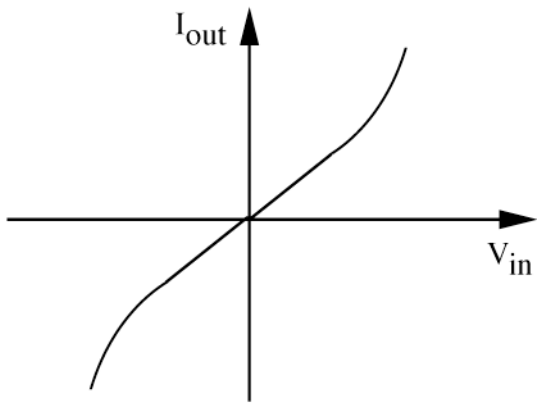
$$V_B + V_{in} = V_{GS2} + V_{GS4} = V_{Th,n} + V_{Th,p} + \left( \sqrt{\frac{2}{k_n'} \left( \frac{W}{L} \right)_2} + \sqrt{\frac{2}{k_p'} \left( \frac{W}{L} \right)_4} \right) \sqrt{I_2}$$

$$V_B - V_{in} = V_{GS1} + V_{GS3} = V_{Th,n} + V_{Th,p} + \left( \sqrt{\frac{2}{k_n'} \left( \frac{W}{L} \right)_3} + \sqrt{\frac{2}{k_p'} \left( \frac{W}{L} \right)_1} \right) \sqrt{I_1}$$

It results:

$I_{out} = K_{8,9} (I_1 - I_2) = \alpha K_{8,9} V_B V_{in}$

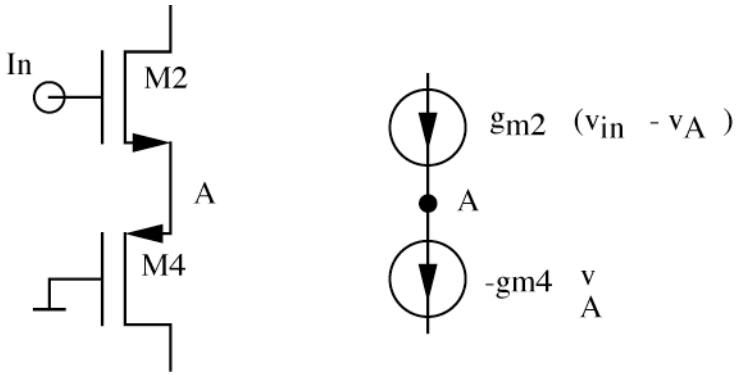
Until $I_1$ or $I_2$ goes to zero, for a larger $V_{in}$, $I_{out}$ increases quadratically with $V_{in}$.




**Small signal gain:**

$A_v = 2 G_m r_{out}$

$G_m$ is the transconductance of the cross coupled input stage




$$g_{m2}\left(V_{in} - V_A\right) = g_{m4}V_A$$

$$V_A = \frac{g_{m2}V_{in}}{g_{m2} + g_{m4}}$$

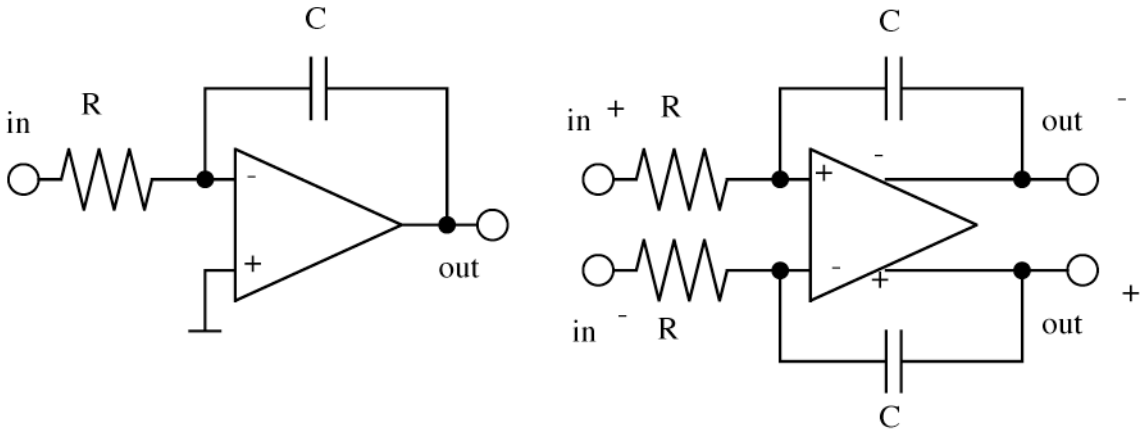
$$I_{out} = g_{m4}V_A = \frac{g_{m2}g_{m4}}{g_{m2} + g_{m4}}V_{in} = G_m V_{in}$$

# Fully differential op-amps

The use of fully differential paths in analog signal processing gives benefits on:

- PSRR
- dynamic range
- clock feedthrough cancellation

Consider an integrator and its fully differential version:

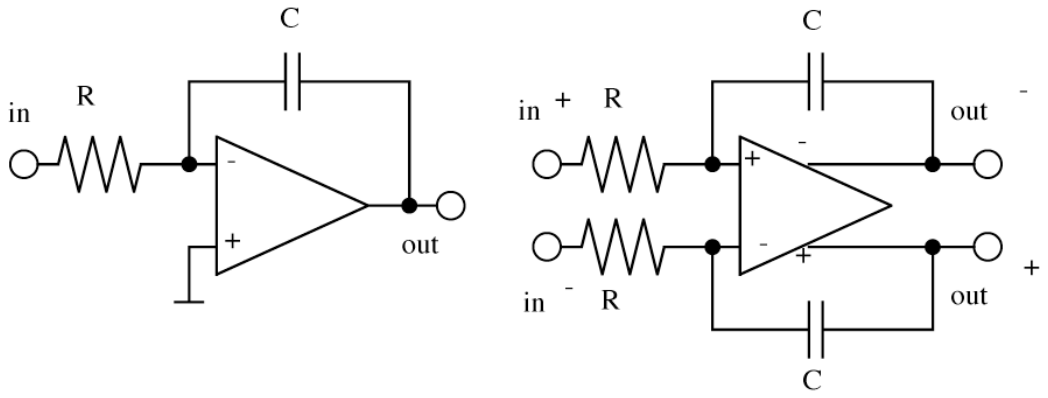


- Noise from the power supply and clock feedthrough are common mode signals.
- The output swing is doubled ($V_{max+} - V_{max-} = 2\ V_{max}$). Since the noise is unchanged, the dynamic range improves by 6 dB.

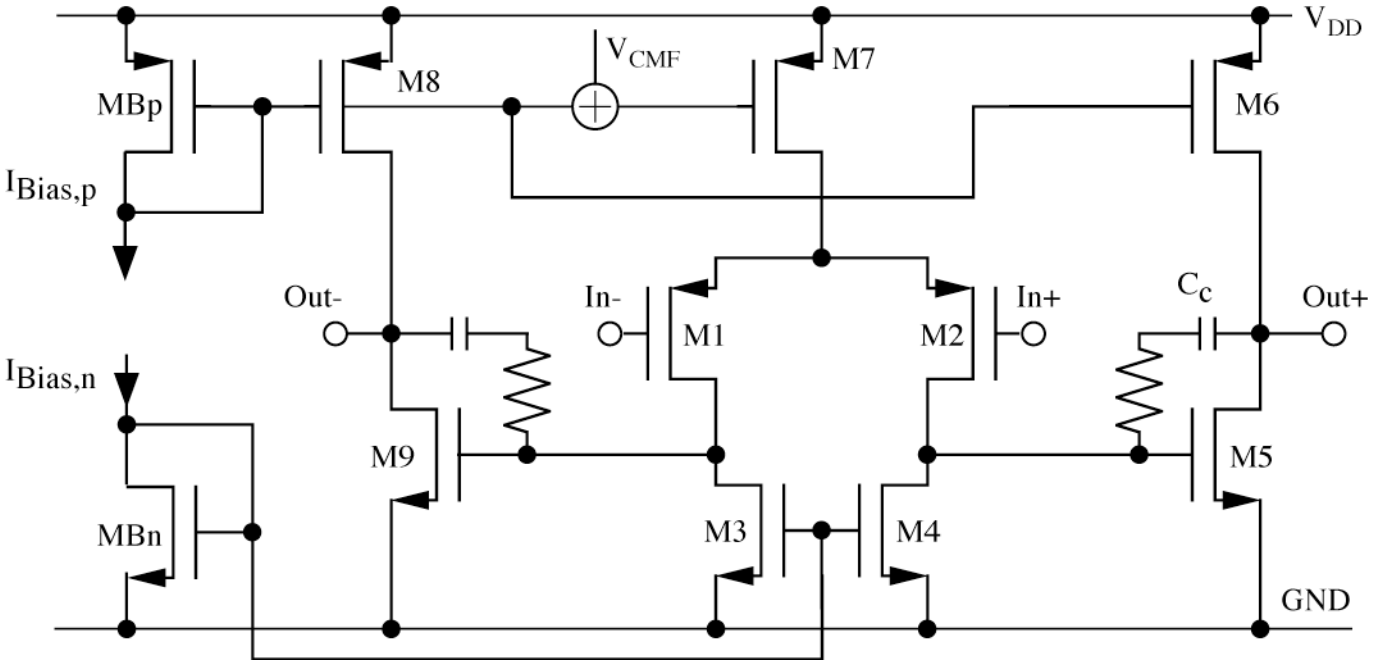
- Single ended to differential and double ended to single ended converters are necessary
- Larger area
- More bussing of bias lines
- Common mode feedback is necessary

The SE/DE and DE/SE blocks increase the complexity and introduce noise. The differential approach is convenient if the differential processor contains more than 4 stages.


The feedback around the op-amp control the difference of the input terminal voltages and not their mean value. In turn, there is no control on the output common mode voltage.



# Fully differential two stage OTA



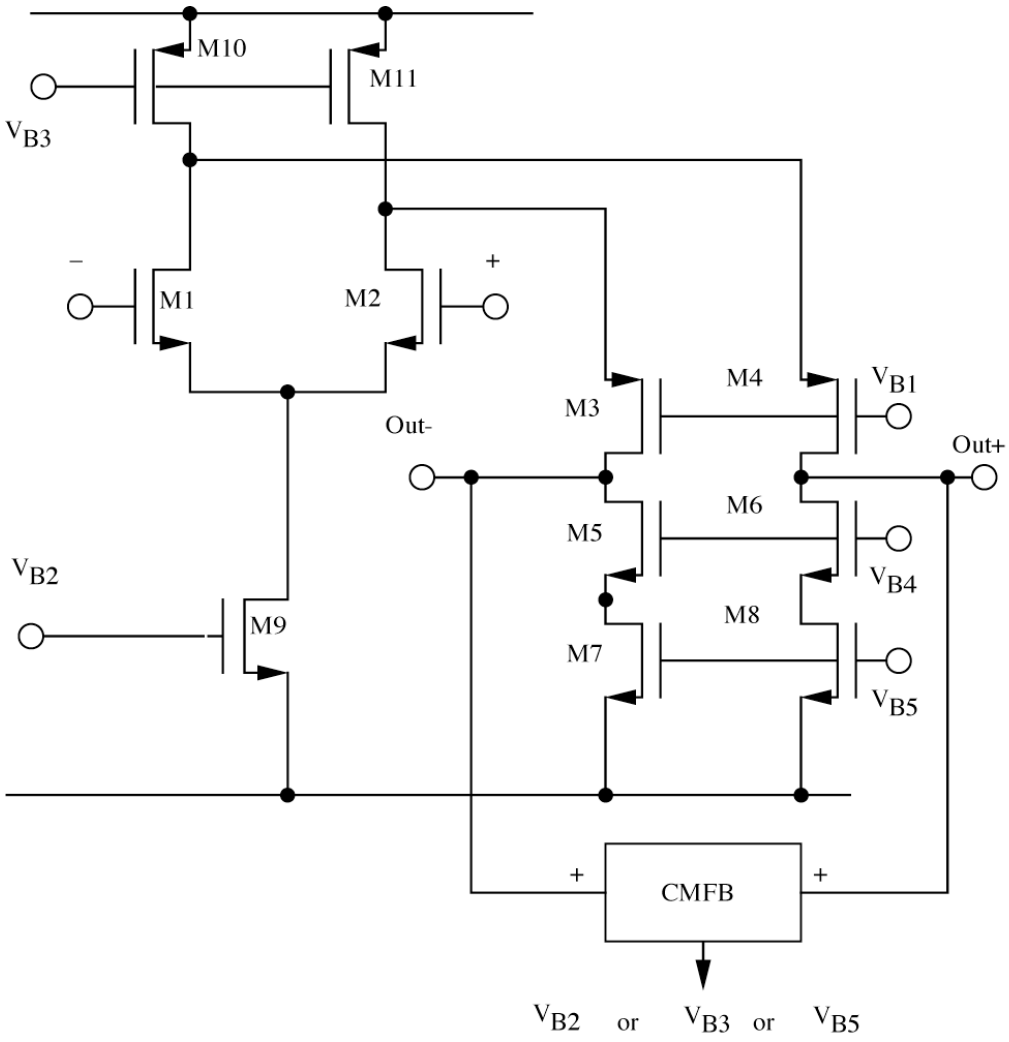

1st stage with gain:

$$\left|A_1\right| = \frac{1}{2}\frac{g_{m1}}{g_{ds1} + g_{ds4}}$$

two 2nd stages with gain:

$$\left|A_2\right| = \frac{g_{m5}}{g_{ds5} + g_{ds6}}$$

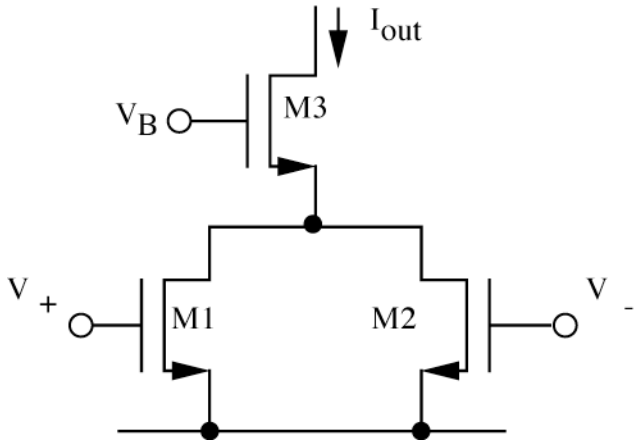
# Fully differential single stage OTA



# COMMON MODE FEEDBACK

- continuous time
- sampled data

## Continuous-time common mode feedback



$V_B$ is such that M1 and M2 are in the linear region; $(W/L)_1 = (W/L)_2$; M1 and M2 are like the parallel of two voltage dependent resistances.

$$I_1 = \mu C_{ox}\left(\frac{W}{L}\right)_1\left[\left(V_+ - V_{Th}\right)V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

$$I_2 = \mu C_{ox}\left(\frac{W}{L}\right)_2\left[\left(V_- - V_{Th}\right)V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

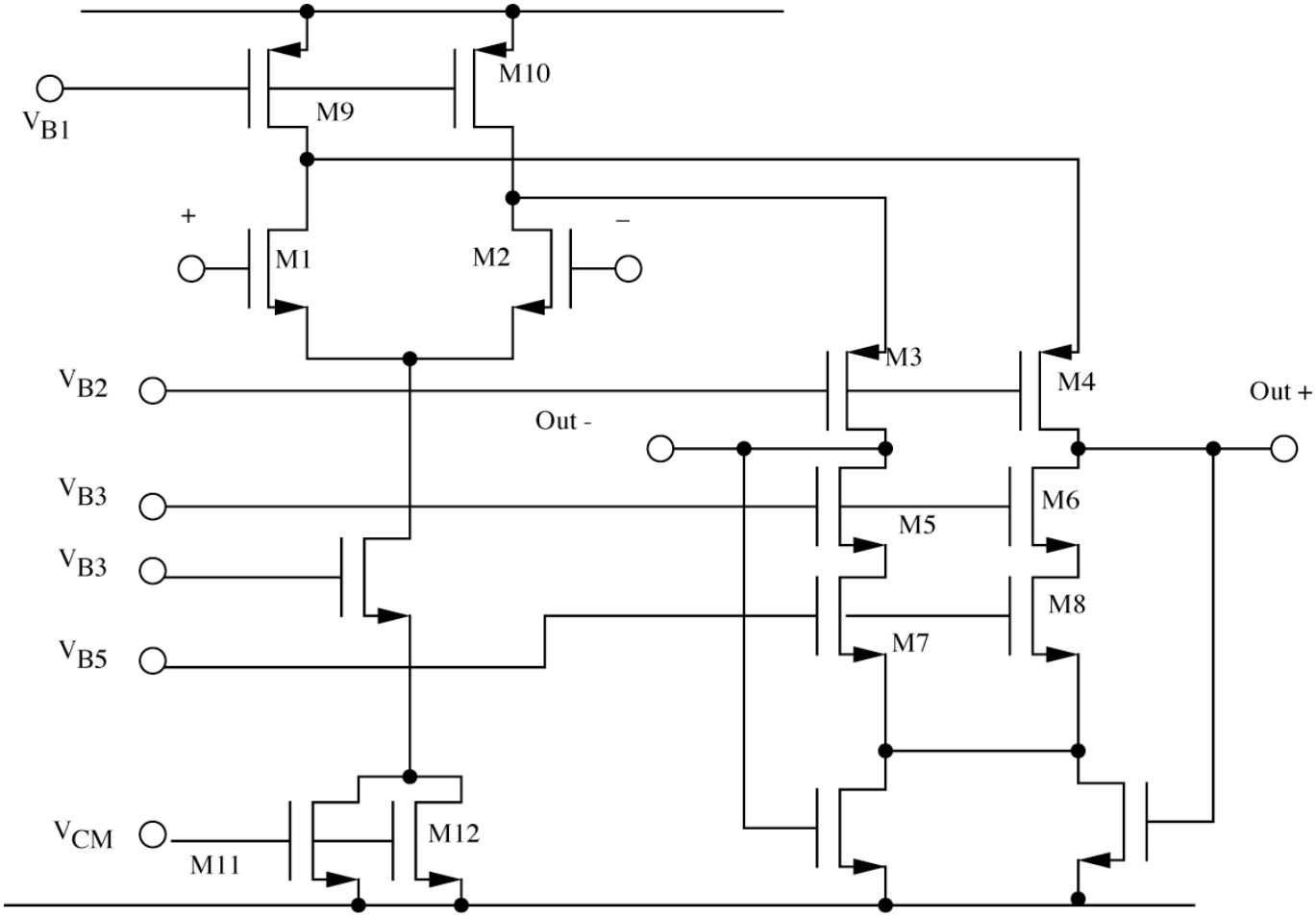
$$I_{out} = I_1 + I_2 = \frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)_3\left(V_B - V_{DS} - V_{Th}\right)^2$$

With a differential signal $I_{out}$ = cost

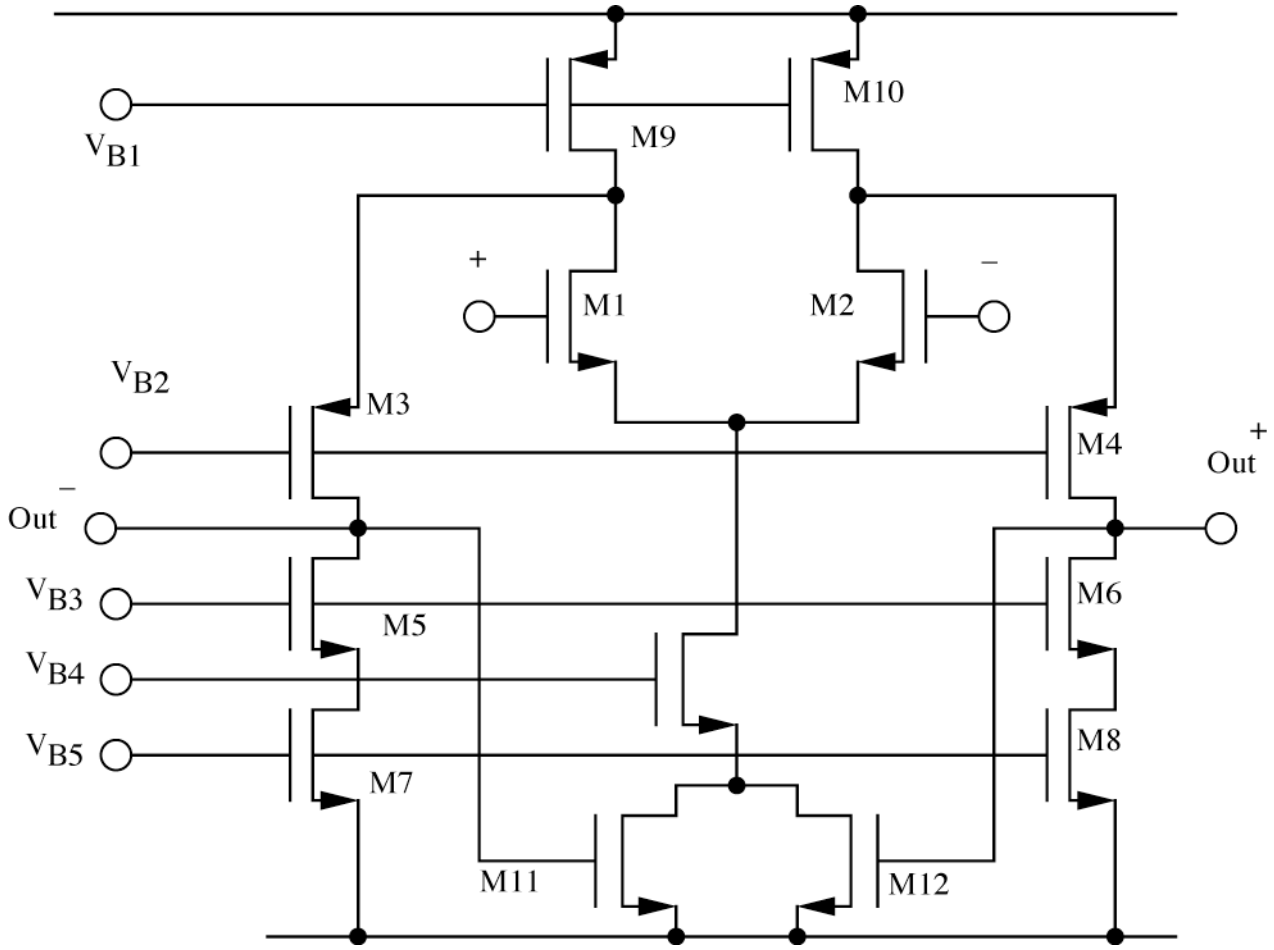
With a common mode signal: if positive, $I_{out}$ increases

if negative, $I_{out}$ decreases

# Fully differential folded cascode with CMFB



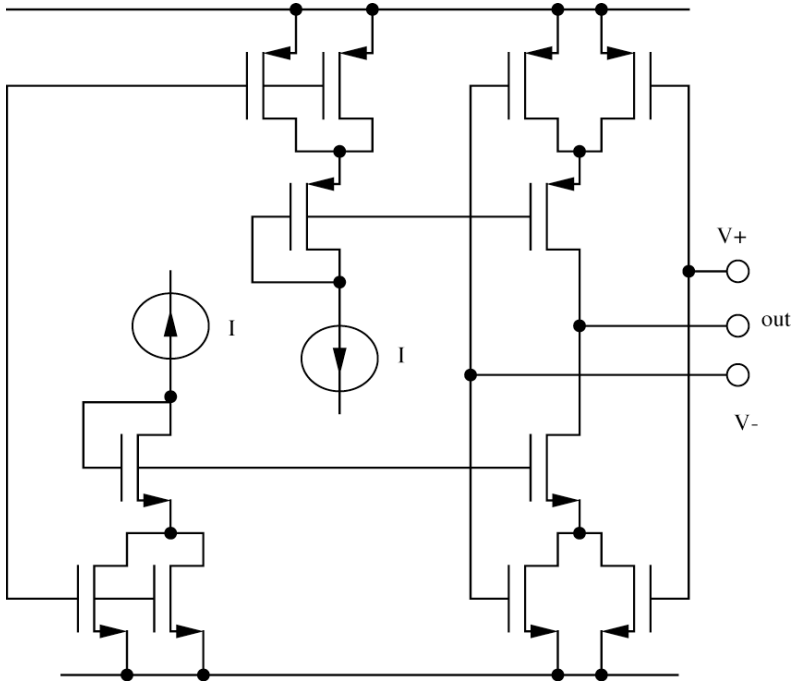
# Fully differential folded cascode with CMFB (2)



**Problems:**

- dynamic range
- linearity

Compensation of the non-linearities of the n-channel and p-channel CMFB cell.

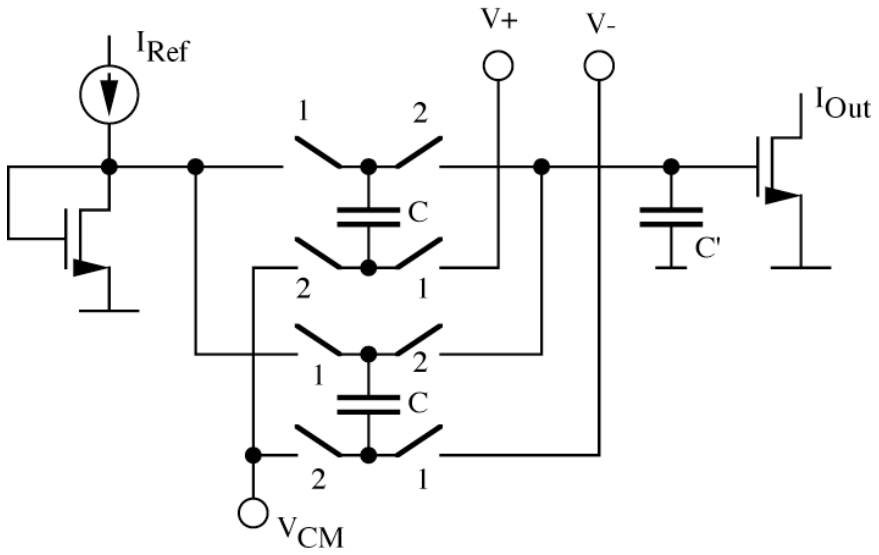


## Sampled-data common mode feedback

The common mode feedback operates on slowly variable signal. It can be implemented at discrete time intervals.

The sampled data feedback is essential for low bias voltage and low power.

- linearity (mean value with capacitors)
- low power consumption
- no limitation to the dynamic range
- clock signal necessary
- clock feedthrough effect



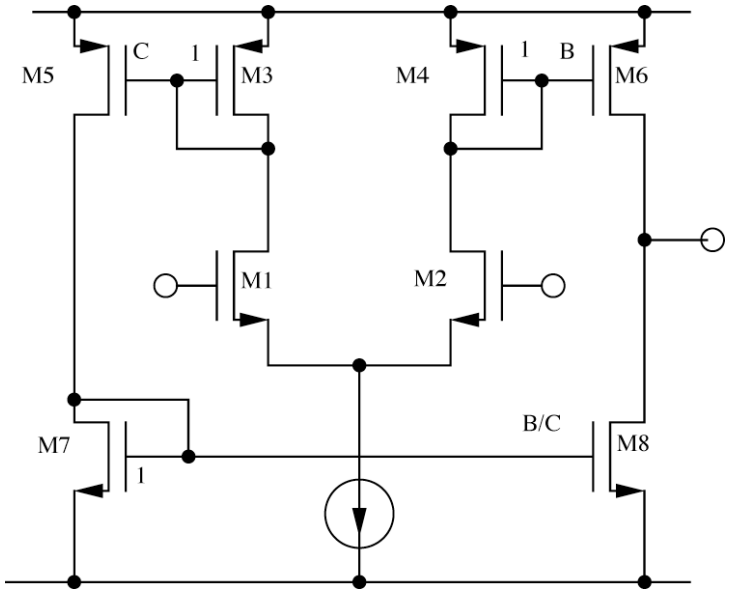
# Micro-power op-amps

- Required in battery operated systems
  (portable/wearable equipment: pocket calculators, PDA's, digital cameras, …; medical equipment: pace makers, hearing aids, …);
- Use of MOS transistors in **weak inversion**;
- Low current (< 10 μA) → low slew rate.

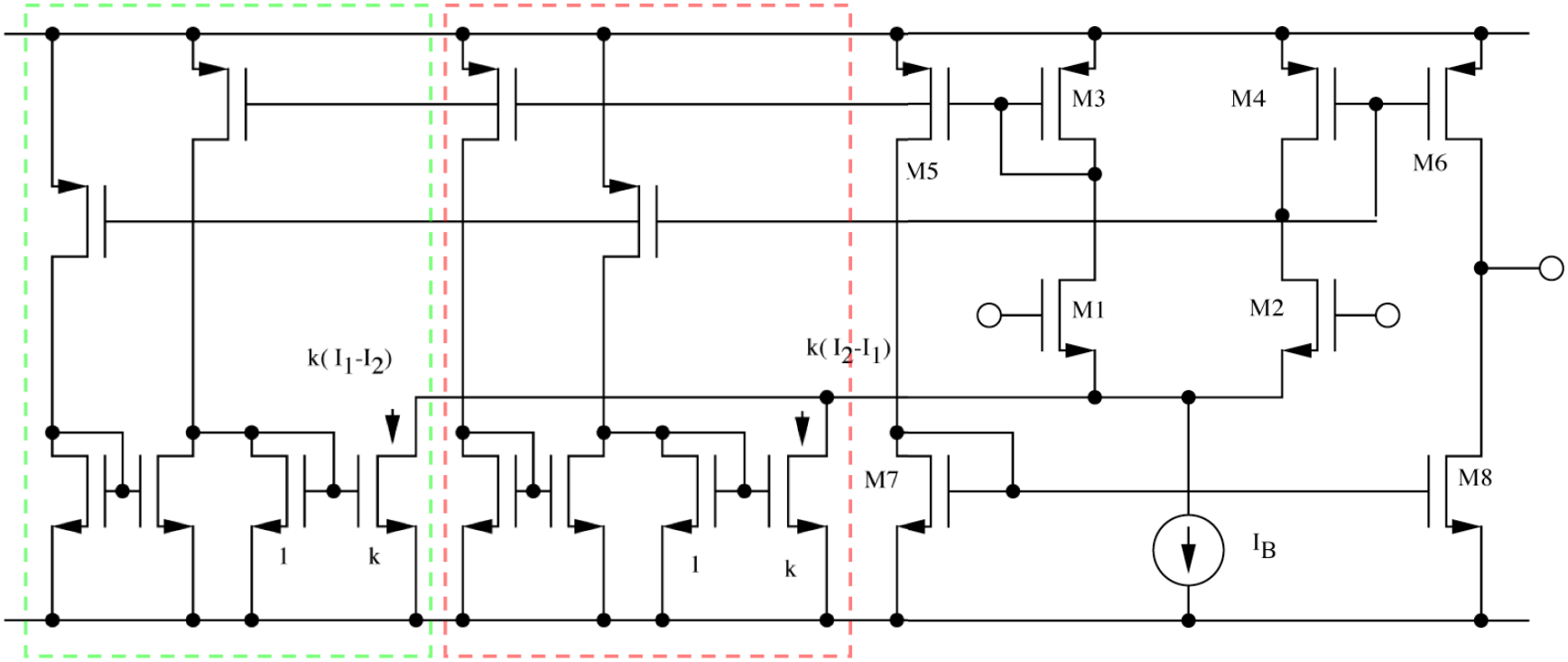
$$g_m = \frac{I_D}{nV_T} \qquad g_{ds} = \lambda I_D$$

$$\left|A_v\right| = \frac{B\, g_{m1}}{g_{ds6} + g_{ds8}} = \frac{B}{nV_T\left(\lambda_n + \lambda_p\right)}$$

high dc gain ($A_v \approx 60$ dB)



# Dynamic biasing of the tail current




**Basic idea:**

Generate $|I_1 - I_2|$ and increase the current in the differential stage by $k|I_1 - I_2|$.

Since

$$i_1 - i_2 = g_m(v_{in+} - v_{in-}) \qquad g_m = \frac{I_D}{nV_T} \qquad I_D = I_B + k\left|i_1 - i_2\right|$$

$$\left|i_1 - i_2\right| = \left(I_B + k\left|i_1 - i_2\right|\right)\frac{\left|v_{in+} - v_{in-}\right|}{nV_T}$$

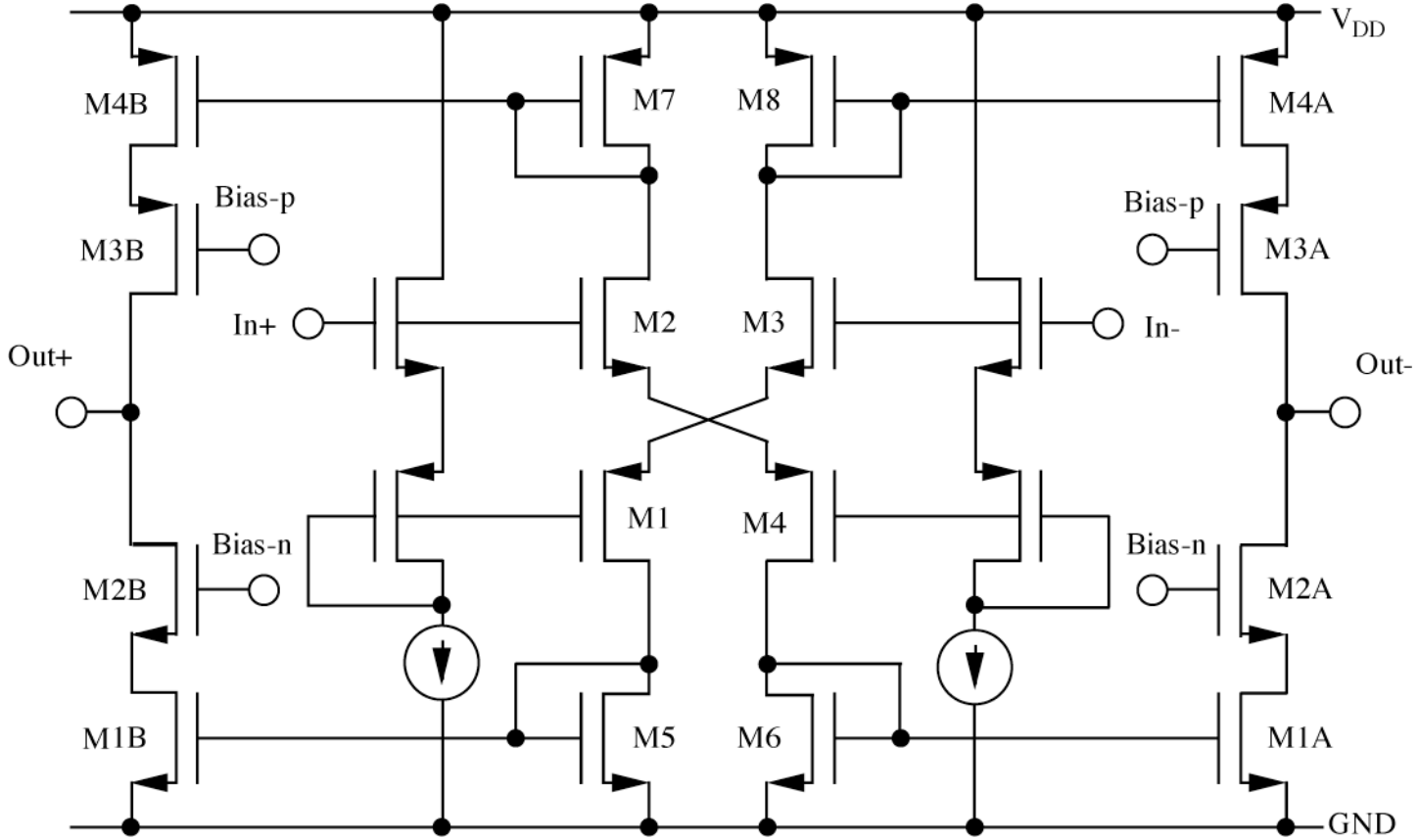
The current increase becomes significant when:

$$k\frac{\left|v_{in+} - v_{in-}\right|}{nV_T} > 1$$

Typical performance:

| | |
|---|---|
| DC gain | 95 dB |
| $f_t$ | 130 kHz |
| SR | 0.1 V/μs |
| $I_B$ | 0.5 μA |
| $I_{tot}$ | 2.5 μA |

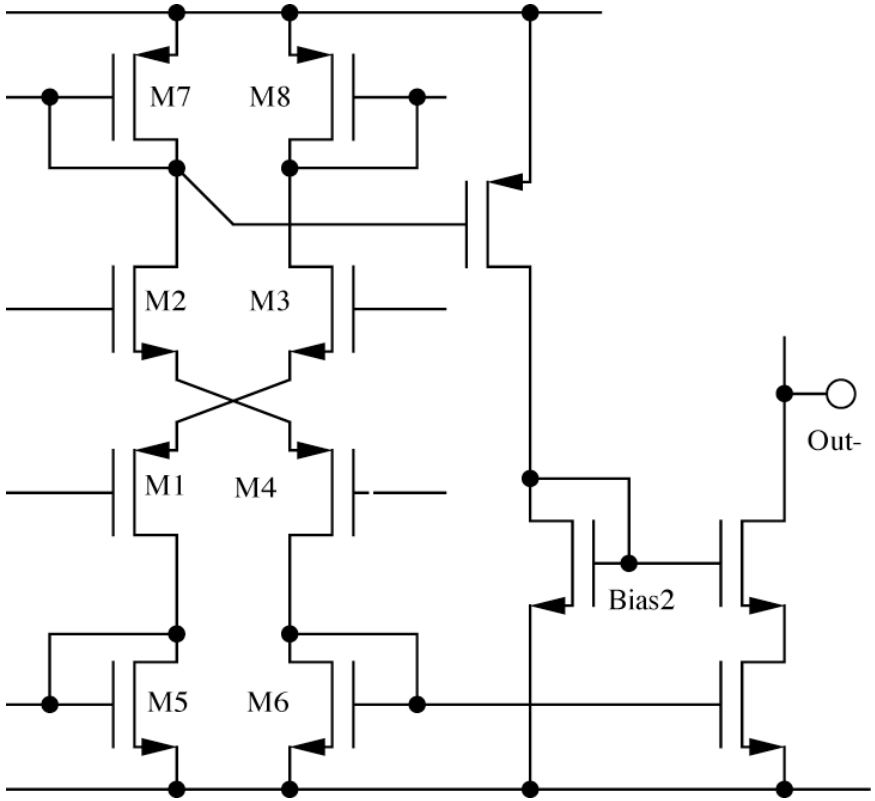
# Class AB single stage with dynamic biasing




For maximum output swing $V_{BIAS\text{-}p}$ and $V_{BIAS\text{-}n}$ must be as close as possible to the supply voltages.

During the slewing the current source of the output cascodes can be pushed in the linear region, hence loosing the advantage of the AB operation.

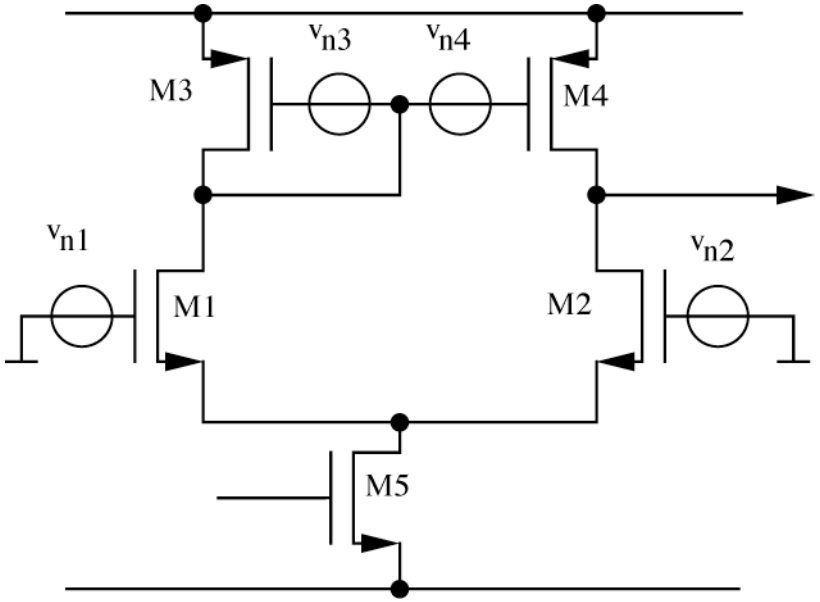
The problem is solved with the dynamic biasing:



# Noise

- The noise of an operational amplifier is described with an input referred voltage source $v_n$.
- The spectrum of $v_n$ is made of a white term and 1/*f* term.
- $v_n$ is due to the contributions, referred to the input, of the noise generators associated to all the transistors of the circuit (assumed uncorrelated).

Consider the input stage of a two stage op-amp.




The output noise voltage is given by:

$$v_{n,out}^2 = \left[g_{m1}^2(v_{n1}^2 + v_{n2}^2) + g_{m3}^2(v_{n3}^2 + v_{n4}^2)\right]\left(\frac{1}{g_{ds2} + g_{ds4}}\right)^2$$

We assume $g_{m1} = g_{m2}$; $g_{m3} = g_{m4}$ (we assume the noise source of M5 does not contribute) moreover since usually $W_1 = W_2$; $L_1 = L_2$; $W_3 = W_4$; $L_3 = L_4$; $v^2_{n1} = v^2_{n2}$; $v^2_{n3} = v^2_{n4}$; if we refer $v^2_{n,out}$ to the input, we get:

$$\frac{v^2_{n,out}}{A_1^2} = v^2_{n,in} = \frac{v^2_{n,out}}{g^2_{m1}}\left(g_{ds2} + g_{ds4}\right)^2 = 2\left(v^2_{n1} + \frac{g^2_{m3}}{g^2_{m1}} v^2_{n3}\right)$$

The contribution of the active loads is reduced by the square of the ratio $g_{m3}/g_{m1}$

It is worth to remember that

$$g_m = \sqrt{2\mu C_{ox} \frac{W}{L} I} \qquad v^2_n = \left(\frac{8kT}{3g_m} + \frac{K_F}{2\mu C_{ox}} \frac{1}{WL} \frac{1}{f}\right)\Delta f$$

The attenuation by the factor $(g_{m3}/g_{m1})^2$ gives, for the white term:

$$v_{n,in,w}^2 = 2v_{n1}^2\left(1+\frac{g_{m3}}{g_{m1}}\right) = 2v_{n1}^2\left(1+\sqrt{\frac{\mu_3\left(W/L\right)_3}{\mu_1\left(W/L\right)_1}}\right)$$

and for the 1/*f* term:

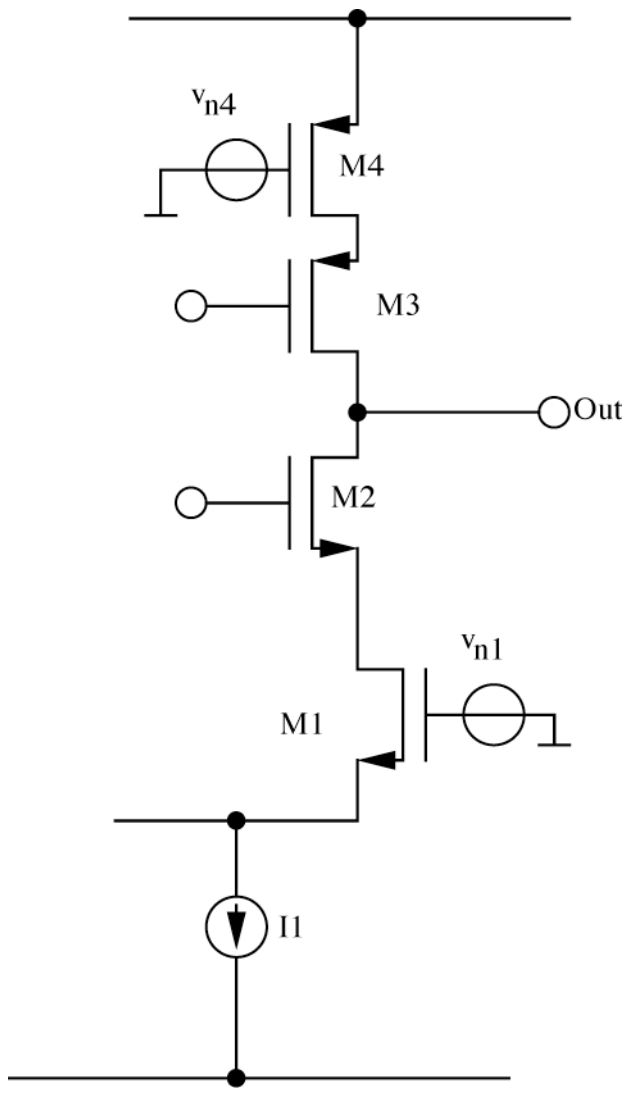
$$v_{n,in,1/f}^2 = 2\frac{K_{F1}}{\mu_1 C_{ox} W_1 L_1}\frac{1}{f}\left(1+\frac{K_{F3}L_1^2}{K_{F1}L_3^2}\right)$$

Where $K_{F1}$ and $K_{F3}$ are the flicker noise coefficient for transistors M1 and M3. The white contribution of the active load is reduced by choosing $(W/L)_{input} >> (W/L)_{load}$. The 1/*f* noise contribution of the active load is reduced by choosing $L_{input} < L_{load}$. If the above conditions are satisfied the input noise is dominated by the input pair.

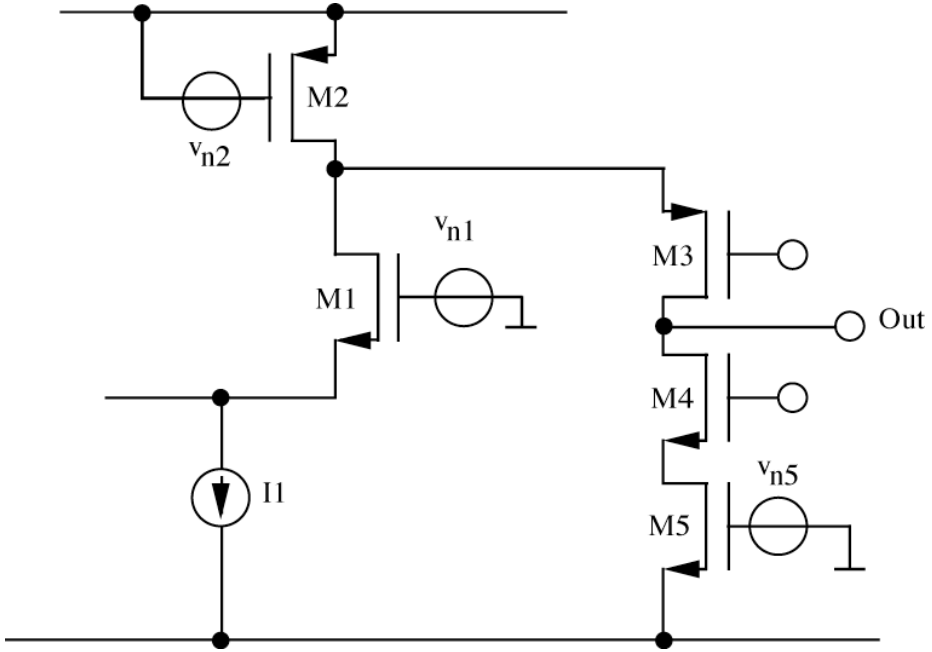
## Cascode scheme:

The noise is contributed by the input pair and the current sources of the cascode load.

$$v_{n,in}^2 = 2\left[v_{n1}^2 + \left(\frac{g_{m4}}{g_{m1}}\right)^2 v_{n4}^2\right]$$



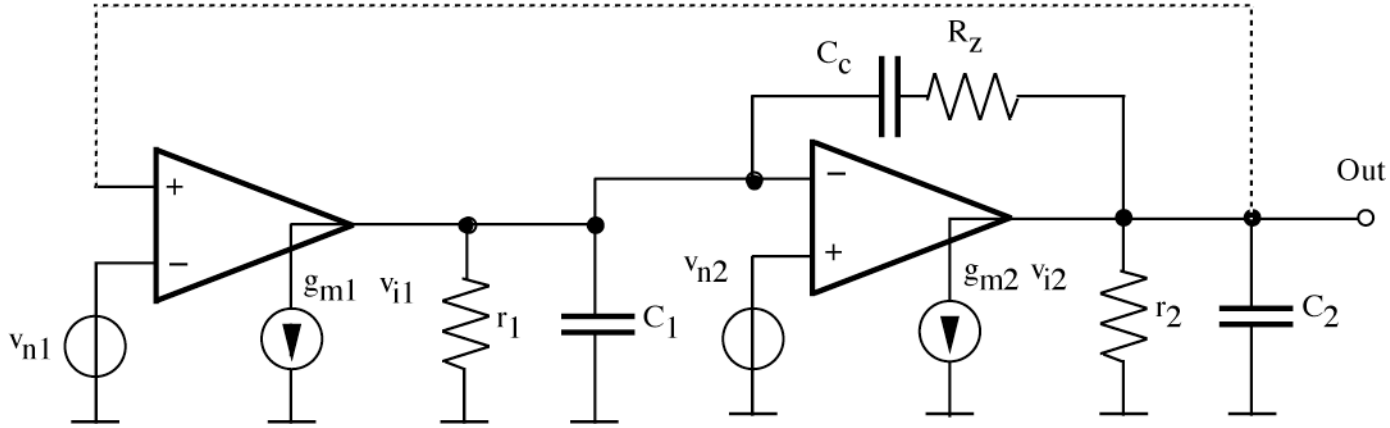
## Folded cascode scheme:



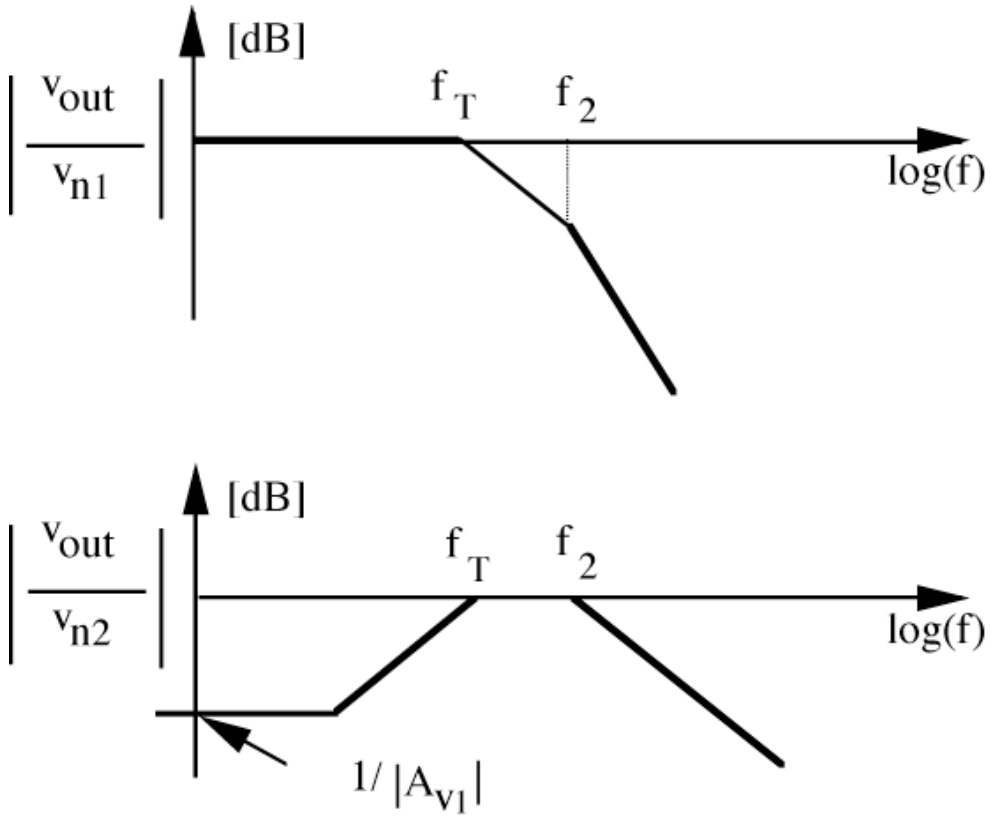

The noise contributed by the same source as in the cascode and by the current source M2.

$$v_{n,in}^2 = 2\left[v_{n1}^2 + \left(\frac{g_{m2}}{g_{m1}}\right)^2 v_{n2}^2 + \left(\frac{g_{m5}}{g_{m1}}\right)^2 v_{n5}^2\right]$$

# Two stage op-amp: (feedforward + zero nulling comp.)




The noise is modeled with two input referred noise sources: one at the input of the first stage and the other at the input of the second stage.




In the low frequency range the noise is dominated by $v_{n1}$.

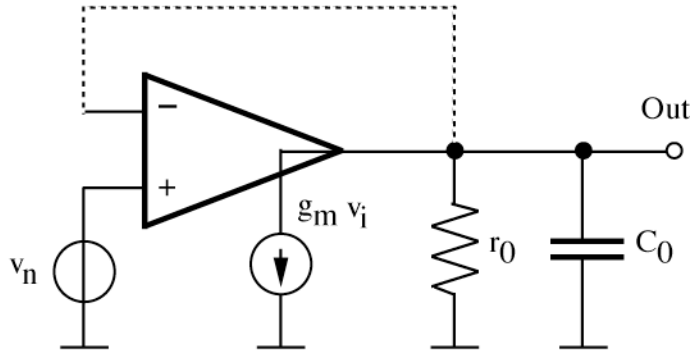
In the high frequency range the noise is dominated by $v_{n2}$.

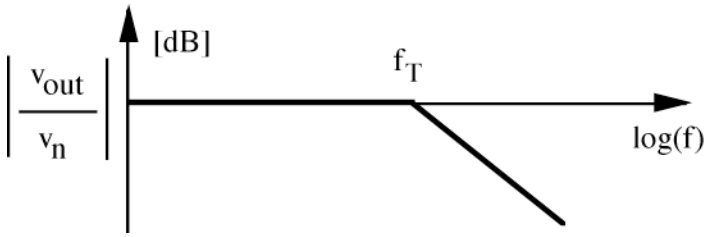
## Frequency response:

The input referred noise generator is transmitted to the output as a conventional input signal

The feedback network around the op-amp must be taken into account.

One stage amplifier:




The cutoff frequency is: $p_1 = -g_m/C_0$

## Power of noise:

We consider only the white term.

- Single stage amplifier:

$$\overline{v_{n0}^2} = \int_0^\infty v_n^2 \frac{df}{\left|1+s/p_1\right|} = 2\left(1+\alpha\right)\frac{8}{3}kT\int_0^\infty \frac{1}{g_{m1}}\frac{df}{1+\left(2\pi f C_0/g_{m1}\right)^2} = \frac{8}{3}\left(1+\alpha\right)\frac{kT}{C_0}$$

- Two stage amplifier: we consider only the white term contributed by the noise source of the second stage

$$v_{n2}^2 = 2\left(1+\alpha'\right)\frac{8}{3}\frac{kT}{g_{m2}}$$

$$\overline{v_{n0}^2} = \int_0^\infty v_{n2}^2 \frac{df}{\left|1+s/p_2\right|}$$

$$p_2 = \frac{g_{m2}}{C_1+C_2}$$

$$\overline{v_{n0}^2} = \frac{4}{3}\left(1+\alpha'\right)\frac{kT}{C_1+C_2}$$

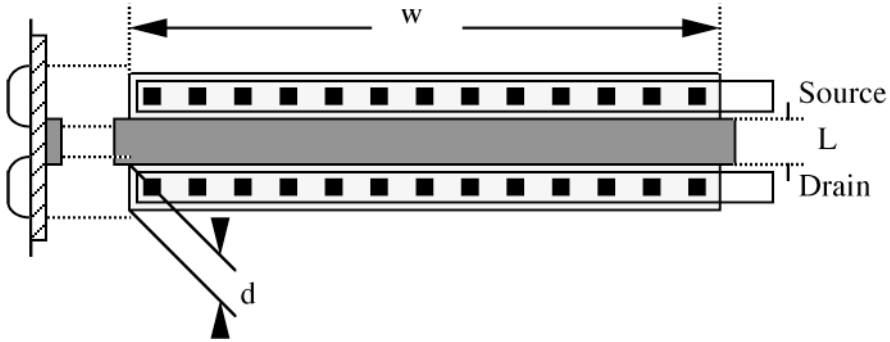
# Layout

**Rules:**

- Use poly connections only for voltage signals, never for currents, because the offset $RI \approx 15$ mV.
- Minimize the line length, especially for lines connecting high impedance nodes.
- Use matched structure (necessary common centroid).
- Respect symmetries (even respect power devices).
- Only straight-line transistors.
- Separate (or shield) the input from the output line, to avoid feedback.
- Shield high impedance nodes to avoid noise injection from the power supply and the substrate.
- Regular shapes and layout oriented design.

## Stacked layout:

$$C_{sb} = C_{db} = C_{jb} W (d + 2x_j)$$



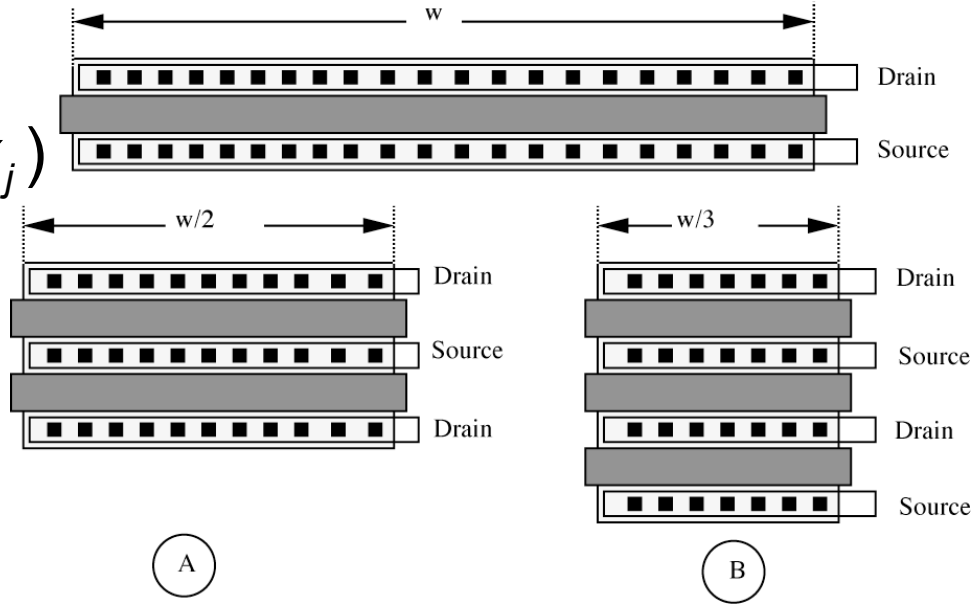

Structure A:

$$C_{sb} = \frac{1}{2} C_{db} = C_{jb} \frac{W}{2} (d + 2x_j)$$

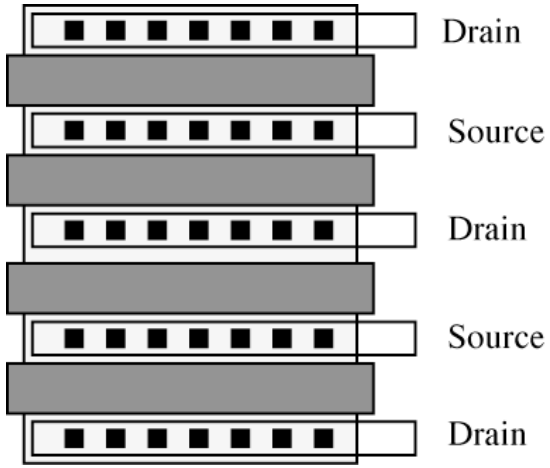
Structure B:

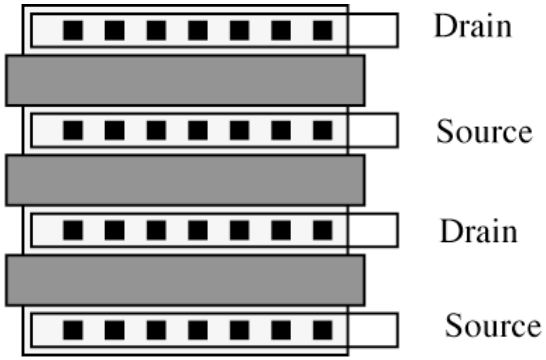
$$C_{sb} = C_{db} = C_{jb} \frac{2W}{3} (d + 2x_j)$$

Capacitances are further reduced if the diffusion area is shared between different transistors.



Key point: use of **equal width** transistors
Transistors with arbitrary width are not allowed.



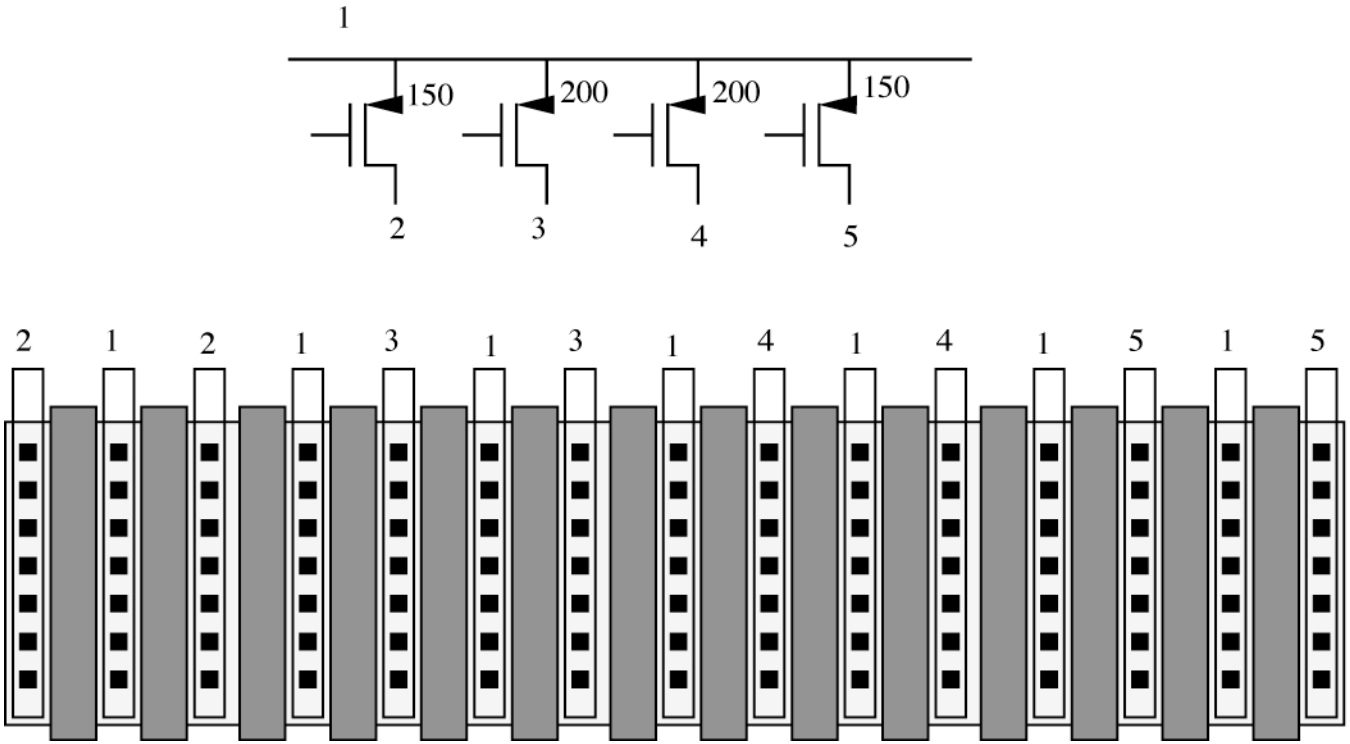



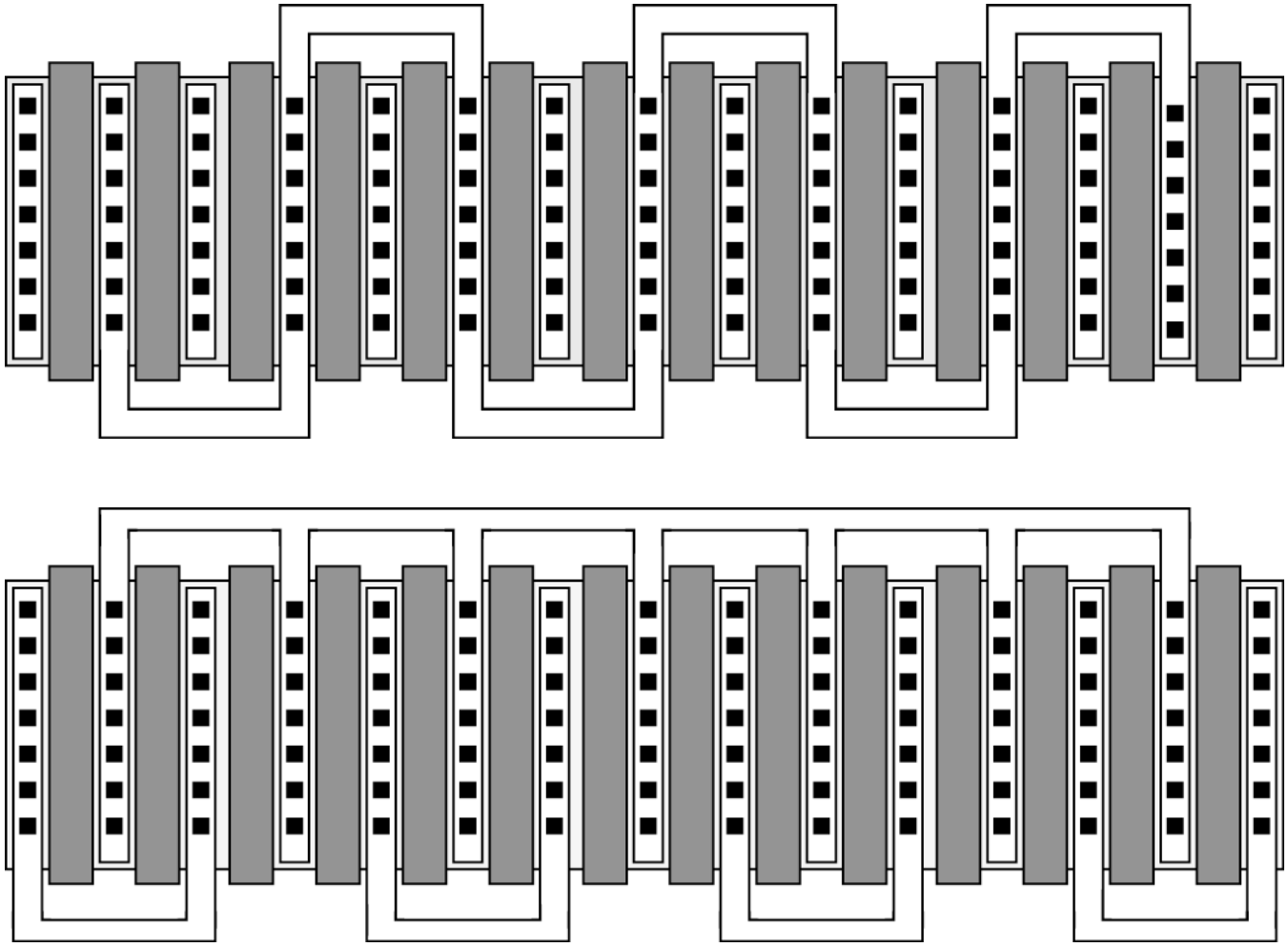

**Placement and routing:**

- If we divide a transistor in an odd number of parallel transistors the resulting stack has the source on one side and the drain on the other side.
- If we divide a transistor in an even number of parts the resulting stack has source or drain on the two sides.

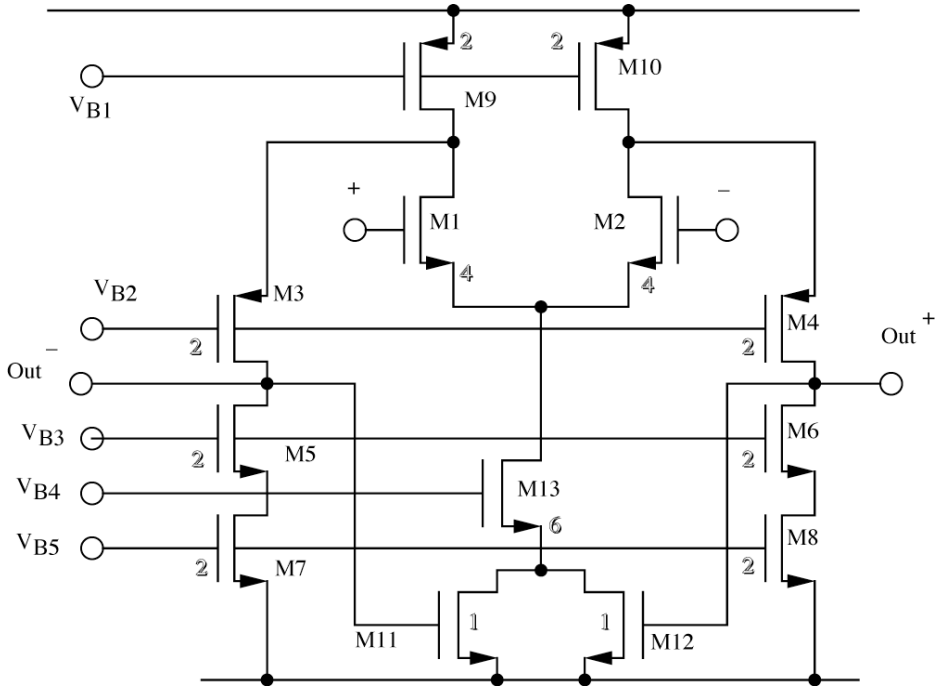
## Example:

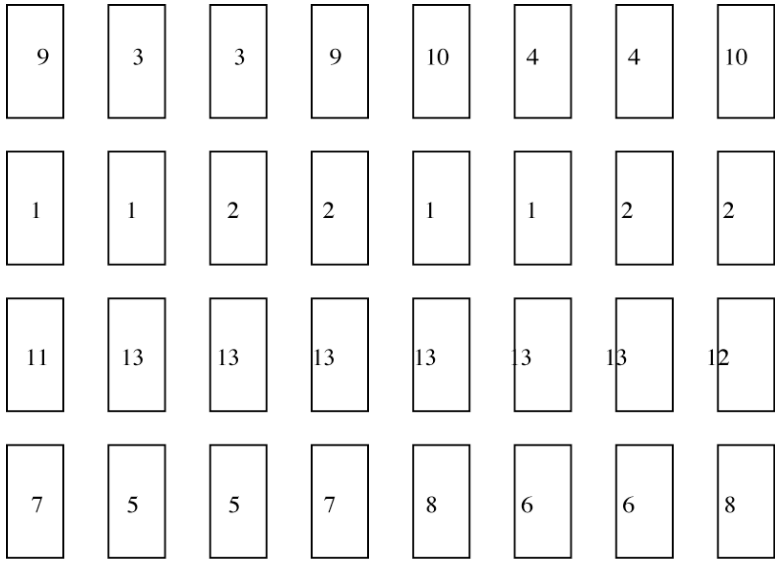
Routing into stacks: use of comb connections or serpentine connections.

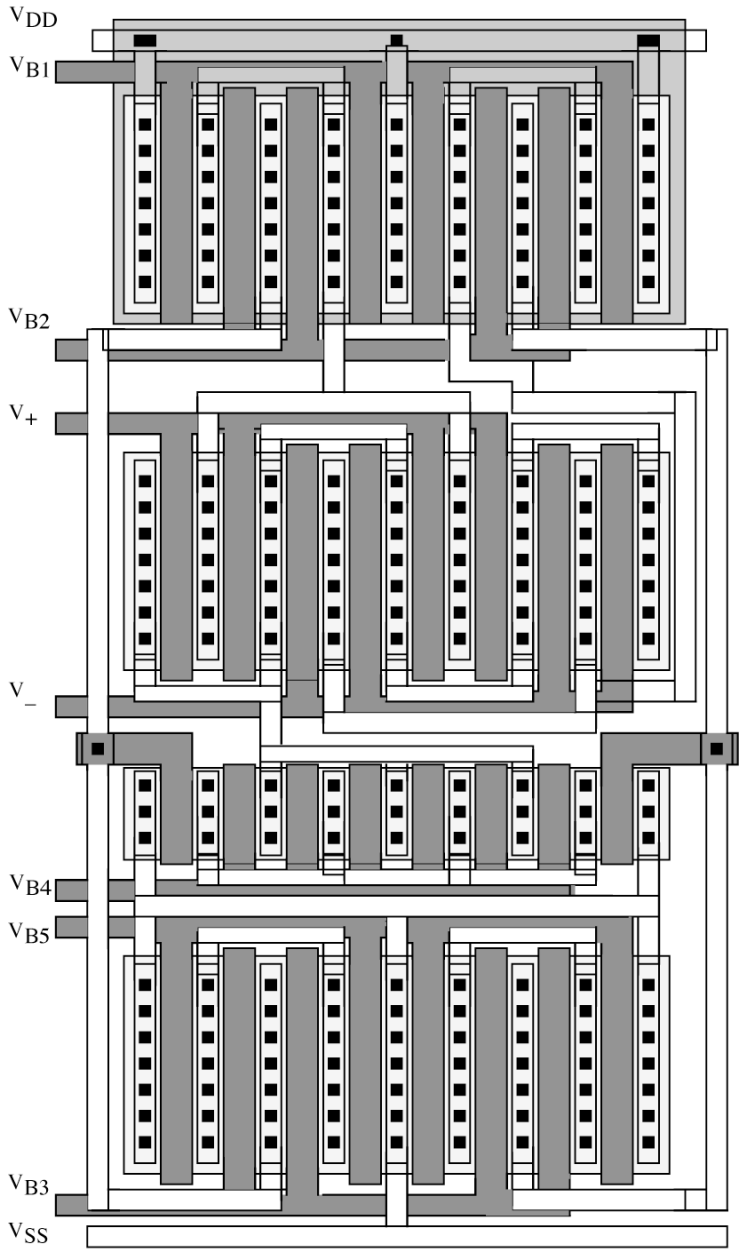




# Example: Fully differential folded cascode.




VDD
VB1
VB2
V+
V−
VB4
VB5
VB3
VSS