Single-Ended 2-Stage Opamp

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***Abstract*- This report details a design and simulation of a single ended 2-stage opamp for use in a Flash A/D Converter. The design is to maximize gain, frequency bandwidth, slew rate, and voltage swing; minimize power; improve phase margin and settling time. This 2-stage opamp is to be used in a 6-Bit Flash A/D Converter with a latch frequency of 500MHz.**

I. Introduction

A 2-stage operational amplifier (Opamp) is one of the most popular architectures for CMOS opamps in integrated circuit design. One of the advantages of a 2-stage opamp is the stability offered by using a Miller compensation capacitance, which will be described later in detail. A 2-stage opamp consists of a differential amplifier in the first stage, cascaded with a common source amplifier in the second stage. A current mirror is used to set the biasing of the two amplifier stages, and transistors dimensions are set to ensure each amplifier stage is biased for considerations such as voltage gain, bandwidth and voltage swing. The output is a single-ended output, although Fig 1 details a block diagram of a typical 2-stage opamp. The 2-stage opamp is designed fully in 90nm gpdk090 CMOS technology

The differential amplifier features a differential input and an active load to increase the gain. The inputs can either be fed into the gate of the PMOS or NMOS differential pair, and the active load uses its' complementary (i.e. NMOS or PMOS) as an active load to boost the gain of the differential amplifier stage. If the differential pair is fed into the inputs of PMOS pair, the overall opamp will feature optimal slew rate, unity gain frequency and minimized flicker noise (or 1/f noise) [3]. If a NMOS is selected as the differential pair input, the overall opamp transistor will improve wideband thermal noise. The choice of differential input, i.e. PMOS or NMOS, will be detailed in Section II.B.

The common source amplifier is known to provide high gain at the tradeoff of stability. A compensation capacitance (C_C) is used in a feedback configuration between the output and the input of the common source amplifier, otherwise called a Miller Capacitance. A PMOS transistor is used to set the biasing of the common source stage, as well as act as an active load to boost the common source amplifier gain [3].

The biasing stage will be a Wilson Current Mirror configuration used to provide a constant current source to bias the differential amplifier and common source amplifier stages. In addition to the Wilson Current Mirror configuration, NMOS or PMOS transistors will be used as current mirrors to set the bias current for its respective amplifier stages [2].

The overall 2-stage opamp will be designed to maximize gain, bandwidth, slew rate and voltage swing, and minimize power dissipation. Phase margin will be set to ensure stability of the opamp and the settling time will be optimized.

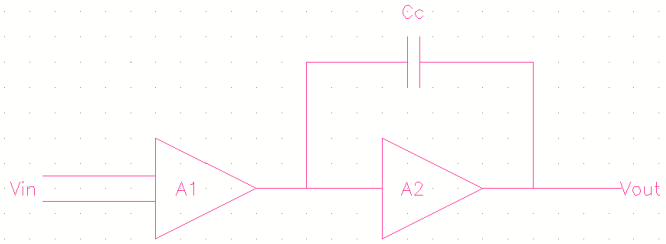

Fig 1 : Block Diagram of a 2-Stage Opamp

II. Single-Ended 2-Stage Opamp Architecture

A. *General 2-Stage Opamp Architecture*

Fig 2 details a simple 2-Stage Opamp architecture that is given in the initial assignment. Modifications are proposed in the following sections (B, C, D) as alterations to the simplified 2-stage opamp architecture.

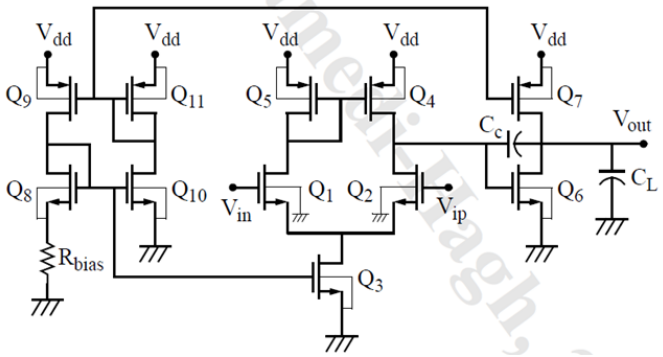

Fig 2 : Simplified architecture of a 2-Stage Opamp

B. *Differential Opamp Inputs*

The PMOS transistors are chosen to be the input of the differential amplifier to improve the slew rate and unity gain frequency of the overall 2-stage op amp, while reducing the overall 1/f noise.

Since the first stage features a PMOS input, the second stage – the common source amplifier – must feature a NMOS input drive transistor to maximize transconductance and, among other factors, increase the second pole, and increase unity-gain frequency.

C. *Compensation capacitance*

As noted in Section I, a compensation capacitance is an advantage in the 2-stage opamp design to improve stability of the opamp. In addition, an alteration to the general 2-stage opamp will be made to further increase the stability of the opamp: a biasing transistor will be used with the compensation

capacitance to act as a resistor and achieve lead compensation at frequencies only around the unity-gain frequency[1].

D. Setting Reference Current, I_{REF}

A NMOS transistor operating in the triode region will be used in place of a biasing resistor to improve power consumption and ease of fabrication. The bias current will be set by the dimensions of the NMOS transistor.

III. Design of the 2-Stage Opamp

A. Design and Specifications

The first step of the design was to set a phase margin to ensure stability of the opamp. The phase margin must be at least 60º to move the dominant pole to a lower frequency without affecting the second pole, to further improve the stability of the overall opamp. However, by moving the dominant pole, the right-hand plane zero results causing a phase lag in the opamps transfer function [1]. A biasing transistor, to act as a resistor, is used in conjunction with the compensation capacitance to move the zero to the right-hand plane. A phase margin of 64º was chosen to select our compensation capacitance, C_C. As noted in Section II.C, a biasing transistor is used between with C_C to improve stability. It should be noted that the settling time is also improved by improving the phase margin.

The slew rate was then used to select the bias current for the differential amplifier stage. A high bias current – set by the current mirror feeding a bias current into the differential amplifier stage – will be set to boost the slew rate. As noted in Section II.B, the input to the differential pair was chosen to be PMOS to improve the slew rate of the op amp.

A reference current, I_{REF}, was set up by a NMOS transistor operating in the triode region, as noted in Section II.D. A Wilson current mirror was used to set up a bias current – both PMOS and NMOS current mirrors – for the biasing of the differential stage amplifier, common source amplifier stage and the lead compensation transistor in the feedback configuration with the compensation capacitor. The Wilson mirror offers high output resistance, r_{rd}, so that a current can be mirrored to a lower resistance load. [2] A length size of 500nm has been selected for medium between gain and bandwidth considerations, and a 500nm length is used throughout the design of the opamp.

The differential amplifier was first designed by selecting the size of the input transistors, or PMOS transistors. Knowing the size of the biasing transistor (from the current mirror to the differential amplifier), the Cadence/Virtuoso parametric sweep tool was used to step the NMOS width and choose the NMOS width that offered the highest bandwidth, it is noted that the width offering the highest bandwidth also offered the highest gain as well[1]. (It is noted that the differential amplifier is fully symmetric between the differential inputs, so the transistor sizes are fully symmetric as well.) The selection of transistor sizes for the differential stage amplifier was chosen with the consideration of the output DC voltage to maximize voltage swing (i.e. 0.5V). It should be noted that the selection of the biasing PMOS transistor (or current mirror transistor feeding the bias current into the differential amplifier stage) directly alters the gain and bandwidth of the individual stages and the overall opamp [1]. Thus, in iterative trials and test benches to design the differential amplifier stage, the biasing PMOS transistor was often stepped using a parametric sweep to select desirable gain and bandwidth parameters.

The common mode stage was designed by first sizing the PMOS transistor, as the PMOS transistor set up current for the common mode stage. Once the PMOS transistor size was known, the NMOS transistor width was found by a parametric sweep and selecting the width that gave the maximum bandwidth. Similar to the design of the differential amplifier stage, optimal width maximized both gain and bandwidth.

Finally, the overall opamp parameters – width and bias voltage – were individually stepped to find optimal specifications. Since this opamp was to be designed for a 6-bit Flash A/D Converter with a latch frequency of 500MHz, a bandwidth of over 500MHz was chosen. A gain of 1000 was targeted, as a gain of 1000 typically offers 97-98% error when used as a comparator for a Flash A/D Converter [2]. During analysis of various test benches used to characterize the transistor and transistor configurations, it was noted that decreasing the length dimensions increased the bandwidth faster than increasing the width dimensions; during the simulations, it was also noted that increasing the width and the length would both increase the gain by nearly the same proportion. As a result, a smaller length was chosen for maximal bandwidth, and a large width was chosen to offer higher gain. The dimensions were found after multiple iterations in various test benches and the overall circuit.

B. Circuit Values

Through various iterations, test benches and overall circuit simulations, the following circuit parameters were chosen in Table 1.

Current Mirror	PM1, PM0	0.5um/0.5um
	NM2, NM3	3um/0.5um
	NM10	10um/0.5um
Differential Amplifier	PM4	5um/0.5um
	PM3, PM2	20um/0.5um
	NM7, NM6	2um/0.5um
Common Source Amplifier	PM8	10um/0.5um
	NM13	15um/0.5um
Feedback Configuration	NM14	1um/0.5um
	C0	300fF
Input bias	Vdm,bias	0.5V

Table 1 : Circuit component values in proposed design

[1] It should be noted that selecting transistor widths that optimize both gain and bandwidth does not imply that both gain and bandwidth are improved mutually exclusively.

C. Test Benches

Test benches were created in Cadence to simulate AC analysis, DC analysis and transient analysis.

IV. Results and Analysis

A. AC Analysis – Gain, Bandwidth, Phase Margin

Results for gain, bandwidth and phase margin are detailed in an AC analysis shown in Fig 4. The desired gain was 60dB, but due to limitations on bandwidth, a gain of 57.06dB was achieved. The bandwidth, defined by the unity gain frequency, was found to be 526.7MHz and the -3dB frequency was found to be 6.79MHz.

The phase margin was found to be -8.8, and does not meet the stability criteria. Various alterations and tests – particularly involving the compensation configuration, both the compensation capacitance and the lead capacitance transistor acting as a resistor – were done to try and improve the phase margin to meet the target of greater than 60 degrees (or 45 degrees) without sacrificing bandwidth. Since bandwidth was chosen to be greater than 500MHz, a poor phase margin was chosen. It is speculated that the opamp cannot achieve 500MHz bandwidth and near-60dB [1] gain without sacrificing phase margin, and through various trails of testing, a phase margin of greater than 60 degrees would limit the bandwidth to less than 130MHz.

B. DC Analysis – Power Consumption

The power consumption of the overall opamp was found to be 1.205mW.

C. Transient Analysis – Slew Rate, Voltage Swing, Settling Time

The slew rate was found using a transient analysis and shown in Fig 6. A pulse was used to measure the slew rate of the opamp (from 10% to 90%) and was found to be 5.2521V/um and -0.8699V/um.

The voltage swing was found using a large sinusoidal input and finding the voltage that the output saturates at. See Fig 5. The outputs were found to saturate at 995.66mV (maximum) and 79.898mV (minimum) for an overall voltage swing of 916.316mV.

The settling time was measured by stimulating the opamp with a small voltage pulse to and find when the percent overshoot would be within 1%. However, no overshoot was observed. An attempt was then made to find the settling time through a relation with the phase margin, but due to the ambiguous phase margin, a settling time could not be found.

C. Opamp Specifications

Table 2 outlines the specifications of the 2-stage opamp design.

Technology	gpdk090
Gain	57.06dB
Bandwidth	526.7MHz
freq (-3dB)	6.79MHz
Phase Margin	-8.8
Slew Rate	5.2521,-0.8699
Voltage Swing	916.316mV
Power	1.205mW

Table 2 : Design Specifications

V. Recommendations

As noted in Section IV.A, the phase margin is found to be less than 60 degrees. Since this opamp is to be used in a design of a Flash A/D Converter, further inspection and analysis will be required to mitigate issues regarding a phase margin of below 0. Should this result be an error during testing (i.e. test bench), this will not be an issue. Should the design require 500MHz bandwidth, as designed for, alternative solutions will be explored to compensate for a phase margin of -8.8 degrees.

VI. Conclusion

The 2-stage opamp designed in report has a gain of 57.06dB, a -3dB frequency of 6.77MHz and a unity gain frequency of 526.7MHz. The phase margin was found to be -8.8 degrees, or unstable [1]. This could either be an error in design or an error in measurement. If the phase margin is found to be an error in design, for applications such the Flash A/D Converter, bandwidth may have to be to improve the phase margin. The slew rate was found to be 5.2521V/um and -0.8699V/um, the voltage swing is found to be 916.316mV and the power consumption is found to be 1.205mW.

Acknowledgment

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References

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[2] . A. Sedra, K. Smith, "Microelectronic Circuits, 5th Edition," Oxford University Press Inc., New York, New York, pp 651-653, 922-943

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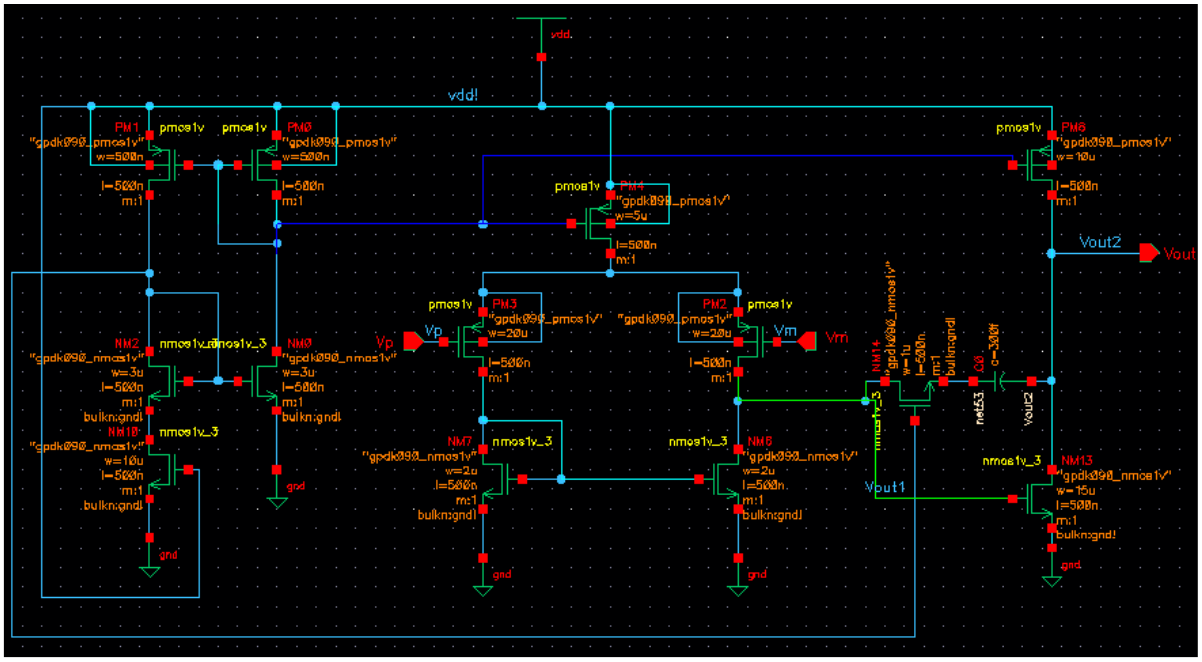

Fig 3 : 2-Stage Opamp Schematic designed in Cadence

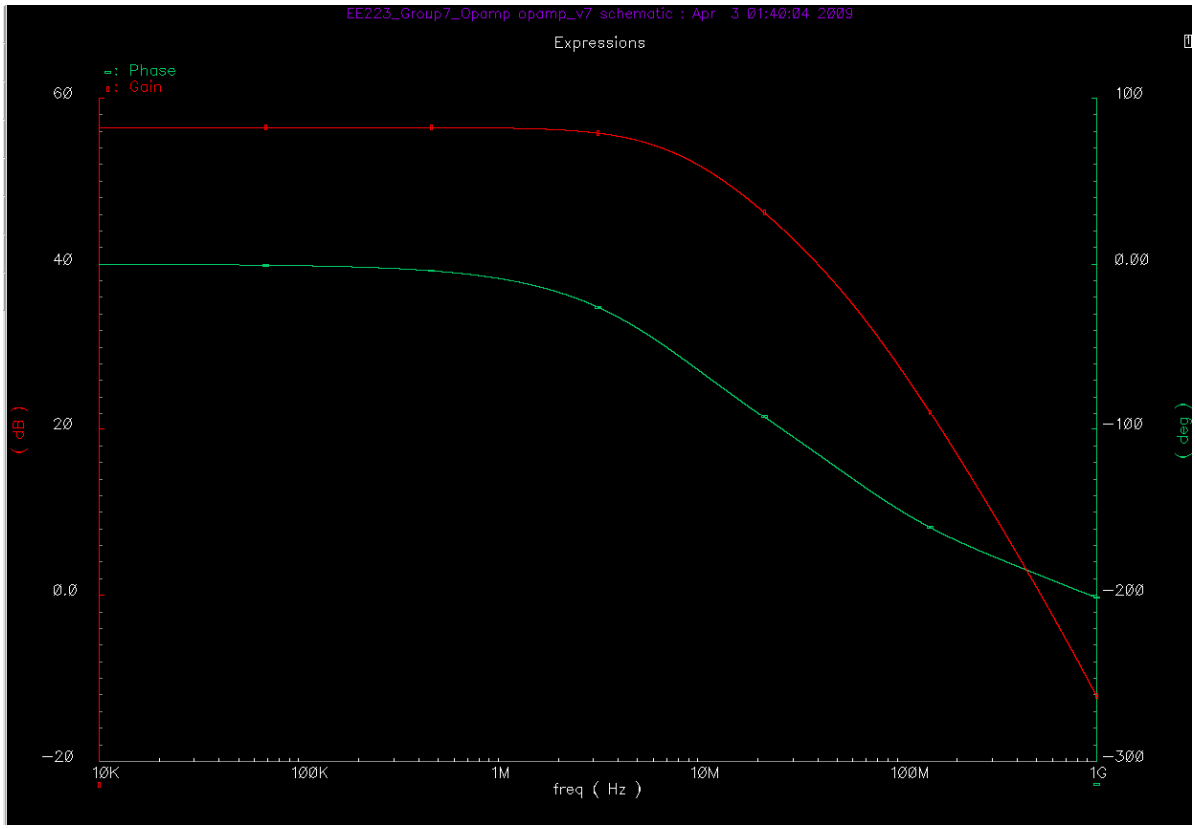

Fig 4 : Gain and Phase results from 2-Stage Opamp DC Analysis

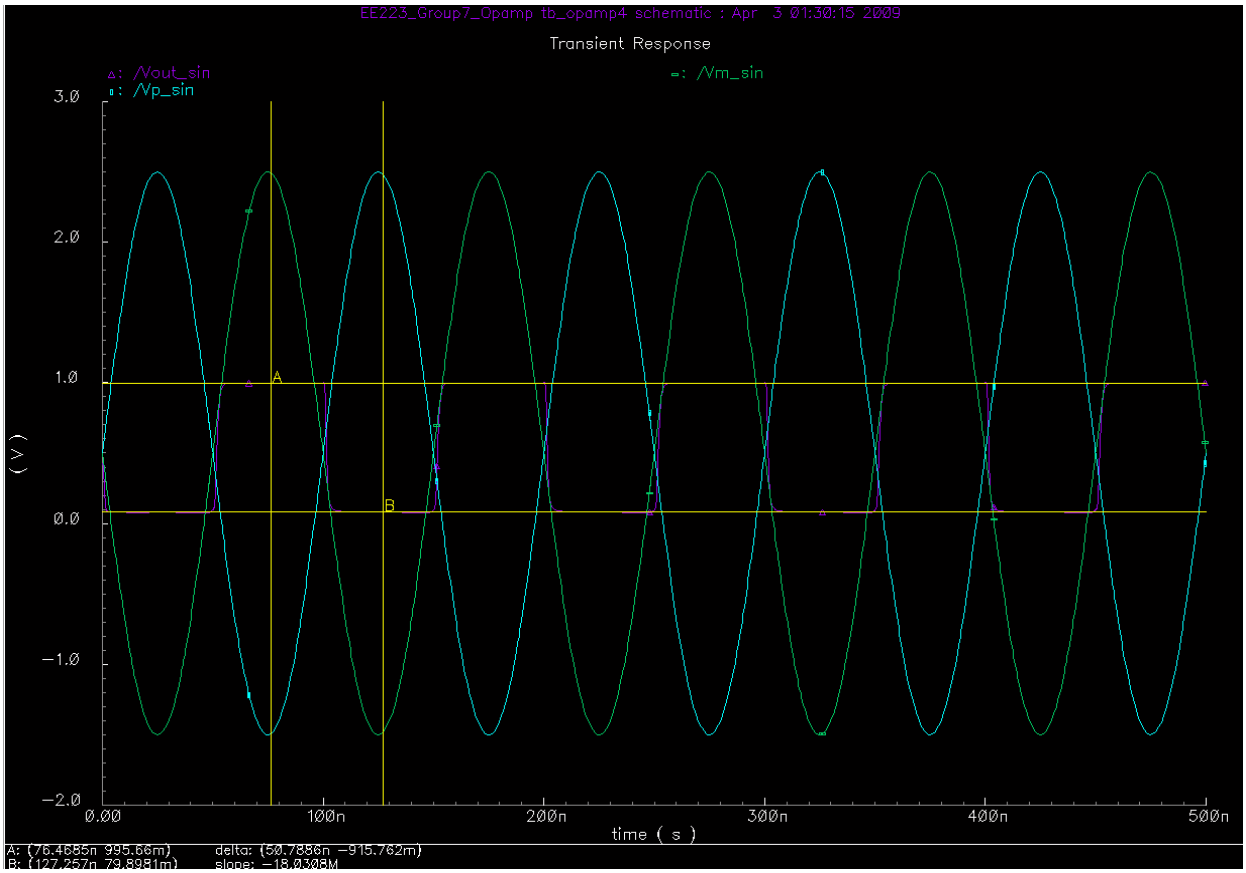

Fig 5 : Voltage Swing results from 2-Stage-Opamp Transient Analysis

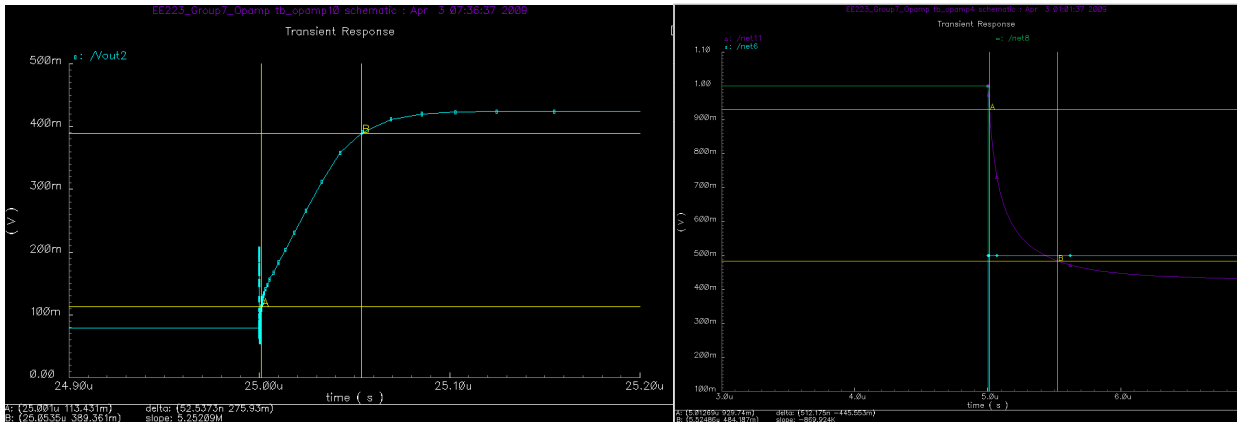

Fig 6 : Slew Rate (Rising, Falling) results from 2-Stage Opamp Transient Analysis