EL303
ANALOG INTEGRATED CIRCUITS
DESIGN PROJECT

OP-AMP DESIGN
PROGRESS REPORT

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1. TWO STAGE OP-AMP SCHEMATIC LEVEL DESIGN

1.1. Design Specifications:

In this project we are supposed to design an op-amp that satisfies following specifications:

- Avo >80dB
- GBW >10MHz
- SR >5V/us
- PM >60deg
- Ptot <500uW (includes biasing currents)
- $PSRR_{dd}$ >40dB (for f<200kHz)
- $PSRR_{ss}$ >40dB (for f<200kHz)
- Load: C_L=10pF

Also input voltage swing and output voltage swing is required to be as large as possible.

We were free to use any amplifier topology such as cascade, cascode, symmetric topologies which satisfy the specification above. Therefore, initially it is needed to decide on a particular topology that has potential to satisfy the specifications easily, so we start to design process by researching about outstanding op-amp topologies that are widely used. The research is ended up with 4 common topologies whose characteristic are well outlined in Table 9.1 of *Design of Analog CMOS Integrated Circuits* (B.Razavi):

	Gain	Output Swing	Speed	Power Dissipation	Noise
Telescopic	Medium	Medium	Highest	Low	Low
Folded-Cascode	Medium	Medium	High	Medium	Medium
Two-Stage	High	Highest	Low	Medium	Low
Gain-Boosted	High	Medium	Medium	High	Medium

Table 1: Comparison of performance of various op-amp topologies

According to *Table 1* , two-stage op-amp topology attracts the attention at the first glance since it is capable of supplying higher gain and output voltage swing than telescopic and folded-cascode topologies although it has drawbacks like low speed and covering larger areas than others. Also as seen in *Table 1*, telescopic and folded-cascode topologies are not sufficient to obtain high gain and this is the reason why they were not chosen to be used since

we are required to obtain a high gain as 80dB. In short, two-stage topology is chosen to implement an op-amp at given specifications since it has potential to supply high gain and highest voltage swing among the other topologies.

1.2.Two-Stage CMOS Op Amp Configuration:

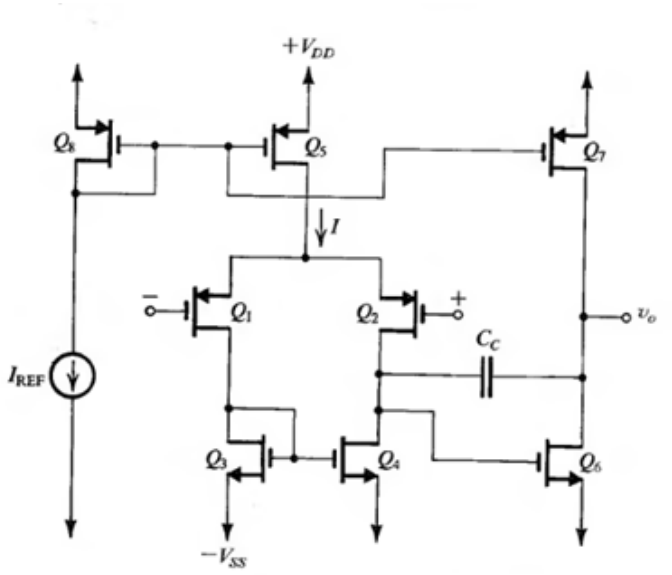


Figure 3.1: Two-stage CMOS op-amp configuration

Two-stage op-amp configuration is a popular structure for CMOS op amps and it has reasonably good quality in addition to the simplicity of circuit. As seen in *Figure 3.1* two-stage op-amp configuration is composed of a differential amplifier input stage and a common-source amplifier which is actively loaded by current source transistor Q_7. Differential amplifier is used in first stage since they are less sensitive to noise as a result of high CMRR. Although there is only a capacitor in the negative feedback path of second stage (frequency compensated) in *Fig. 3.1*, a resistor in parallel with C_c is used to improve phase margin of op-amp by placing zero at a negative axis location. One drawback of this configuration is that it does not have a low output resistance that is proper for driving low loads or low input impedance next stages.

In order to implement I_{REF} current in *Fig. 3.1,* a bias circuit in *Fig. 3.2* that is capable of providing current which is independent of the supply voltage and MOSFET threshold voltage. One useful and interesting property of this bias circuit is that g_ms of the transistors biased by this circuit are only dependent on R_B value and device dimentions.

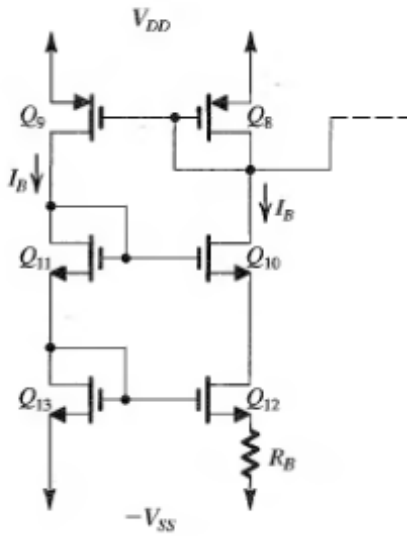


Figure 3.2: Configuration used to bias two-stage op-amp.

As seen in *Fig. 3.2* a resistor is connected in series with the source of Q_{12}. This resistor R_B determines the bias current I_B and g_{m12}.

Detailed analysis of the both two-stage op-amp circuit in *Fig. 3.1* and bias circuit in *Fig. 3.2* is performed in the ***Appendix***.

1.2.1. Schematic of Two Stage Op-Amp: Schematic of op-amp implemented in Cadence by using two-stage op-amp configuration and special bias circuit in Fig. 3.1 is below:

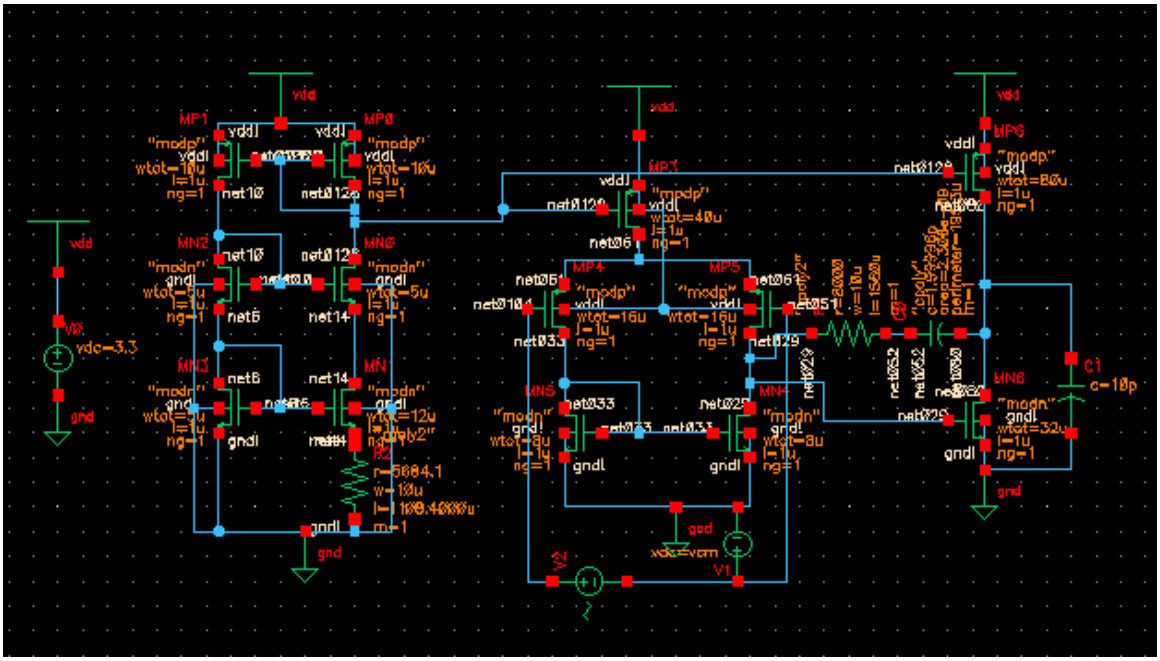


Figure 3.3: Schematic of two-stage op-amp.

2. APPENDIX

HAND CALCULATIONS:

2.1.Power Consumption: As seen in specifications of op-amp Ptot should be lower than 500uW. As seen in schematic in Figure 3.3, it is decided to use V_{SS}=0 for simplicity in layout design process and V_{DD}=3.3V. Hence:

$$Ptot = I_{tot}V_{tot} = I_{tot}V_{DD}$$

$$Ptot < 500uW, \quad I_{tot}V_{DD} < 500uW, \; I_{tot} < 151uA$$

$$I_{tot} = 2I_B + I_{D5} + I_{D7}$$

In order to obtain high gain and place the zero of op amp in high frequencies g_{m6} of transistor Q_6 *in* $Fig.3.1$ should be high. Since $g_{m6} = \frac{2I_{D6}}{Vov} = \frac{2I_{D7}}{Vov}$, we should bias common-source stage with a quite high current. In addition, g_{m1} of transistor Q_6 *in* $Fig.3.1$ has a dominant effect on the BW of op-amp so in order to obtain a high BW and reasonable gain in differential stage $g_{m1} = \frac{I_{D5}}{Vov}$ and in return I_{D5} should be as large as possible. Considering all of this, it is decided to choose $I_B = 10uA$, $I_{D5} = 40uA$, $I_{D7} = 80uA$.

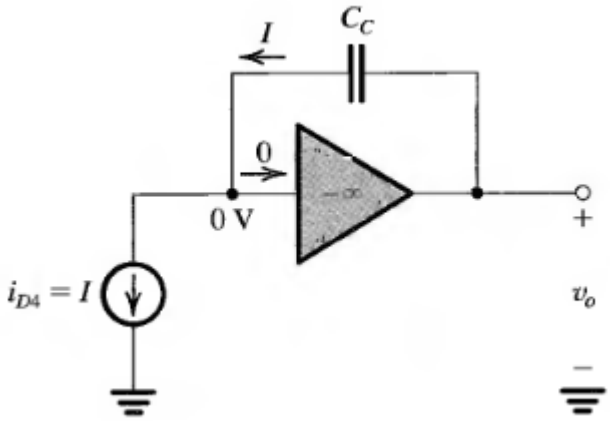


Figure A.1: Model for two stage opamp of Fig.3.1 under high differential voltage

$\boldsymbol{SR = \frac{I}{C_c}}$ Thus, determined values for currents is valid with SR constraint: SR>5V/us

According to calculation: $SR = 40uA/2pF$

SR=20V/us (The reason for picking $C_C = 2pF$ will be apparent in frequency analysis.)

2.2.Bias Circuit Analysis and Calculations: I_B current that is generated in bias circuit in *Fig.3.2* can be deduced as :

$$I_B = \frac{2}{\mu_n C_{ox}(W/L)_{12}R_B^2}\left(\sqrt{\frac{(W/L)_{12}}{(W/L)_{13}}} - 1\right)^2$$

As seen in the formula above, I_B only depends on values of process parameters and R_B as well as dimensions of Q_{12} and Q_{13}. Also Q_{12} and $Q_{13}$is deliberately mismatched, with $Q_{12}$is chosen usually about 4 times wider than Q_{13}(Sedra/Smith). However, the value of R_B should satisfy the equation below:

$$R_B = \frac{2}{\sqrt{2\mu_n C_{ox}(W/L)_{12} I_B}}\left(\sqrt{\frac{(W/L)_{12}}{(W/L)_{13}}} - 1\right)$$

According to equation of R_B, in order to obtain a stable current I_B with lower $R_B(in\ Kohms\ range)$, ratio of $\frac{\left(\frac{W}{L}\right)_{12}}{\left(\frac{W}{L}\right)_{13}}$ should be low. Therefore, I decided on $\frac{\left(\frac{W}{L}\right)_{12}}{\left(\frac{W}{L}\right)_{13}}$=**2.4**.

In order to obtain high voltage gain in each stage, L=1um is chosen. (The reason will be apparent in the Voltage Gain Calculation step.) Also, according to Table 6.1 in Sedra/Smith, typical values for $\mu_n C_{ox}$ is close to 125uA/V^2 whereas typical values for $\mu_p C_{ox}$ is close to 60uA/V^2. Vov is usually is in the range 0.2V to 0.4V so Vov is decided as 0.2V initially. According to all of these considerations, all the transistor dimensions and R_B value calculated below :

$$I_B = 10uA = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_{8,9} Vov^2 = \frac{1}{2}60\left(\frac{W}{L}\right)_{8,9} 0.2$$

$$\left(\frac{W}{L}\right)_{8,9} \cong 8.3\ so\ i\ rounded\ it\ up\ to\ 10\ for\ simplicity.$$

$$I_B = 10uA = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{10,11,13} Vov^2 = \frac{1}{2}125\left(\frac{W}{L}\right)_{8,9} 0.2$$

$$\left(\frac{W}{L}\right)_{10,11,13} \cong 4.2\ so\ picked\ up\ as\ 5\ in\ schematic\ design.$$

$\frac{\left(\frac{W}{L}\right)_{12}}{\left(\frac{W}{L}\right)_{13}}$=2.4 thus $\left(\frac{W}{L}\right)_{12} = 12$

$$R_B = \frac{2}{gm12}\left(\sqrt{\frac{\left(\frac{W}{L}\right)_{12}}{\left(\frac{W}{L}\right)_{13}}} - 1\right),\quad gm_{12} = \frac{2I_B}{\text{Vov}} \approx 100$$

Thus $\boldsymbol{R_B \approx}$ **9kohm.** Probably this value will not be similar to resistance in Cadence. It can be well defined by DC sweep analysis as $R_B\ is\ variable$.

2.3.Differential Amplifier: Transistor Dimensions Calculations:

As seen in Fig.3.1, there is a relation between currents $I_{D5}\ and\ I_{D8}$ as :

$$\frac{\left(\frac{W}{L}\right)_5}{\left(\frac{W}{L}\right)_8} = \frac{I_{D5}}{I_{D8}} = \frac{40uA}{10uA} = 4$$

$$\text{Thus } \left(\frac{\boldsymbol{W}}{\boldsymbol{L}}\right)_{\mathbf{5}} = \mathbf{4}\left(\frac{\boldsymbol{W}}{\boldsymbol{L}}\right)_{\mathbf{8}} = 40$$

Current through Q_1, Q_2, Q_3, Q_4 is $I_{D1} = I_{D2} = I_{D3} = I_{D4}$=20uA, and Vov=0.2V,

$$\frac{I_{D5}}{2} = 20uA = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{3,4} Vov^2 = \frac{1}{2}125\left(\frac{W}{L}\right)_{3,4} 0.2$$

$$\left(\frac{W}{L}\right)_{3,4} = 8$$

$$\frac{I_{D5}}{2} = 20uA = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_{1,2} Vov^2 = \frac{1}{2}60\left(\frac{W}{L}\right)_{1,2} 0.2$$

$$\left(\frac{W}{L}\right)_{1,2} \approx 16.6 \; so\ it\ is\ used\ as\ 16\ in\ schematic.$$

2.4.Common Source Stage: Transistor Dimensions Calculations

There are 2 types of offset such as random offset and systematic offset. Random offset derives from device mismatches that are random. Although all devices are perfectly matched, systematic offset can be present. However, systematic offset can be minimized by appropriate design. In order to minimize systematic offset in two-stage op-amp the condition below should be met for circuit in *Fig.3.1*:

$$\frac{\left(\frac{\boldsymbol{W}}{\boldsymbol{L}}\right)_{\mathbf{6}}}{\left(\frac{\boldsymbol{W}}{\boldsymbol{L}}\right)_{\mathbf{4}}} = \mathbf{2}\frac{\left(\frac{\boldsymbol{W}}{\boldsymbol{L}}\right)_{\mathbf{7}}}{\left(\frac{\boldsymbol{W}}{\boldsymbol{L}}\right)_{\mathbf{5}}}$$

We had decided on current through Q_7as $I_{D7} = 80uA$ at the beginning.

Therefore, from the current mirror between Q_7 and Q_8 we can decide the ratio $\left(\frac{W}{L}\right)_7$.

$$\frac{\left(\frac{\boldsymbol{W}}{\boldsymbol{L}}\right)_{\mathbf{7}}}{\left(\frac{\boldsymbol{W}}{\boldsymbol{L}}\right)_{\mathbf{8}}} = \frac{I_{D7}}{I_{D8}} = \frac{80uA}{10uA} = 8$$

$$\left(\frac{\boldsymbol{W}}{\boldsymbol{L}}\right)_{\mathbf{7}} = 80$$

Since we have calculated $\left(\frac{\boldsymbol{W}}{\boldsymbol{L}}\right)_{\mathbf{4}}, \left(\frac{\boldsymbol{W}}{\boldsymbol{L}}\right)_{\mathbf{5}}, \left(\frac{\boldsymbol{W}}{\boldsymbol{L}}\right)_{\mathbf{7}}$ we are able to deduce $\left(\frac{\boldsymbol{W}}{\boldsymbol{L}}\right)_{\mathbf{6}}$ from minimization condition of systematic offset .

$$\frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_4} = 2\frac{\left(\frac{W}{L}\right)_7}{\left(\frac{W}{L}\right)_5} = 2\frac{80}{40} = 4 \qquad Thus\ \left(\frac{W}{L}\right)_6 = 32$$

Summation of dimensions of transistors used in schematic as a result of hand calculations:

$$\left(\frac{W}{L}\right)_{1,2} = 16, \quad \left(\frac{W}{L}\right)_{3,4} = 8, \quad \left(\frac{W}{L}\right)_{\mathbf{5}} = 40, \quad \left(\frac{W}{L}\right)_{6} = 32$$

$$\left(\frac{W}{L}\right)_{\mathbf{7}} = 80, \quad \left(\frac{W}{L}\right)_{8,9} = 10, \quad \left(\frac{W}{L}\right)_{10,11,13} = 5\,, \quad \left(\frac{W}{L}\right)_{\mathbf{12}} = 12$$

2.5.Voltage Gain of Two-Stage Op-Amp:

Voltage gain of the first stage :

$$A_1 = -g_{m1}(r_{o2} \parallel r_{o4})$$

$$A_1 = -\frac{2}{V_{OV1}} \Big/ \left[\frac{1}{|V_{A2}|} + \frac{1}{V_{A4}}\right]$$

DC Voltage gain of actively loaded common-source amplifier:

$$A_2 = -g_{m6}(r_{o6} \parallel r_{o7})$$

$$A_2 = -\frac{2}{V_{OV6}} \Big/ \left[\frac{1}{V_{A6}} + \frac{1}{|V_{A7}|}\right]$$

As seen in equations of dc voltage gain of each stage above, as the early voltages of transistors Q_2, Q_4, Q_6 and Q_7 increases dc gain obtained in first and second stages increases.

As we know; $V_A = V_A{}'$ L; so in order to increase early voltages of transistors L is chosen as 1um.

Overall dc voltage gain is the product of gains at each stage:

$$A_V = A_1 A_2 = g_{m1}(r_{o2} \parallel r_{o4}) g_{m6}(r_{o6} \parallel r_{o7})$$

We can simply find out the values of output resistances ro2, ro4, ro6 and ro7 by looking DC operating points of corresponding transistors in schematic. There is a transconductance parameter like **gds** between DC operating parameters in netlist.

$$r_o = \frac{vds}{gds}$$

Thus we deduced output resistances as below by utilizing dc operating points of transistors:

$$r_{02} \approx 2.2Mohm \quad r_{04} \approx 986kohm$$

$$g_{m1} \approx 200uA/V$$

Thus $A_1 = 200u * (2.2Mohm \;\; // \;\; 986kohm)$ = 139V/V

$$r_{06} \approx 2.2Mohm \quad r_{07} \approx 986kohm$$

$$r_{06} \approx 1.2Mohm \quad r_{07} \approx 343kohm$$

$$g_{m6} \approx 734uA/V$$

$A_2 = 734u * (1.2Mohm \ // \ 343kohm)$=186V/V

By using these values:

$$A_V = A_1 A_2 = 88.23dB$$

2.6.Frequency Response of Two-Stage Op-Amp:

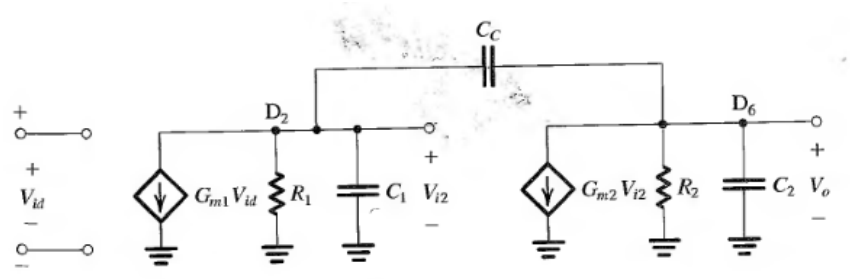


Figure A.2: Equivalent high frequency circuit of op-amp in *Fig.3.1*

Poles and zeros of the equivalent circuit in *Fig. A.2* as below and f_{P1} is the dominant pole.

$$f_{P1} \cong \frac{1}{2\pi R_1 G_{m2} R_2 C_C}$$

$$f_{P2} \cong \frac{G_{m2}}{2\pi C_2}$$

$$f_Z \cong \frac{G_{m2}}{2\pi C_C}$$

Where $C_2 \approx C_L$.

Cc should be selected so that the a phase margin above 60degree can be obtained. In order to 60degre phase margin $C_C \approx 0.22 * C_L \approx 2pF$.

In order to design an opamp with a gain slope of -20dB/decade until unity gain frequency, the unity gain frequency w_t should be lower than w_z and w_{P2}.

$$\omega_t = (G_{m1} R_1 G_{m2} R_2)\omega_{P1}$$

$$\omega_t = \frac{G_{m1}}{C_C}$$

Hence $f_t = \frac{gm_1}{2\pi C_C} \approx 15.92MHz$,

Phase margin of the equivalent circuit in *Fig A.2* can be deduced as follow:

$$\begin{aligned}\text{Phase margin} &= 180° - \phi_{\text{total}} \\ &= 90° - \tan^{-1}(f_t/f_{P2}) - \tan^{-1}(f_t/f_Z)\end{aligned}$$

As seen in equation above, it is possible to improve phase margin by arranging ratio of f_t/f_z equal or smaller than zero so that arctangent comes zero or negative. By adding a resistance R in series to Cc it is possible to provide it since zero of circuit can be send to infinity or a negative location according to equation :

$$s = 1/C_C\left(\frac{1}{G_{m2}} - R\right)$$

As seen from the equation of zero above, by selecting R as larger than $\frac{1}{G_{m2}} \approx 1.2kohm$ it is possible to place zero at the negative axis and arctangent of f_t/f_z will be negative. However in order to obtain high PM in schematic R=8k used.

$$\frac{f_t}{f_z} \approx -0.27 \quad \frac{f_t}{f_{P2}} \approx 1.36$$

$$PM = 90 - 53.7 + 15.24 \approx 68.94\, degree$$

In addition to all of these calculation in order to obtain high output voltage headroom and high output voltage legroom (high output voltage swing), V_{OUT} should be biased around 3.3V/2 $\approx 1.6 - 1.8V$.

Output Voltage Swing: Since we assumed Vovs as 0.2V for each transistors, output is bounded by 3.3V-0.2V=3.1V from above and it is bouded from below by the Vov value of Q6 transistor. Thus output voltage swing is from 0.2V to 3.1V.

3. DC OPERATING POINTS OF OP-AMP SCHEMATIC

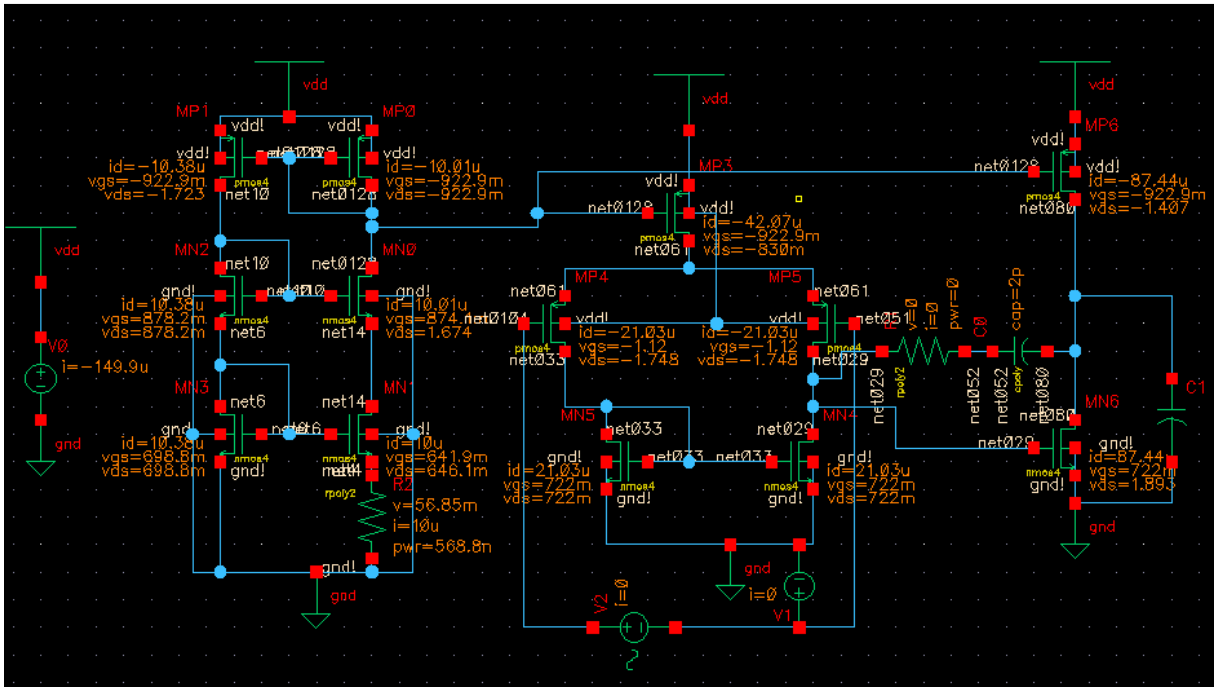


Figure 3.4: DC operating points of two-stage op-amp.

As seen in Fig.3.4 output point of two stage opamp is biased around 1.8V in order to have proportional voltage headrooms and legrooms. Thus it is prevented to lead a situation like high voltage headroom with low legroom or vice versa.

4. TWO STAGE OPAMP SCHEMATIC SIMULATIONS

4.1. Gain, GBW and Phase Margin:

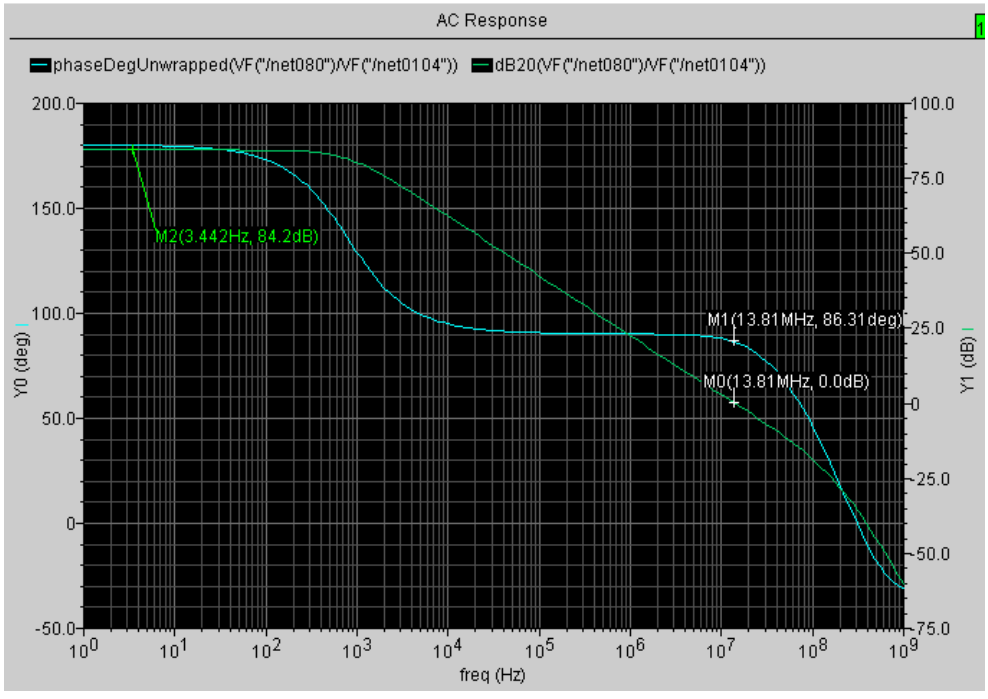


Figure 3.5: Frequency response of opamp implemented as Fig.3.4.

As seen in *Fig.3.5* DC gain of two stage opamp is 84.2dB which is lower than the value we deduced in hand calculations (88.23dB). Distinction between the hand calculations and simulation may be derive from some assumptions we made and Cadence also takes account of higher order effects of transistors during simulations which we disregard to simplify hand calculation process. Also the unity gain frequency of opamp is 13.81MHz according to *Fig.3.5.* Although this value satisfy our specifications it is lower than the value we calculated (15.92MHz). In addition, in Fig.3.5 we get PM around 86degree, higher than the value calculated($\sim 69degree$).

4.2.Power Consumption:

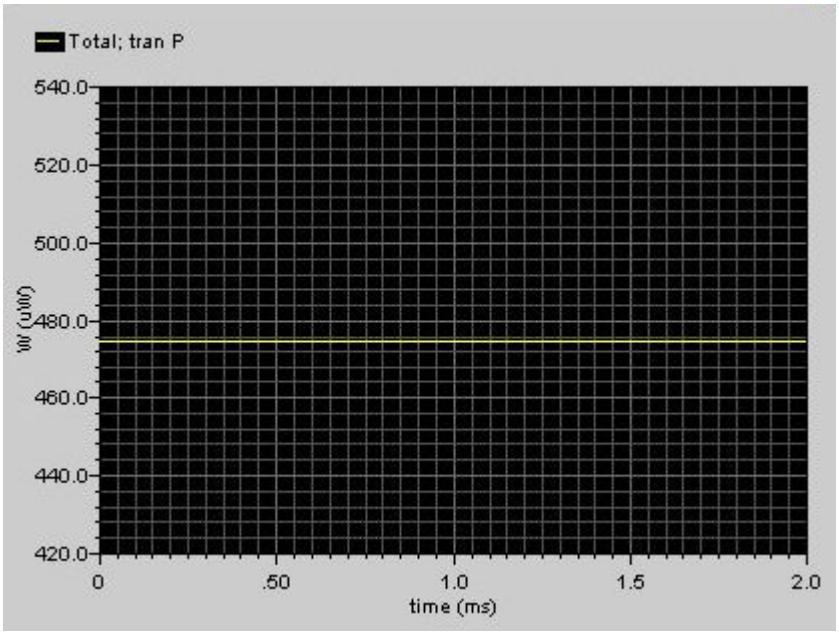


Figure 3.6: Total power consumption graph of opamp.

As seen in Fig.3.6, power consumption of opamp is close to given design specification but it nevertheless satisfy the condition Ptot<500uW. Ptot graph in Fig.3.6 obtained from transient analysis through **Results>Direct Plot>Main Form**.

4.3.Slew Rate:

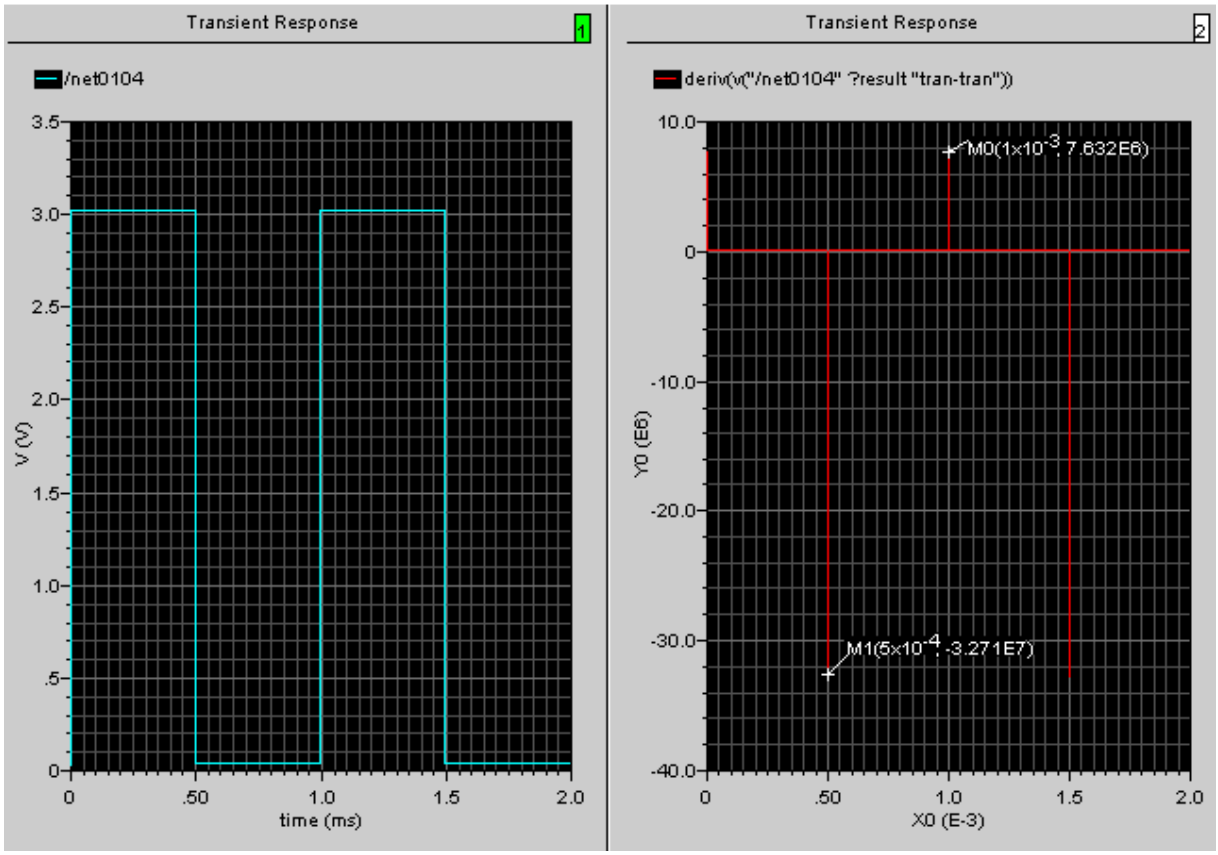


Figure 3.7: Transient response to input pulse signal and derivative of output pulse utilized to determine Rising Edge and Falling Edge Slew rates.

As seen in the graph of derivative of output signal in Fig.3.7, rising edge slew rate is around 7.63V/us and falling edge slew rate is around 32.7/us. Rising edge slew rate is higher than design specifications (7.63V/us>5V/us) and lower than the SR that is calculated during calculations. Falling edge slew rate is much larger then the design specification given and also larger than calculated SR=20V/us. Maybe the reason of higher falling edge than rising SR can be that we are using a single ended topology for output stage.

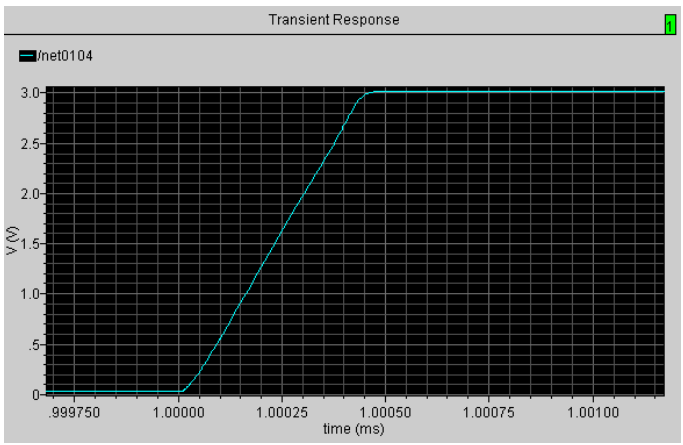


Figure 3.7.1: Rising Edge SR

4.4.$PSRR_{DD}$

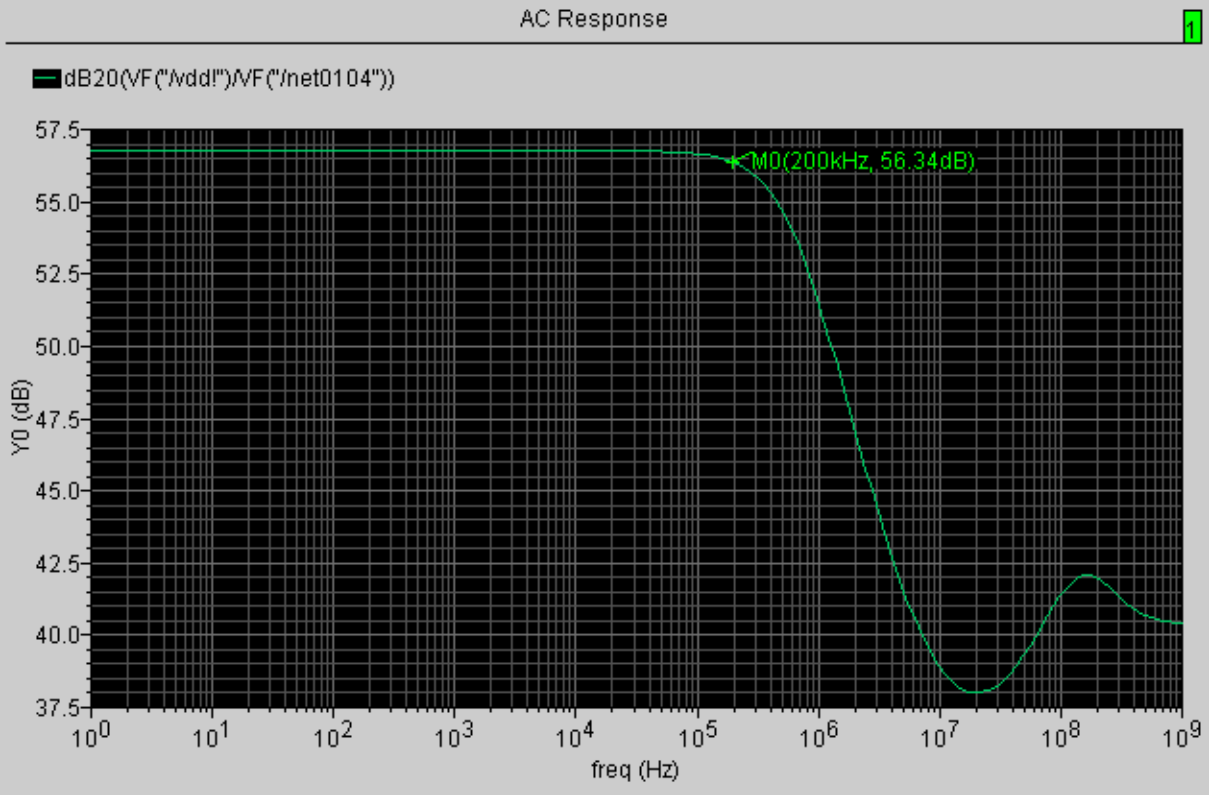


Figure 3.8: $PSRR_{DD}$ analysis of two stage op-amp.

Negative input of opamp is buffer connected and no signal is given from the positive input, in order to meause $PSRR_{DD}$ input signal superimposed on VDD signal. PSRR of an opamp is given as below :

$$PSRR = \Delta VDD / \Delta VOUT.$$

When the AC analysis is performed graph in Fig.3.8 obtained. According to this graph of PSRR, 56.35dB ratio is obtained at 200kHz. Thus, given specification for $PSRR_{DD}$ is satisfied.

4.5.Output Swing Range:

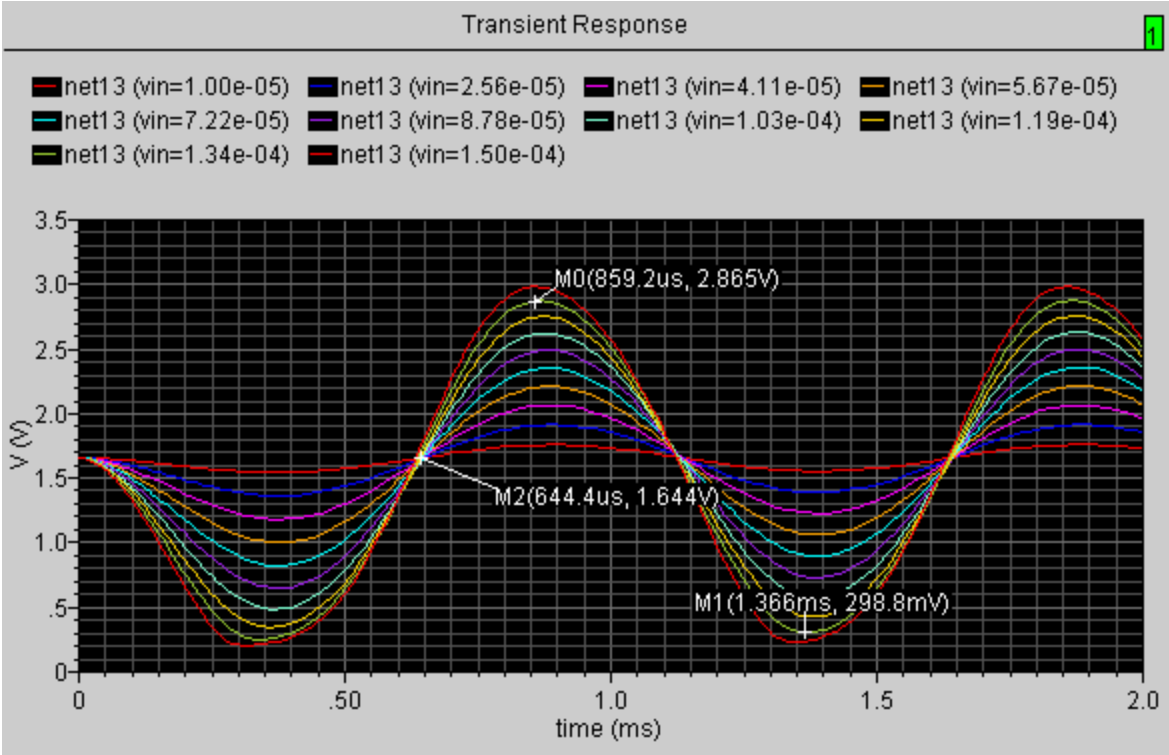


Figure : Output Voltage Swings

5. CONCLUSION:

As seen in table below all the specifications are met the circuit implemented in Fig.3.4. As seen in table below, power consumption is so close to design specification. It can be improved by changing DC bias current at each stage. However this change will lead to complete change in the small signal parameters and thus change of simulation results.

	Handcalculations	Simulation Results	Specifications
Av	**88.23**	**84.2**	**>80dB**
Unity Gain Freq.	**15.92Mhz**	**13.81Mhz**	**>10Mhz**
PM	**69degree**	**86degree**	**>60degree**
SR	**20V/us**	**7.63V/us**	**>5V/us**
Ptot	**462uW**	**Around 480uW**	**<500uW**
PSRRdd	**-**	**56.35dB**	**>40db**
Output Swing	**0.2V to 3.1V**	**0.15V to 3V**	

6. LAYOUT DESIGN OF TWO STAGE OP-AMP

First stage in the layout design is the creating stick diagram representation of circuit to be constructed on the layout level. Thus, in order to go through convention, stick diagram of two stage of op-amp derived by utilizing source-drain sharing method and cross coupling method in the input stage of op-amp.

Source-drain sharing method let us to create more compact layout design in addition to less parasitic resistances. In order to utilize source-drain sharing of transistors, there should be common ratio between some of transistors. In the schematic level design we had foresee this situation so that some of transistors arranged like follow:

$$\left(\frac{W}{L}\right)_7 = 2\left(\frac{W}{L}\right)_5 = 80\,,\quad \left(\frac{W}{L}\right)_6 = \left(\frac{W}{L}\right)_{3,4} = 16,\ \left(\frac{W}{L}\right)_{8,9} = 10,\ \left(\frac{W}{L}\right)_{11,13} = 5$$

These mosfets with input pmos transistors of differential pair are constructed according to source drain methodology, in other words 2 or 3 transistors are created on the same mosfet structure.

As it is stated in *Design of Analog CMOS Integrated Circuits* (B.Razavi), gradients in fabrication process give rises to some mismatches. However, there are some certain ways to reduce the error that derives from this mismatches by using common centroid configuration. (refer to Fig. 18.19 in Razavi). However routing of interconnects in this configuration is quite difficult since they can lead to some asymmetries. One alternative basic configuration in order to suppress linear gradients effect in layout is one dimentional cross coupling as seen in Fig.3.9. In two stage op-amp layout design we benefit from one dimentional cross coupling configuration to prevent input stage to be affected by gradients.

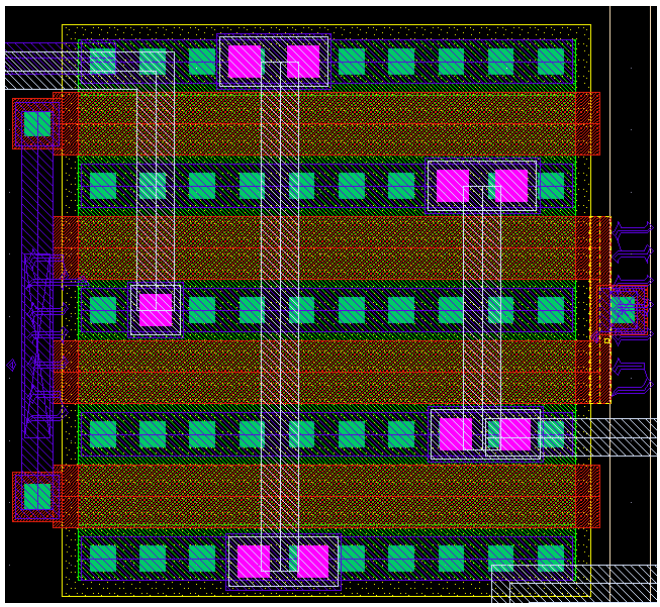


Figure 3.9: One dimentional cross coupling of Q1 and Q2 transistors in Fig.3.1.

As seen in Fig.3.3, half of transistors are placed along vertical axis and Q1 and Q2 are formed by connecting either the near ones and the far ones.

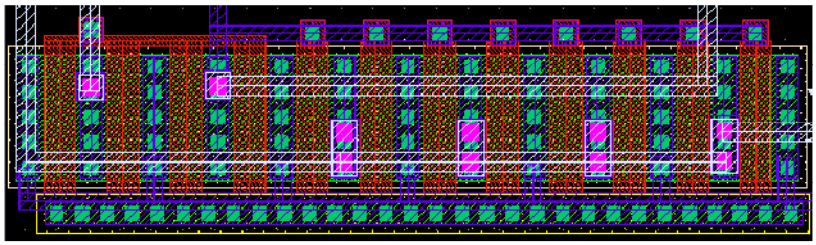


Figure 3.10: Source Sharing of Q3, Q4, Q6 in *Fig.3.1.*

In addition to this methods depicted in *Fig. 3.9 and 3.10*, we obey the some layout design conventions such as putting all pmos transistors close to eachother to place them in the same nwell, using contacts(NDC or PDC) which are placed in positions to be close each pmos or nmos respectively. Also in order to design layout in as minimum area as possible, almost after each connection, DRC used to determine if connection violate a design rule or whether it is possible to use connection closer to other component or not. Thus, at the end of layout design we did not face with any DRC errors as seen in *Fig. 3.11*.

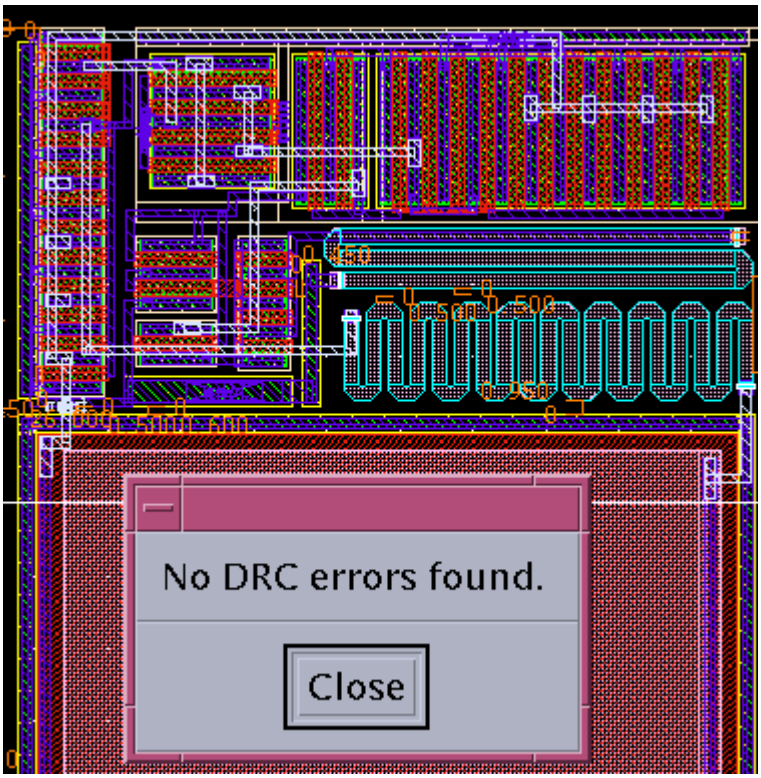


Figure 3.11: Results of DRC simulation of two-stage op-amp.

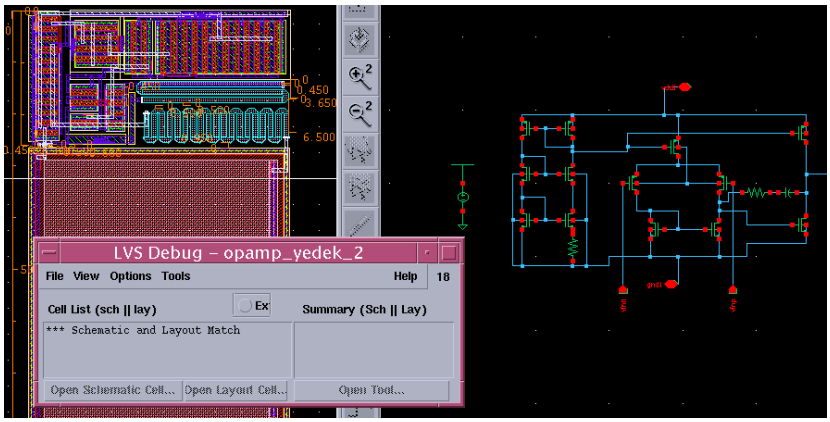


Figure 3.12: Result of LVS Simulation of Two-stage op-amp.

As seen in Fig.3.12, layout and schematic of two-stage op amp in Fig. 3.1 is matched at the end design. However, they were not matched in the first attempt since bodies of all nmos transistors in layout and schematic did not matched each other. In order to resolve this problem, more PDC contacts are used such that all nmos transistors are close to contacts.

After DRC and LVS simulations, our layout seems like follow:

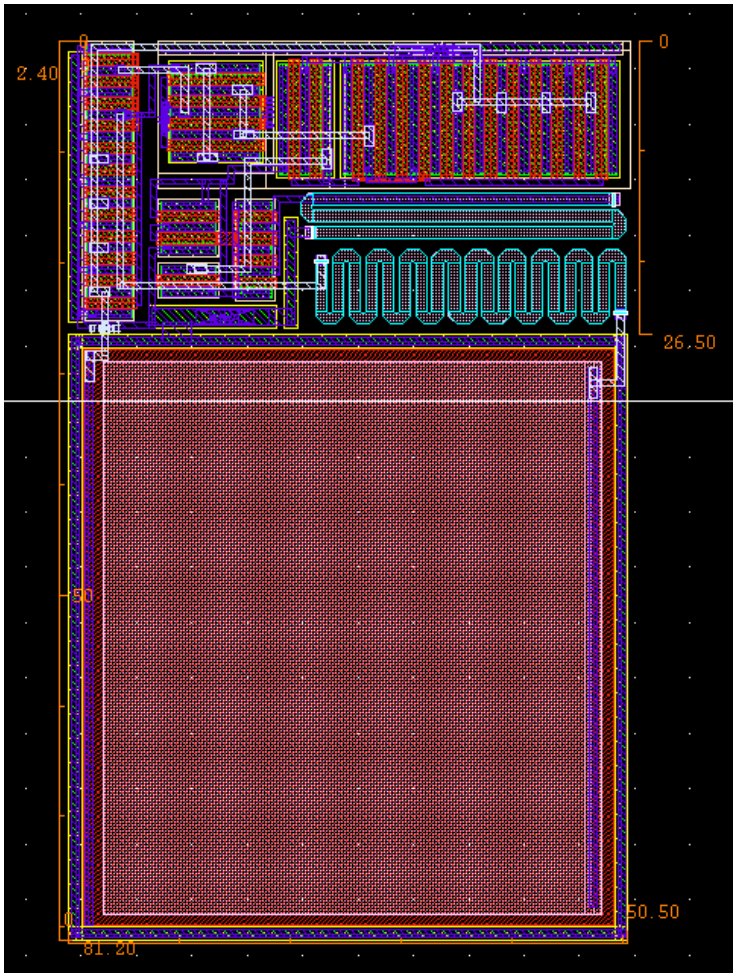


Figure 3.13: Layout level design of Two-stage op-amp.

As seen in Fig.3.13, we managed to construct layout of opamp in an area :

AREA: 81.20um X 50.50um.

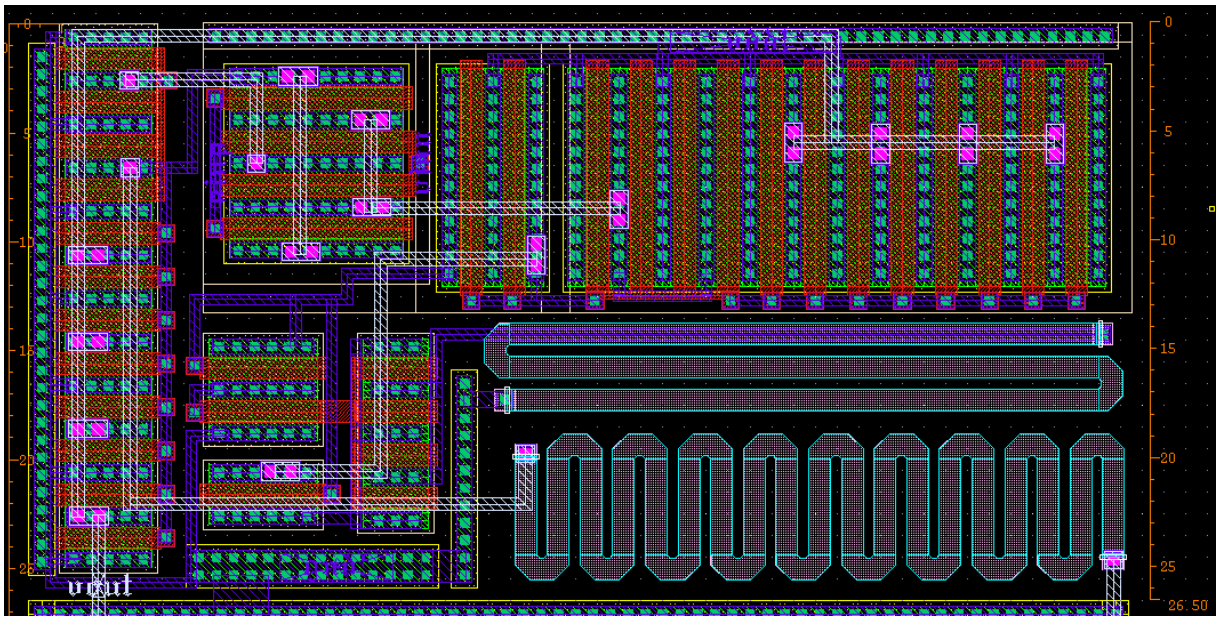


Figure 3.14: Layout of only 6 pmos, 7nmos and 2 Resistors.

After DRC and LVS simulations are completed, we conduct the RCX simulation for only capacitances. Extracted view of layout is with parasitic capacitances as in *Fig.3.15:*

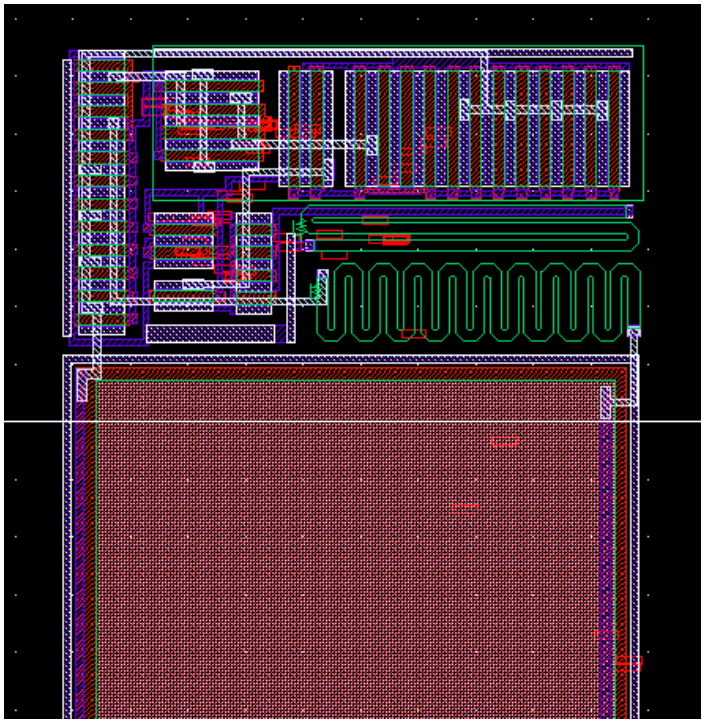
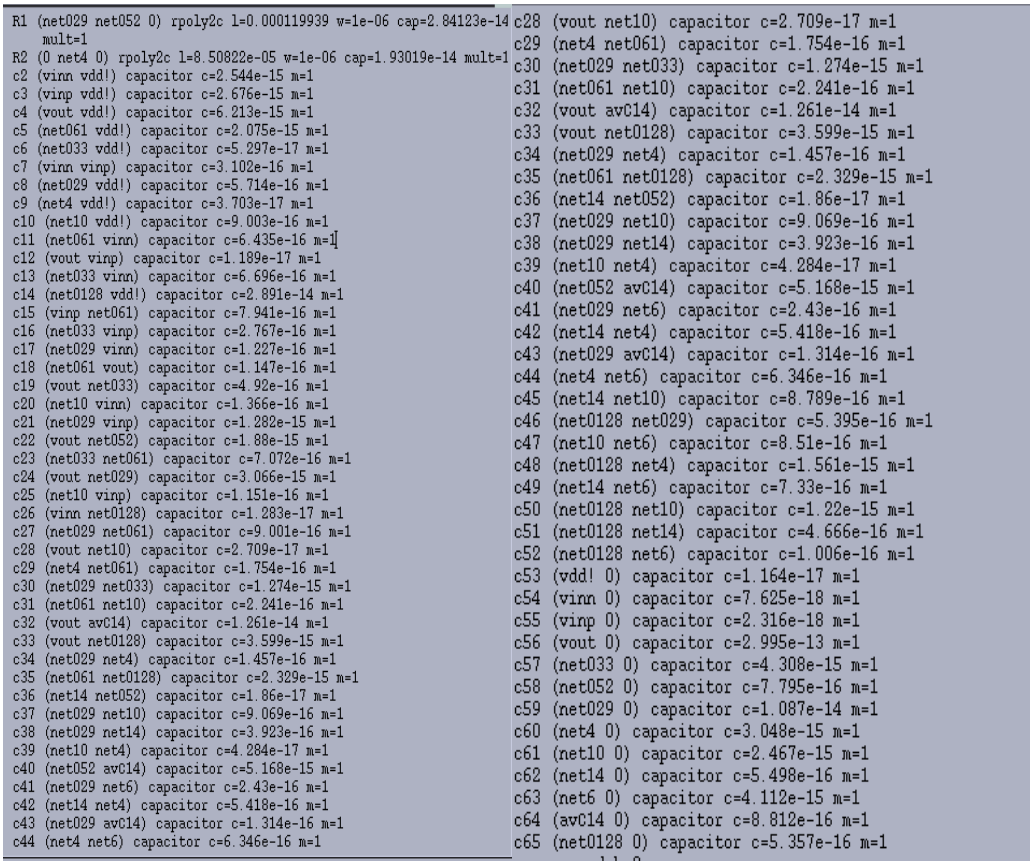


Figure 3.15: Extracted graph of layout.

We can examine the netlist in order to look at values of extracted parasitic capacitances and determine largest values in them. As seen in Fig.3.15 layout contains lots of small parasitic capacitances that derives from interconnects and source/drain areas, affects performance of circuit by changing dc operating points of transistors and frequency response of circuit.



```
R1 (net029 net052 0) rpoly2c l=0.000119939 w=1e-06 cap=2.84123e-14
    mult=1
R2 (0 net4 0) rpoly2c l=8.50822e-05 w=1e-06 cap=1.93019e-14 mult=1
c2 (vinn vdd!) capacitor c=2.544e-15 m=1
c3 (vinp vdd!) capacitor c=2.676e-15 m=1
c4 (vout vdd!) capacitor c=6.213e-15 m=1
c5 (net061 vdd!) capacitor c=2.075e-15 m=1
c6 (net033 vdd!) capacitor c=5.297e-17 m=1
c7 (vinn vinp) capacitor c=3.102e-16 m=1
c8 (net029 vdd!) capacitor c=5.714e-16 m=1
c9 (net4 vdd!) capacitor c=3.703e-17 m=1
c10 (net10 vdd!) capacitor c=9.003e-16 m=1
c11 (net061 vinn) capacitor c=6.435e-16 m=1
c12 (vout vinp) capacitor c=1.189e-17 m=1
c13 (net033 vinn) capacitor c=6.696e-16 m=1
c14 (net0128 vdd!) capacitor c=2.891e-14 m=1
c15 (vinp net061) capacitor c=7.941e-16 m=1
c16 (net033 vinp) capacitor c=2.767e-16 m=1
c17 (net029 vinn) capacitor c=1.227e-16 m=1
c18 (net061 vout) capacitor c=1.147e-16 m=1
c19 (vout net033) capacitor c=4.92e-16 m=1
c20 (net10 vinn) capacitor c=1.366e-16 m=1
c21 (net029 vinp) capacitor c=1.282e-15 m=1
c22 (vout net052) capacitor c=1.88e-15 m=1
c23 (net033 net061) capacitor c=7.072e-16 m=1
c24 (vout net029) capacitor c=3.066e-15 m=1
c25 (net10 vinp) capacitor c=1.151e-16 m=1
c26 (vinn net0128) capacitor c=1.283e-17 m=1
c27 (net029 net061) capacitor c=9.001e-16 m=1
c28 (vout net10) capacitor c=2.709e-17 m=1
c29 (net4 net061) capacitor c=1.754e-16 m=1
c30 (net029 net033) capacitor c=1.274e-15 m=1
c31 (net061 net10) capacitor c=2.241e-16 m=1
c32 (vout avC14) capacitor c=1.261e-14 m=1
c33 (vout net0128) capacitor c=3.599e-15 m=1
c34 (net029 net4) capacitor c=1.457e-16 m=1
c35 (net061 net0128) capacitor c=2.329e-15 m=1
c36 (net14 net052) capacitor c=1.86e-17 m=1
c37 (net029 net10) capacitor c=9.069e-16 m=1
c38 (net029 net14) capacitor c=3.923e-16 m=1
c39 (net10 net4) capacitor c=4.284e-17 m=1
c40 (net052 avC14) capacitor c=5.168e-15 m=1
c41 (net029 net6) capacitor c=2.43e-16 m=1
c42 (net14 net4) capacitor c=5.418e-16 m=1
c43 (net029 avC14) capacitor c=1.314e-16 m=1
c44 (net4 net6) capacitor c=6.346e-16 m=1
c45 (net14 net10) capacitor c=8.789e-16 m=1
c46 (net0128 net029) capacitor c=5.395e-16 m=1
c47 (net10 net6) capacitor c=8.51e-16 m=1
c48 (net0128 net4) capacitor c=1.561e-15 m=1
c49 (net14 net6) capacitor c=7.33e-16 m=1
c50 (net0128 net10) capacitor c=1.22e-15 m=1
c51 (net0128 net14) capacitor c=4.666e-16 m=1
c52 (net0128 net6) capacitor c=1.006e-16 m=1
c53 (vdd! 0) capacitor c=1.164e-17 m=1
c54 (vinn 0) capacitor c=7.625e-18 m=1
c55 (vinp 0) capacitor c=2.316e-18 m=1
c56 (vout 0) capacitor c=2.995e-13 m=1
c57 (net033 0) capacitor c=4.308e-15 m=1
c58 (net052 0) capacitor c=7.795e-16 m=1
c59 (net029 0) capacitor c=1.087e-14 m=1
c60 (net4 0) capacitor c=3.048e-15 m=1
c61 (net10 0) capacitor c=2.467e-15 m=1
c62 (net14 0) capacitor c=5.498e-16 m=1
c63 (net6 0) capacitor c=4.112e-15 m=1
c64 (avC14 0) capacitor c=8.812e-16 m=1
c65 (net0128 0) capacitor c=5.357e-16 m=1
```

Figure 3.16: Extracted Capacitances in Netlist.

As seen in Fig. 3.16, there are 65 extracted capacitances and most of them capacitances derived from layout are in the range $10^{-15} - 10^{-17}F$. Largest extracted capacitances are in the order of 10^{-13}F.

7. POST SIMULATION RESULTS

After layout design is completed, post layout simulations are conducted to determine the effect of parasitic capacitances on the opamp specifications.

7.1.Gain, GBW and Phase Margin:

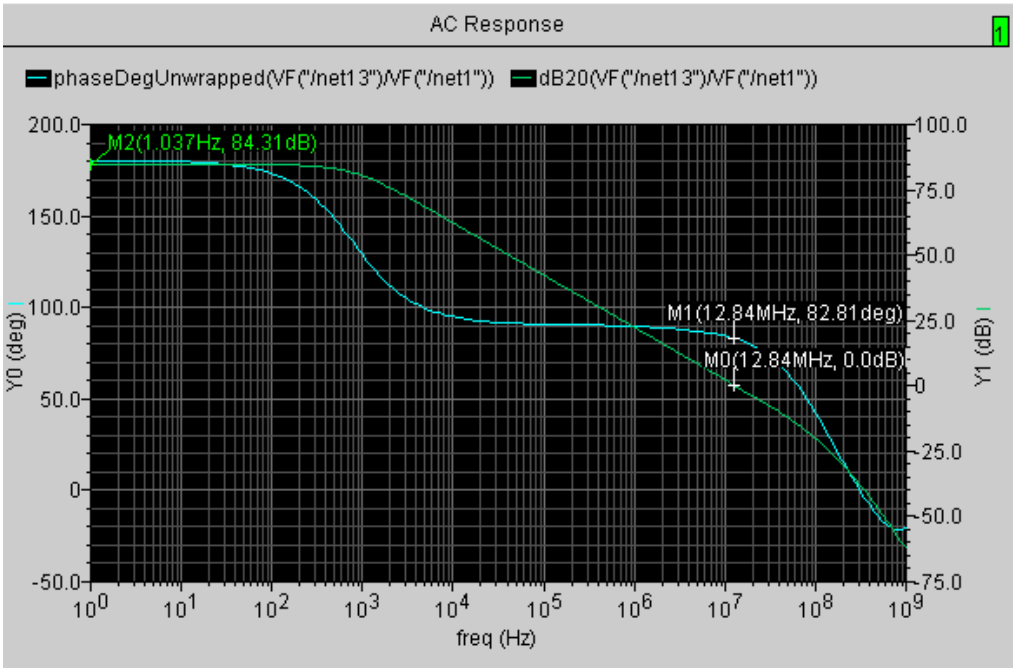


Figure 3.17: Frequency Response of two stage op-amp with extracted capacitances in layout.

As seen in Figure 3.17, dc gain of opamp with parasitic capasitances is 84.31dB which is 0.11dB is larger than schematic simulation and satisfy the design specification (>80dB). Unity gain frequency of opamp decreased to 12.84MHz when parasitic capacitances are considered. This value of f_t is roughly 1MHz lower than f_t found in schematic simulation. The decrease in the unity gain frequency derives from extracted capacitances values which affect the dc operating points of mosfets and lead to changes in mosfet small signal parameters. 12.84MHz unity gain frequency satisfies design constraints too. Also, in Fig.3.17 we see that Phase Margin of two stage opamp is 82.81degree which is approximately 3degree lower than the value found in schematic simulation. This value of phase margin is much larger than design constraint (>60degree).

7.2.Power Consumption

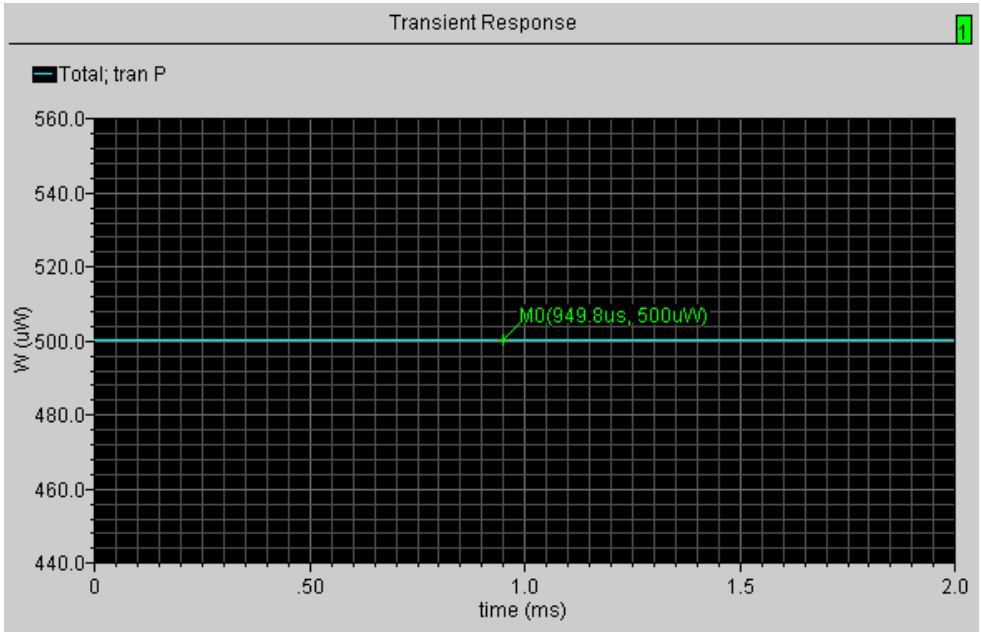


Figure 3.18: Power Dissipation of Opamp with extracted capacitances.

As seen in *Fig.3.18*, power dissipation of circuit is exactly 500uW, in other words it is in the boundary of design specification. The value of power dissipation of opamp is roughly 20uW larger than the schematic result.

7.3.Slew Rate

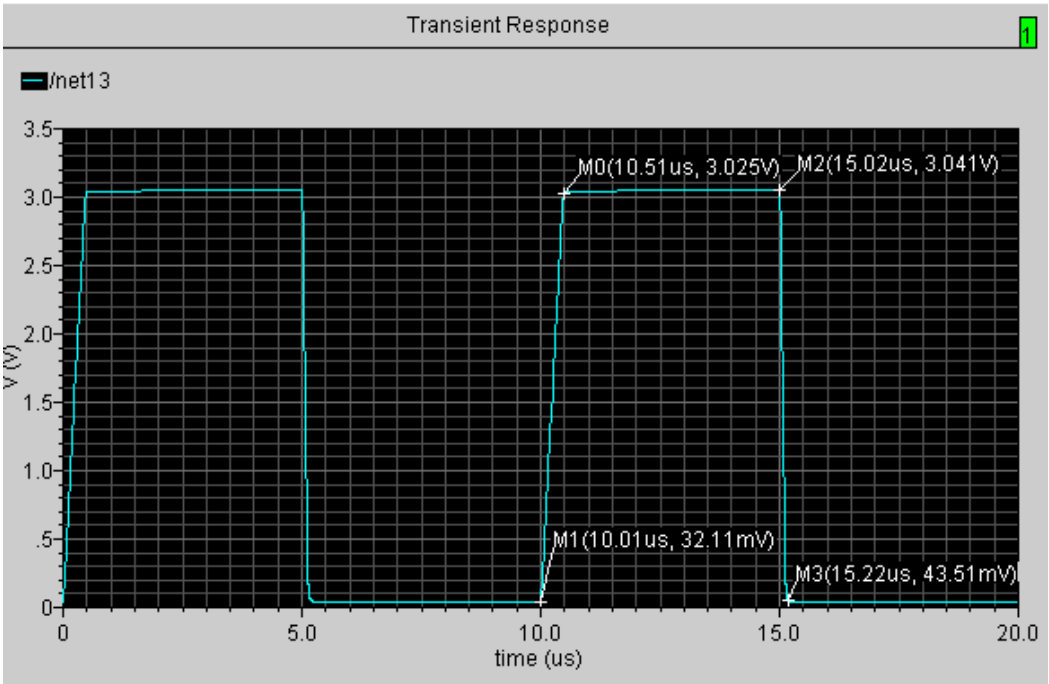


Figure 3.18: Rising and Falling Edge Slew Rate

According to Fig.3.18, SR for rising and falling edges can be calculated as follow:

$$Rising\ Edge\ SR = \frac{3.025V - 32.11mV}{(10.51 - 10.01)us} = 5.986V/us$$

$$Falling\ Edge\ SR = \frac{3.041V - 43.51mV}{(15.02 - 15.22)us} \cong 14.99V/us$$

Another way to detect SR in rising and falling edges is to check derivative of waveform in *Fig.3.18* and this way is depicted in *Fig.3.19.*

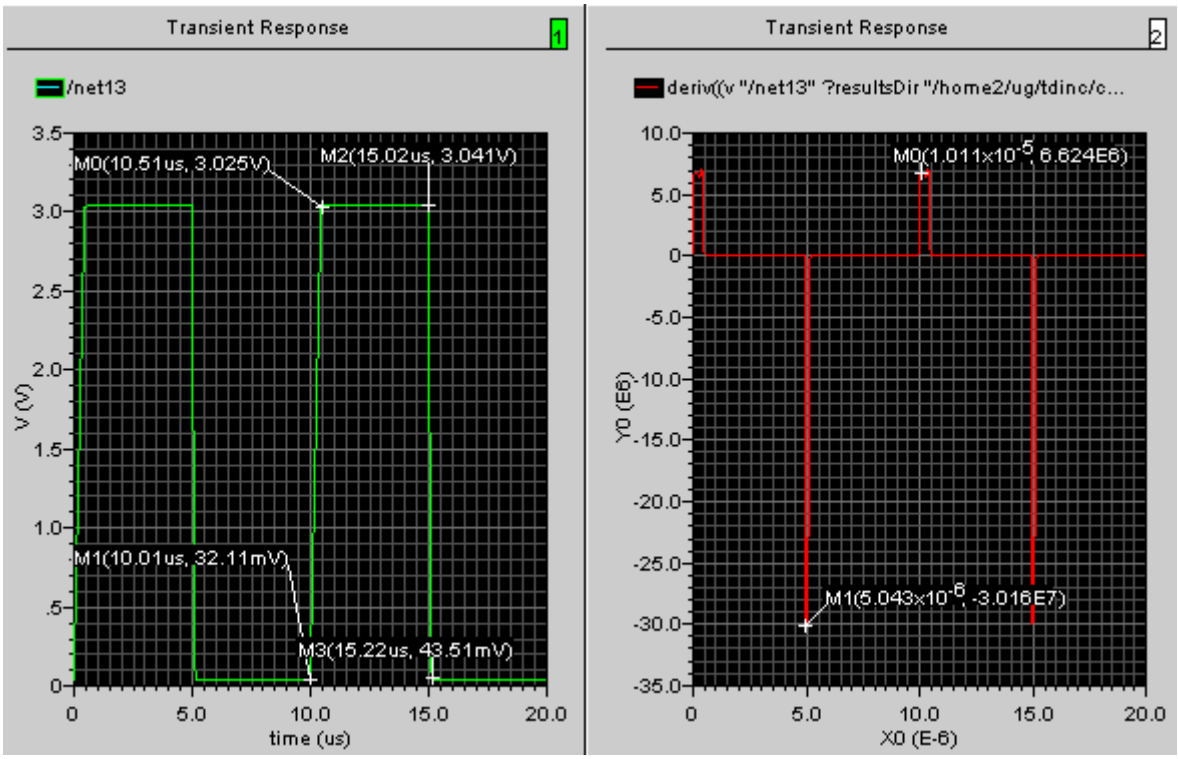


Figure 3.18: Response of opamp to pulse signal and derivative of it.

Pulses in the derivative of periodic square wave signal gives us to slopes in the rising and falling edges which are equal to our rising edge SR and falling edge SR respectively. Therefore according to Fig.3.18, Rising Edge SR of opamp when extracted capacitances are considered is 6.624V/us and Falling Edge SR is -30V/us which are more reliable datas then the calculations we made above. Thus rising edge slew rate 1V/us lower than schematic results whereas falling edge SR is 2V/us lower than the value found in schematic simulations.

7.4. $PSRR_{DD}$

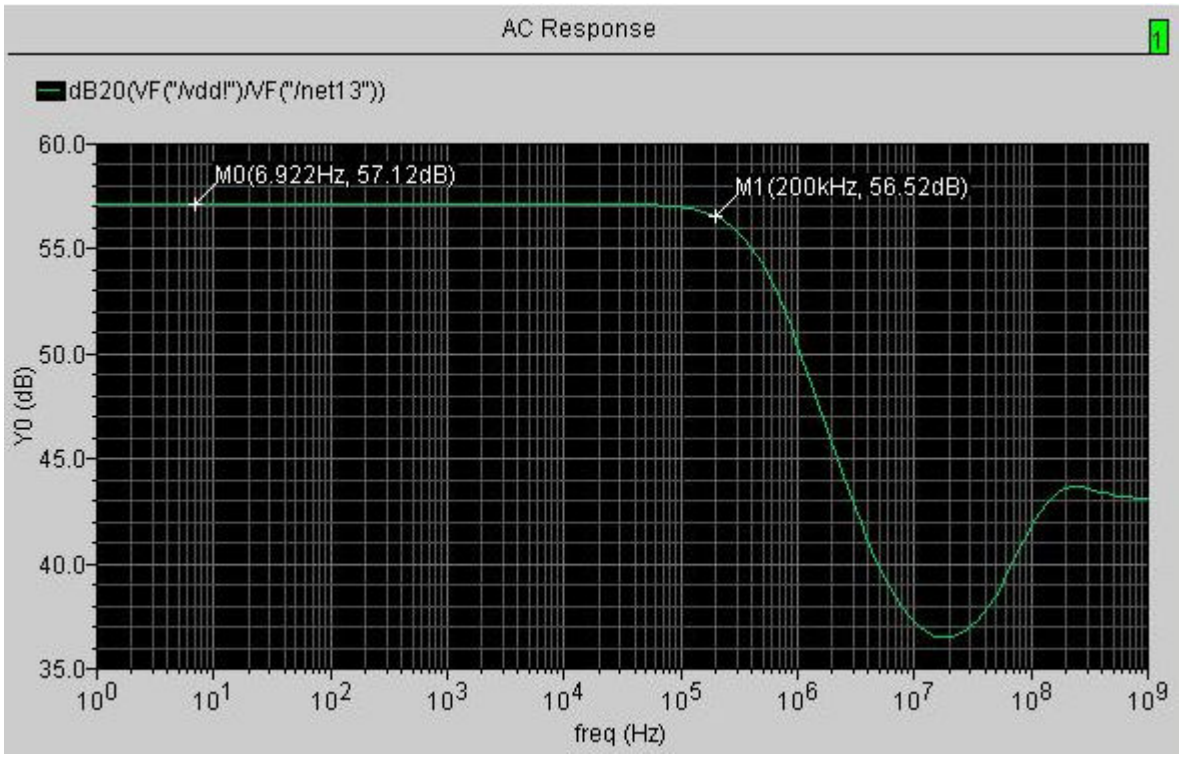


Figure 3.19: PSRRdd response of opamp with extracted capacitances.

In post layout simulation for $PSRR_{DD}$ in Fig.3.19, it is obvious that out PSRR value is around 57.12dB for frequencies close to zero and it is 56.52dB at 200kHz. We had found PSRR as 56.35dB in schematic simulations.

7.5.Output Voltage Swing

In order to increase output voltage swing we should bias the output node of circuit so that it is around 1.65V . In order to accomplish this, I gave a variable to amplitude of sinusoidal signal and conduct a DC sweep analysis to find out necessary VCM value to be given to input terminal. At the end of analysis VCM found as 1.024V.

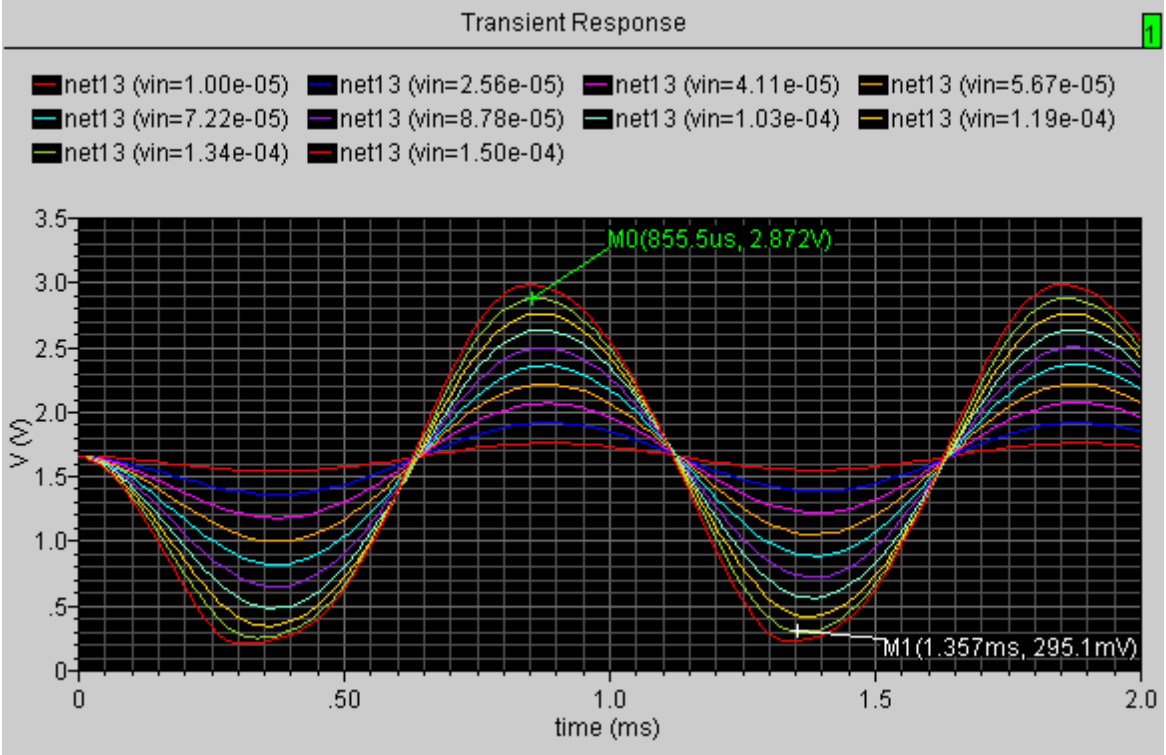


Figure3.20 Output Swing of Opamp (Lay out)

As seen in Fig.3.20, maximum output voltage swing is from 0.295V to 2.872V and voltage head room and legroom of output signal is nearly equal. Also notice than ac signals swing on roughly 1.65V DC voltage.

CONCLUSION:

	Handcalculations	Simulation Results	Specifications	Post Layout	% LVS
Av	**88.23**	**84.2**	**>80dB**	**84.31dB**	**0.1**
Unity Gain Freq.	**15.92Mhz**	**13.81Mhz**	**>10Mhz**	**12.84Mhz**	**7.8**
PM	**69degree**	**86degree**	**>60degree**	**82.81degree**	**3.8**
SR	**20V/us**	**7.63V/us**	**>5V/us**	**6.624V/us**	**15.1**
Ptot	**462uW**	**Around 480uW**	**<500uW**	**500uW**	**4**
PSRRdd	**-**	**56.35dB**	**>40db**	**56.52**	**0.3**
Output Swing	**0.2V to 3.1V**	**0.298V to 2.865V**		**0.295-2.872**	**0.6**

Comparation of values found during handcalculation, schematic simulations , post layout simulations is shown above. As seen in table, all the specifications given are satisfied. Also notice that, most deviation between layout and schematic occurs at SR.