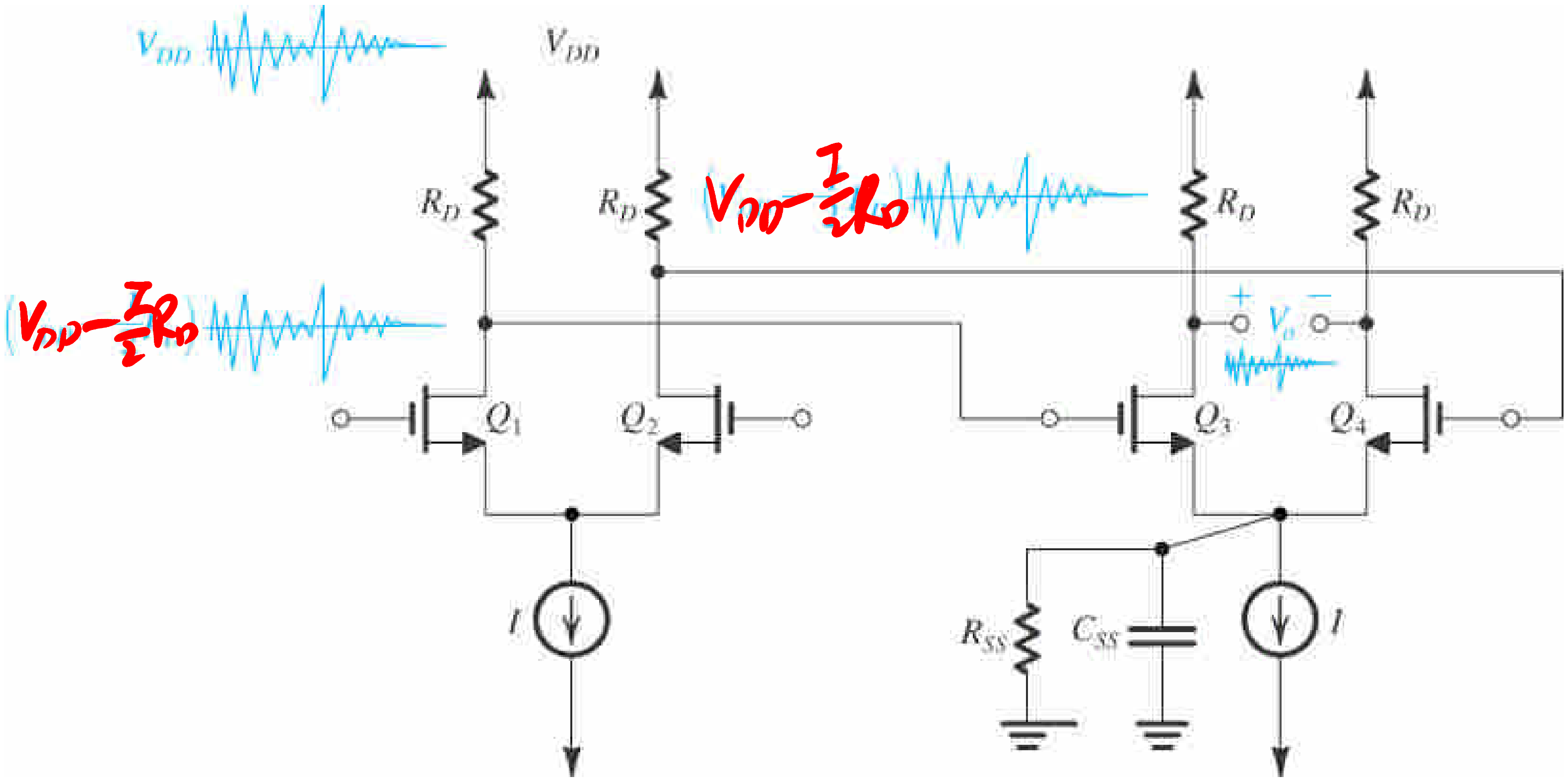
CHAPTER 7

Differential and Multistage Amplifiers

Outline

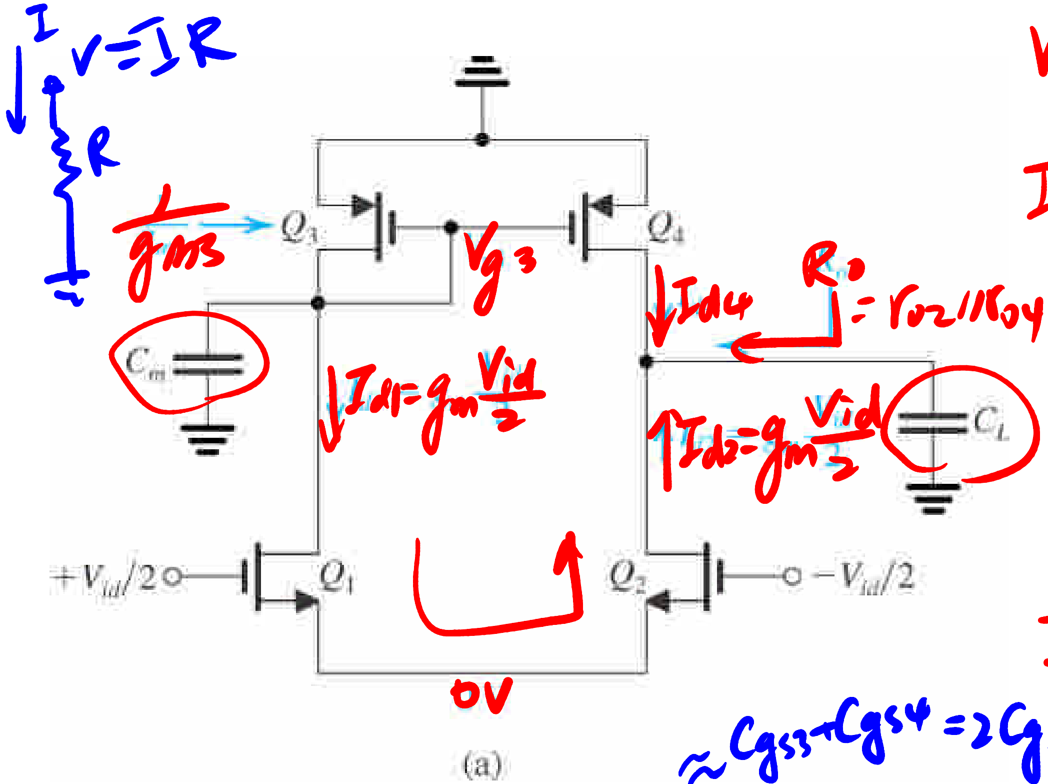
- The MOS Differential Pair
- Small-Signal Operation of the MOS Differential Pair
- The BJT Differential Pair
- Other Nonideal Characteristics of the Differential Amplifier
- The Differential Amplifier with Active Load
- **Frequency Response of the Differential Amplifier**
- Multistage Amplifiers

High CMRR at Higher Frequencies



Active-Loaded MOS Amplifier

$$f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})} \approx \frac{g_m}{2\pi C_{gs}}$$



$$V_{g3} = -g_m \cdot \frac{V_{id}}{2} \cdot \frac{1}{g_{m3} + sC_m}$$

$$I_{d4} = -g_{m4} V_{g3} = \frac{g_m \cdot \frac{V_{id}}{2}}{1 + s\frac{C_m}{g_{m3}}}$$

$$f_{p2} = \frac{g_m}{2\pi \cdot (2C_{gs3})} = \frac{f_T}{2}$$

$$I_o = I_{d2} + I_{d4} = g_m \cdot \frac{V_{id}}{2} + \frac{g_m \cdot \frac{V_{id}}{2}}{1 + s\frac{C_m}{g_{m3}}}$$

$$V_o = I_o \cdot \frac{1}{\frac{1}{R_o} + sC_L}$$

$$A_d = \frac{V_o}{V_{id}} = (g_m R_o)\left(\frac{1}{1 + sC_L R_o}\right)\left(\frac{1 + s\frac{C_m}{2g_{m3}}}{1 + s\frac{C_m}{g_{m3}}}\right)$$

dc gain, f_{p1}, f_z, f_{p2}

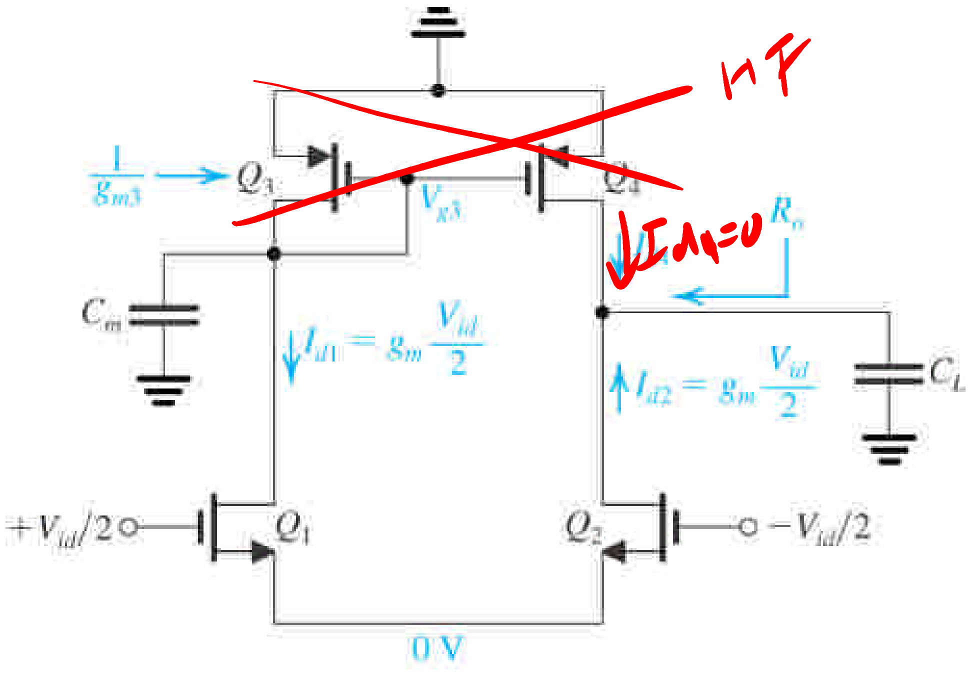
$$C_m = C_{gd1} + C_{db1} + C_{db3} + C_{gs3} + C_{gs4}$$

$$\approx C_{gs3} + C_{gs4} = 2C_{gs3}$$

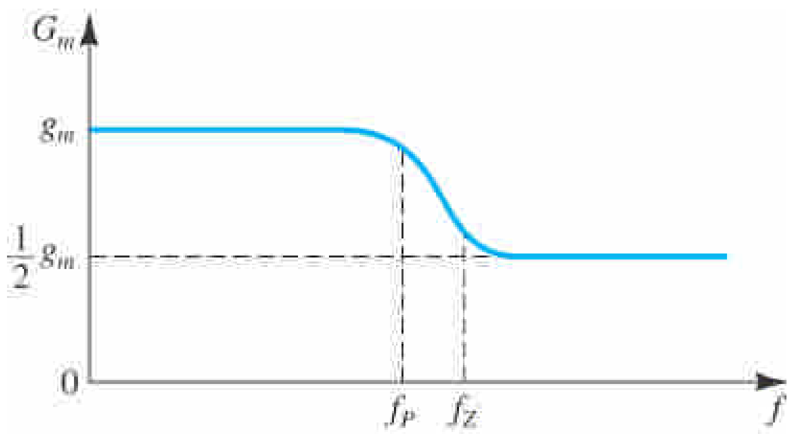
$$C_L = C_{gd2} + C_{db2} + C_{gd4} + C_{db4} + C_x$$

$$f_{p1} = \frac{1}{2\pi C_L R_o}, \quad f_{p2} = \frac{g_{m3}}{2\pi C_m}, \quad f_z = \frac{2g_{m3}}{2\pi C_m}$$

C_m on Transconductance G_m



(a)

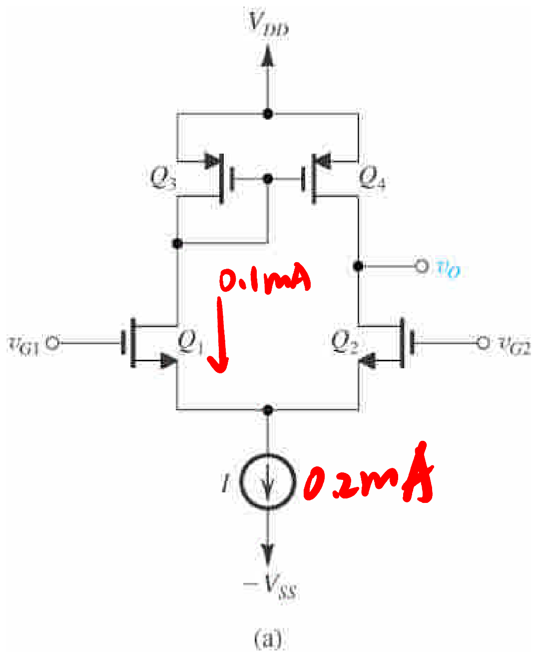


(b)

Low Freq: $G_m = g_m$

High Freq: $G_m = \frac{1}{2} g_m$

Example 7.2



To find:
A_d, A_{cm}, CMRR
Poles and zeros of A_d
Dominant pole of CMRR

Q_3, Q_4: $V_{ov} = 0.34V$, $g_m = 0.6\, mA/V$, $r_o = 21.6k\Omega$

Q_1, Q_2: $100 = \frac{1}{2} \cdot 387 \cdot \frac{7.2}{0.36} \cdot V_{ov}^2$

$\Rightarrow V_{ov} = 0.16\,V$

$g_{m1} = g_{m2} = \frac{2 \times 0.1}{0.16} = 1.25\left(\frac{mA}{V}\right)$

$r_{o1} = r_{o2} = \frac{5 \times 0.36}{0.1} = 18k\Omega$

Low Freq.

$A_d = g_m(r_{o2} // r_{o4}) = 12.3 (V/V)$

$A_{cm} = -\frac{1}{2 g_{m3} R_{SS}} = -0.033$

CMRR = 369 = 51.3 dB

$C_m = 55fF$
$C_L = 45fF$

$f_{p1} = 360\,MHz$
$f_{p2} = 1.74\,GHz$
$f_z = 3.5\,GHz$

W/L = 7.2µm/0.36µm, C_{gs} = 20fF
C_{gd} = 5fF, C_{db} = 5fF, $\mu_n C_{ox}$ = 387µA/V^2
$\mu_p C_{ox}$ = 86µA/V^2, V_{An}' = 5V/µm, $|V_{Ap}'|$ = 6V/µm
I = 0.2mA, R_{ss} = 25kΩ, C_{ss} = 0.2pF
Another output capacitance C_x = 25fF

$f_z = \frac{1}{2\pi C_{SS} R_{SS}} = 31.8\,MHz$

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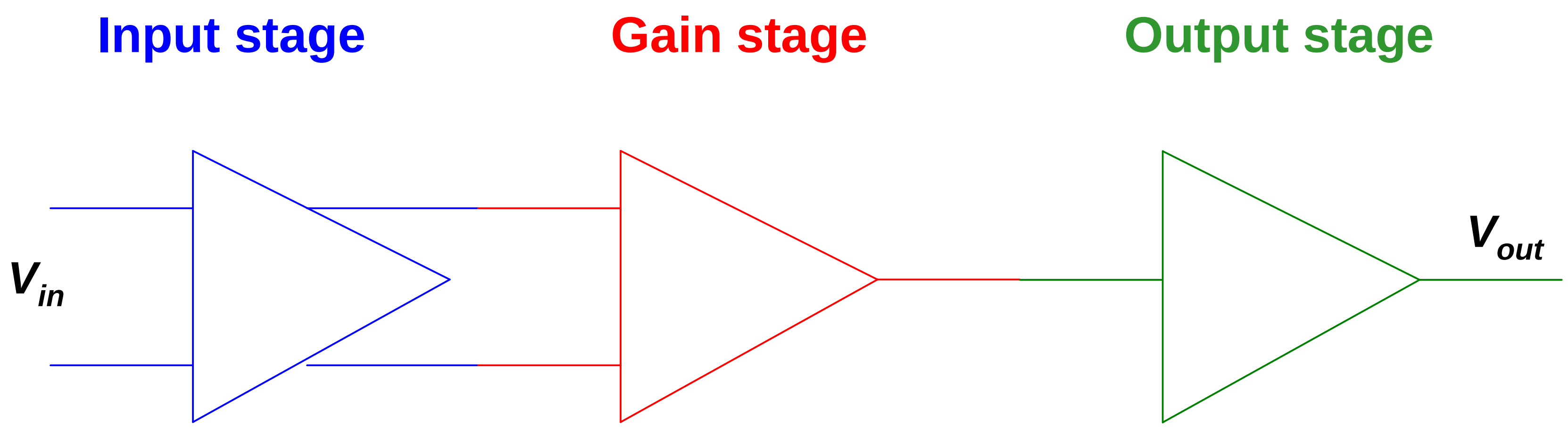
Multistage Amplifiers

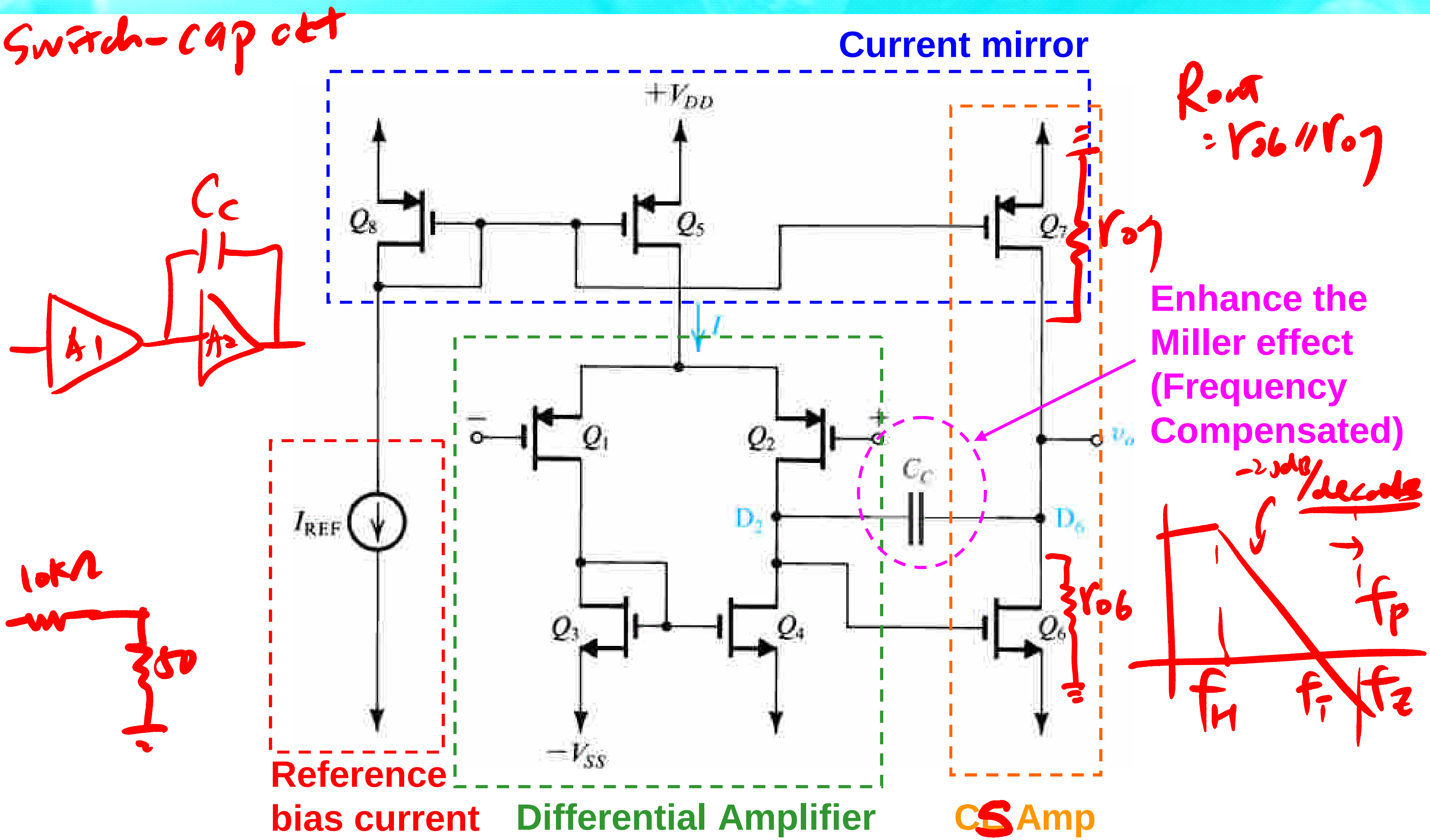


First stage:
-High input resistance
-Large CMRR
-Voltage gain

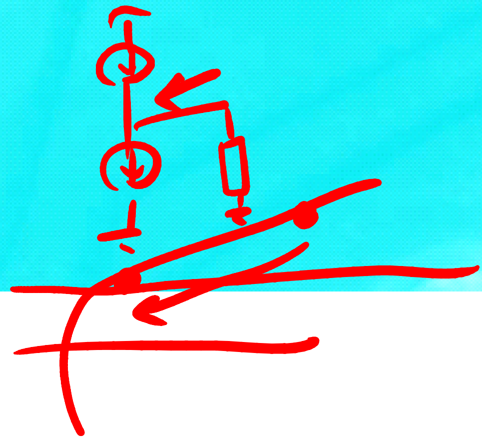
Middle stages:
-Voltage gain
-Differential to Single-ended
-DC-level shifting

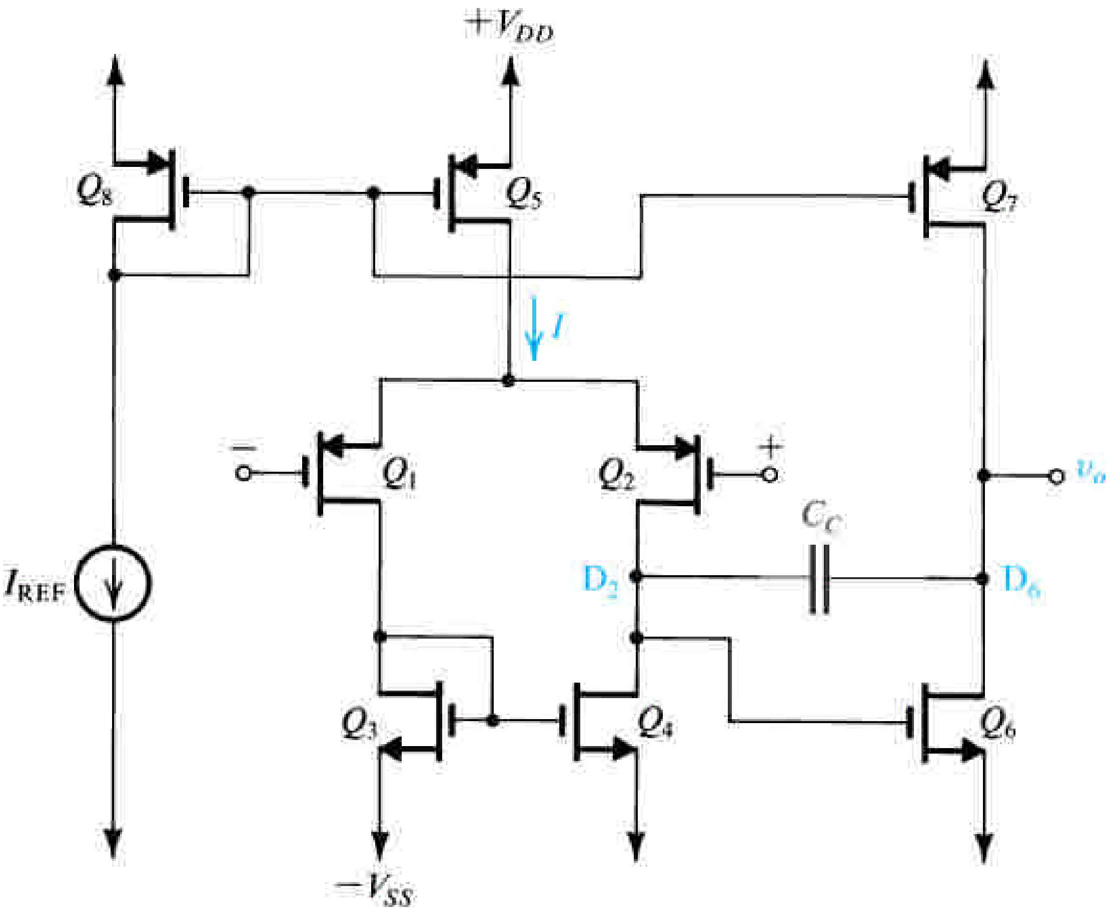
Last stage:
-Low output resistance
-Supply current efficiently

A Two-Stage CMOS Op Amp



Voltage Gain





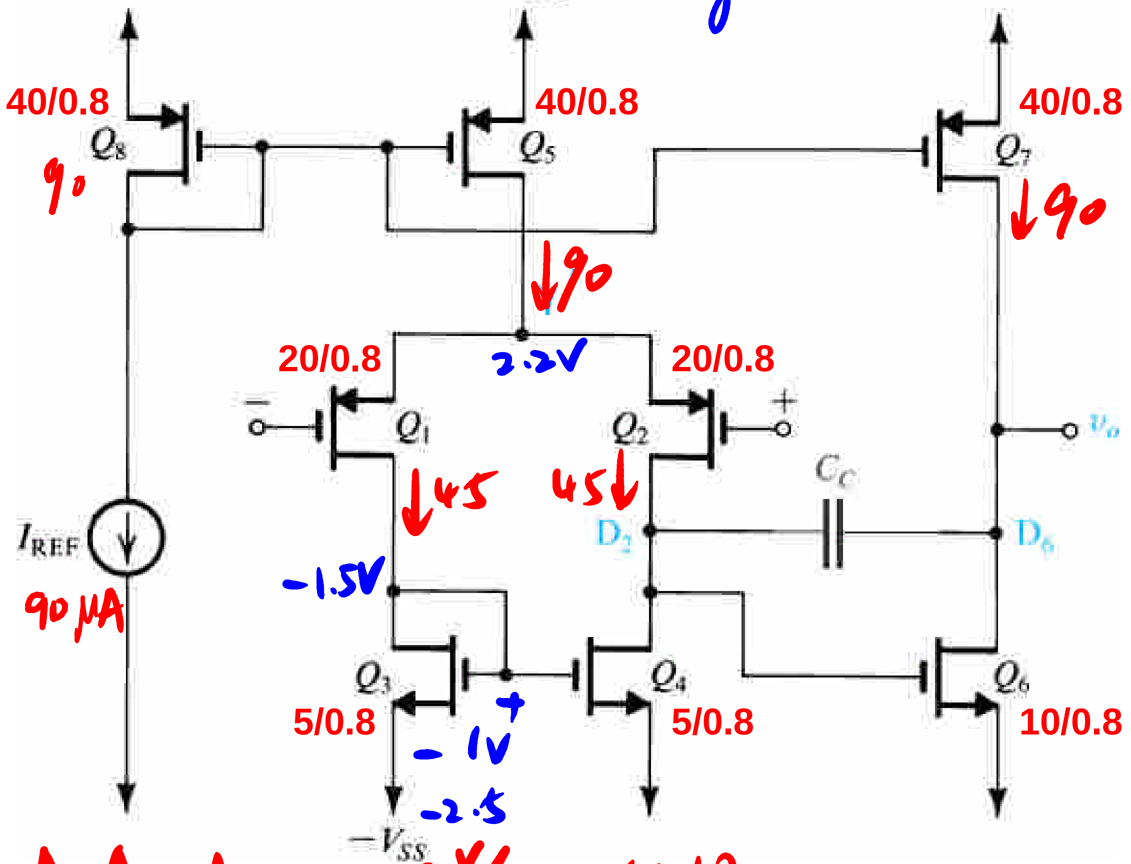
$A_1 = -g_{m1}(r_{o2} // r_{o4})$

$A_2 = -g_{m6} \cdot (r_{o6} // r_{o7})$

$A = A_1 \cdot A_2$

Example 7.3

Input common mode range < Lower = -1.5 - 0.8 = -2.3V ; Higher = 2.2 - 1.1 = 1.1V



$A = A_1 \times A_2 = 1109 (V/V) = 61dB$

I_{REF} = 90μA, V_{tn} = 0.7V, V_{tp} = -0.8V, $\mu_n C_{ox}$ = 160μA/V², $\mu_p C_{ox}$ = 40μA/V², $|V_A|$ = 10V, $V_{DD} = V_{ss}$ = 2.5V

V_{GS} = 1.1V for Q1.2.5.7.8
1V for Q3.4.6

(a) I_D

(b) $|V_{OV}|$ — $I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}V_{ov}^2$ (0.3V)

(c) $|V_{GS}|$ — $|V_{GS}| - |V_t| = |V_{ov}|$

(d) g_m — $2I_D/|V_{ov}|$ — 0.3mA/V Q1-4; 0.6 Q5-8

(e) r_o — $|V_A|/I_D$

(f) A_1 — -33.3 (V/V) — 222kΩ Q1-Q4

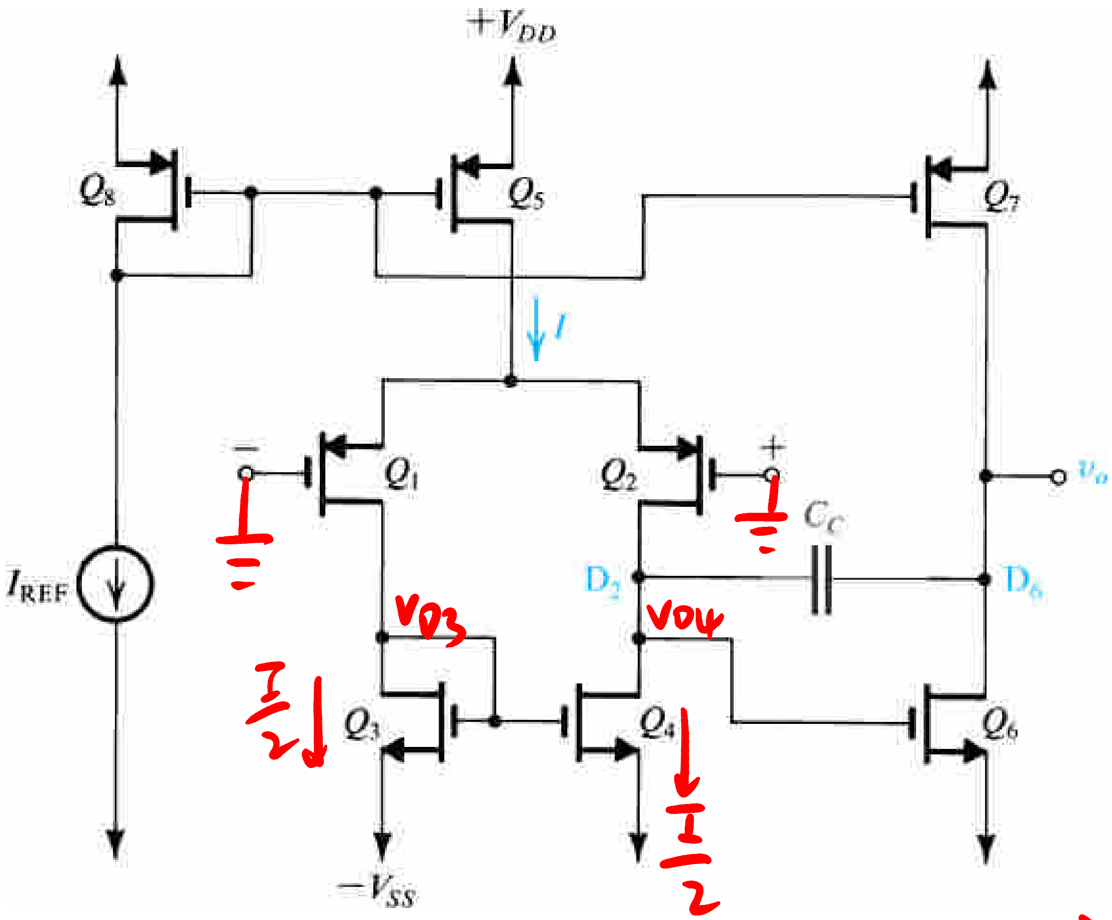
(g) A_2 — 111kΩ Q5-Q8

(h) Input common-mode range

(i) Output voltage range

-2.2V — 2.2V

Input Offset Voltage



Random offset

- *W/L*
- V_t

Systematic offset

$$V_{D3} = V_{D4} = -V_{SS} + V_{GS4} = V_{G6}$$

$$\Rightarrow V_{GS6} = V_{GS4}$$

$$I_6 = \frac{(W/L)_6}{(W/L)_4}\frac{I}{2}$$

$$I_7 = \frac{(W/L)_7}{(W/L)_8}\cdot I = \frac{(W/L)_7}{(W/L)_5} I$$

$$\Rightarrow \frac{(W/L)_6}{(W/L)_4} = 2\frac{(W/L)_7}{(W/L)_5}$$

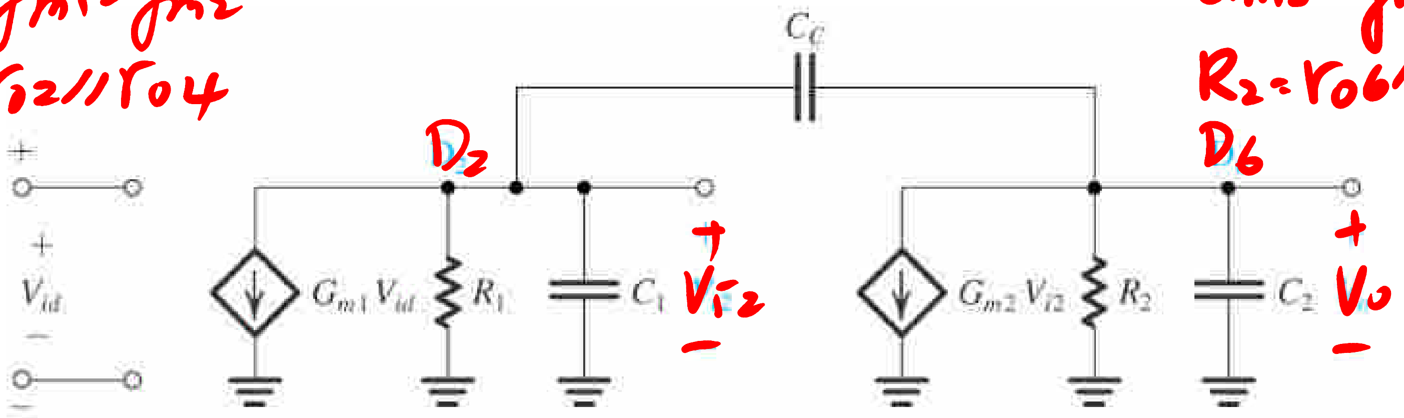
Frequency Response

$G_{m1} = g_{m1} = g_{m2}$

$R_1 = r_{o2} // r_{o4}$

$G_{m2} = g_{m6}$

$R_2 = r_{o6} // r_{o7}$



C_1 = $C_{gd4} + C_{db4} + C_{gd2} + C_{db2} + C_{gs6}$

C_2 = $C_{db6} + C_{db7} + C_{gd7} + \underline{C_L}$

Node D_2 $G_{m1}V_{id} + \frac{V_{i2}}{R_1} + sC_1V_{i2} + sC_C(V_{i2} - V_o) = 0$

Node D_6 $G_{m2}V_{i2} + V_o/R_2 + sC_2V_o + sC_C(V_o - V_{i2}) = 0$

$$\frac{V_o}{V_{id}} = \frac{G_{m1}(G_{m2} - sC_C)R_1R_2}{1 + s[C_1R_1 + C_2R_2 + C_C(G_{m2}R_1R_2 + R_1 + R_2)] + s^2[C_1C_2 + C_C(C_1 + C_2)]R_1R_2}$$

Frequency Response (con't)

$$\frac{V_o}{V_{id}} = \frac{G_{m1}\left(G_{m2} - sC_C\right)R_1R_2}{1 + s\left[C_1R_1 + C_2R_2 + C_C\left(G_{m2}R_1R_2 + R_1 + R_2\right)\right] + s^2\left[C_1C_2 + C_C\left(C_1 + C_2\right)\right]R_1R_2}$$

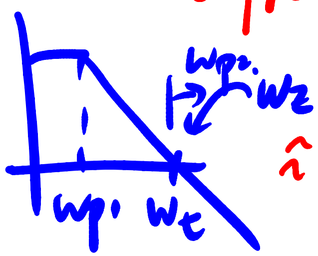
1) For $s=0$ $\quad V_o/V_{id} = (G_{m1}\cdot R_1)\cdot(G_{m2}\cdot R_2)$

2) W_Z. $\quad G_{m2} - s_Z C_c = 0 \Rightarrow S_Z = G_{m2}/C_c$

3) $D(s) = \left(1+\frac{s}{w_{p1}}\right)\left(1+\frac{s}{w_{p2}}\right) = 1 + s\left(\frac{1}{w_{p1}}+\frac{1}{w_{p2}}\right) + \frac{s^2}{w_{p1}w_{p2}} \approx 1 + \frac{s}{w_{p1}} + \frac{s^2}{w_{p1}w_{p2}}$

$\Rightarrow w_{p1} = \frac{1}{C_1R_1 + C_2R_2 + C_c(G_{m2}R_1R_2 + R_1 + R_2)} = \frac{1}{R_1\left[C_1 + C_c(1+G_{m2}R_2)\right] + R_2(C_2 + C_c)}$

Miller



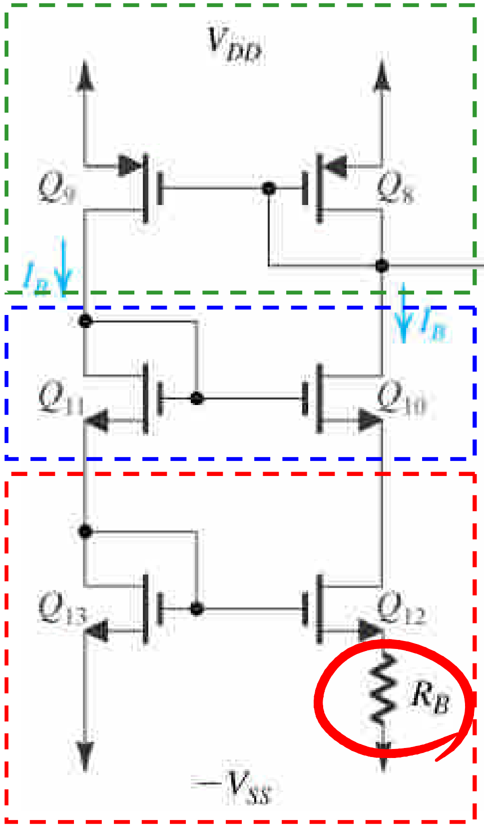
$\approx \frac{1}{R_1C_cG_{m2}R_2}$

$w_t = w_{p1}\cdot(G_{m1}R_1G_{m2}R_2) = \frac{G_{m1}}{C_c}$

$\Rightarrow w_{p2} = \frac{G_{m2}C_c}{C_1C_2 + C_c(C_1+C_2)}$ $\quad C_1 \ll C_2 \quad C_1 \ll C_c \quad \frac{G_{m2}}{C_2}$

$\omega_Z = G_{m2}/C_c$ $\qquad \omega_{P1} = \frac{1}{R_1C_cG_{m2}R_2}$ $\qquad \omega_{P2} = \frac{G_{m2}}{C_c}$

A Bias Circuit



$$I_B = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{12}(V_{GS12}-V_t)^2 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{13}(V_{GS13}-V_t)^2$$

$$V_{GS13} = V_{GS12} + I_B R_B$$

$$\Rightarrow I_B = \frac{2}{\mu_n C_{ox}\left(\frac{W}{L}\right)_{12} R_B^2}\left(\sqrt{\frac{(W/L)_{12}}{(W/L)_{13}}}-1\right)^2$$

$$\Rightarrow R_B = \frac{2}{\sqrt{\mu_n C_{ox}\left(\frac{W}{L}\right)_{12} I_B}}\cdot\left(\sqrt{\frac{(W/L)_{12}}{(W/L)_{13}}}-1\right)$$

g_{m12}

$$\Rightarrow g_{m12} = \frac{2}{R_B}\left(\sqrt{\frac{(W/L)_{12}}{(W/L)_{13}}}-1\right)$$

$$g_m \propto \sqrt{I_D\left(\frac{W}{L}\right)} \qquad g_{mi} = g_{m12}\sqrt{\frac{I_{Di}(W/L)_i}{I_B (W/L)_{12}}} \quad \text{NFET}$$

Announcements

- 下星期五(5/11)補課: 8AM
- HW #2 Exercise 7.2, 7.14, 7.17, 7.39, 7.40, 7.50, 7.63, 7.71, 7.80, 7.90
  - Due date 5/22/07
  - Late policy: Turn in class: 100%, before 12PM: 90%, 5/22 after 12AM: 80%, 5/23: 60%, 5/24: 40%, 5/25: 20%, after 5/26: 0%
- Midterm #2
  - Test date 5/15/07 ~~18:00-20:00~~ 19:00-21:00
  - Coverage: Ch6, Ch7, and a part of Ch8 (8.1-8.4)