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# ELE6308

## Microélectronique analogique et mixte

### --- Ampop avancés ---

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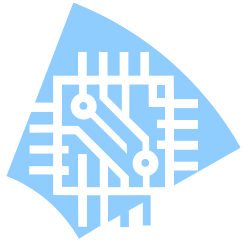
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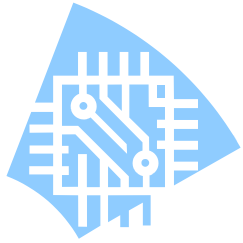


# Advanced Opamps Plan

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- I. Generality (CMRR, PSRR, ...)
- II. Input Common Mode Range
- III. Noise in CMOS Opamps
- IV. Cascodes amplifiers
- V. Telescopic Opamp
- VI. Gain boosted opamp
- VII. Folded cascode amplifier
- VIII. Class AB amplifier
- IX. Fully-differential Opamp.





# Advanced Opamps

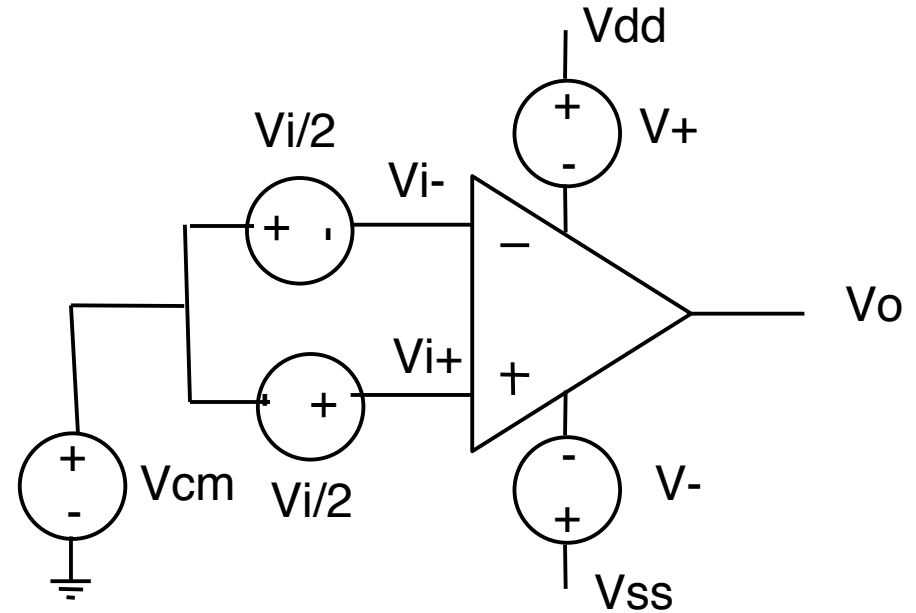
- **Generality**

$$v_i = v_i^+ - v_i^-$$

$$v_{cm} = \frac{v_i^+ + v_i^-}{2}$$

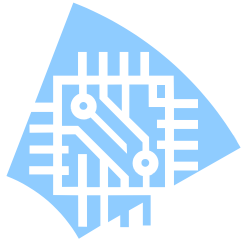
$$v_i^+ = v_{cm} + \frac{v_i}{2}$$

$$v_i^- = v_{cm} - \frac{v_i}{2}$$



$$v_O = A_{dm} v_i + A_{cm} v_{cm} + A^+ v^+ + A^- v^-$$



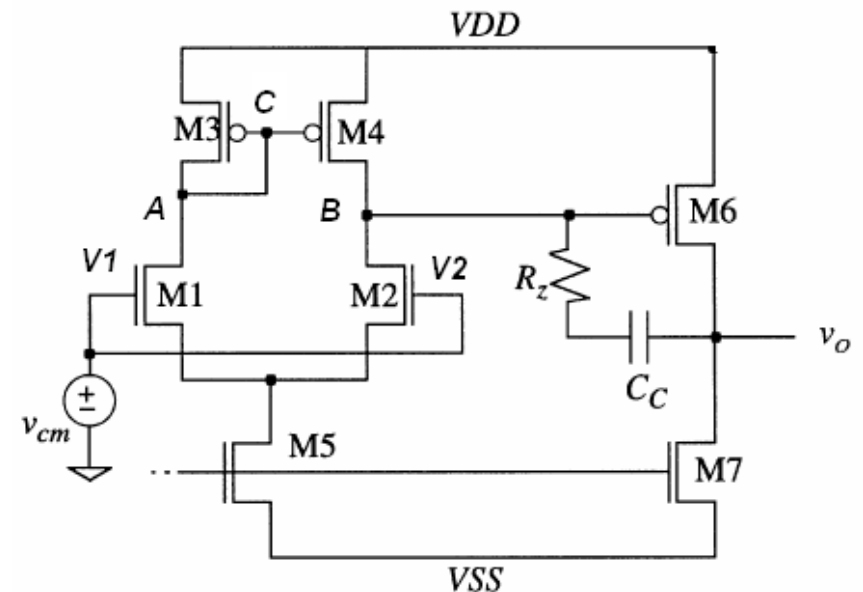


# CMRR

- The common-mode rejection ratio (CMRR) measures how well the amplifier can reject signals common to both inputs

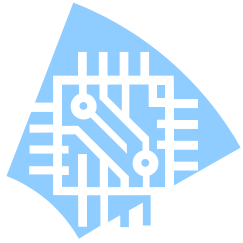
$$\text{CMRR} = 20 \log \left| \frac{A_{dm}}{A_{cm}} \right| = 20 \log \left| \frac{v_o / v_i}{v_o / v_{cm}} \right|$$

- The differential stage determines how well the entire opamp rejects common mode signals.



$$\text{CMRR}_{\text{Op Amp}} = \text{CMRR}_{\text{Input Stage}}$$





# CMRR (Cont'd)

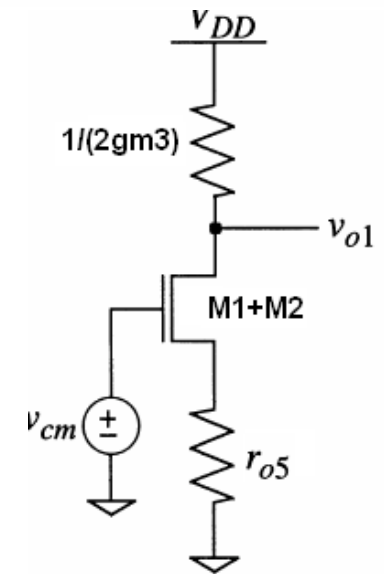
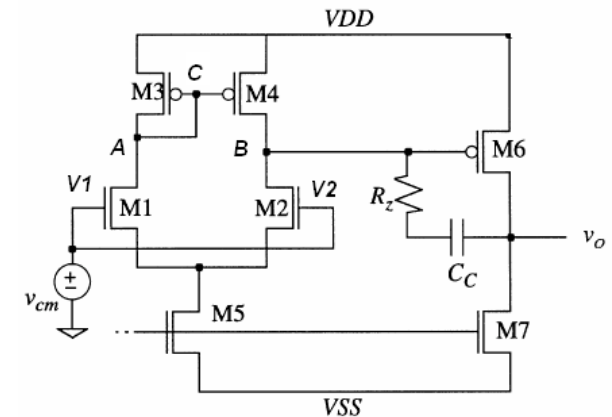
- The common-mode signal appearing on the drains of M3 and M4 will be identical

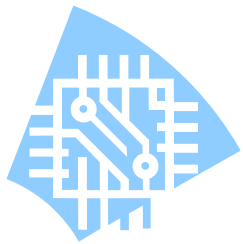
$$\frac{v_{o1}}{v_{cm}} = -\frac{1/g_{m3,4}}{2r_{o5}}$$

$$\text{CMRR} = 20\log\left|\frac{A_{dm}}{A_{cm}}\right| = 20\log\left|\frac{v_o/v_i}{v_o/v_{cm}}\right|$$

$$\text{CMRR} = 20\log(2g_{m1,2}g_{m3,4}(r_{o2}\parallel r_{o4})r_{o5})$$

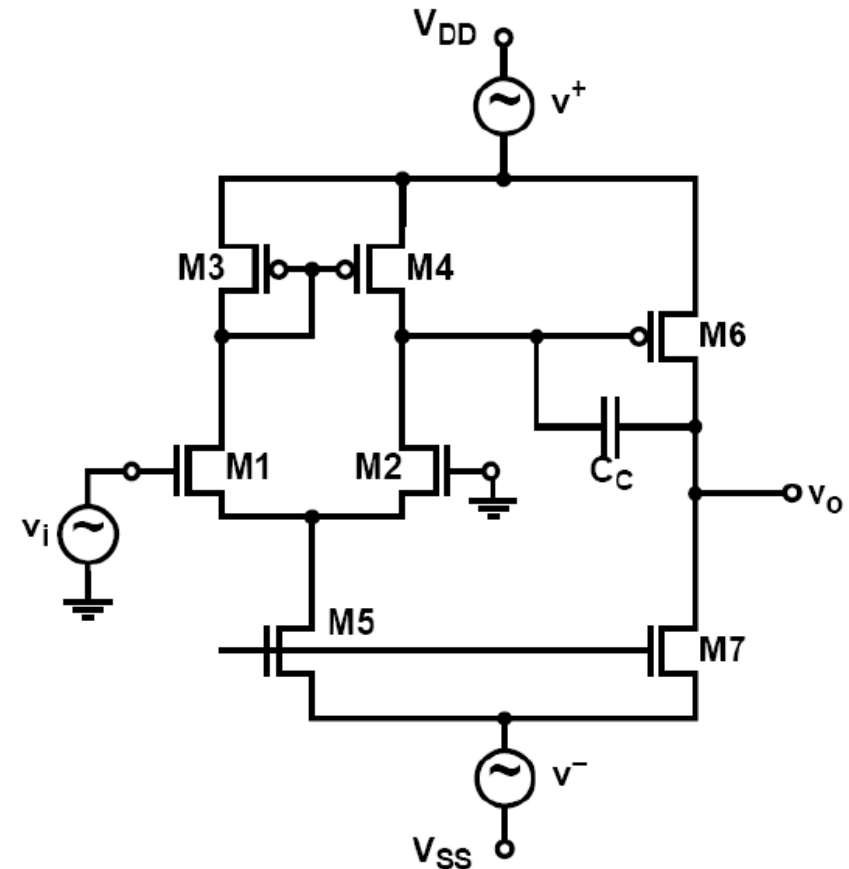
- The most efficient manner in which to increase the CMRR of this amplifier is to increase the resistance  $r_{o5}$

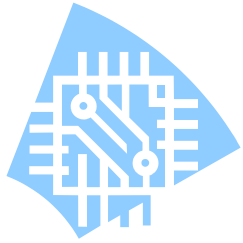




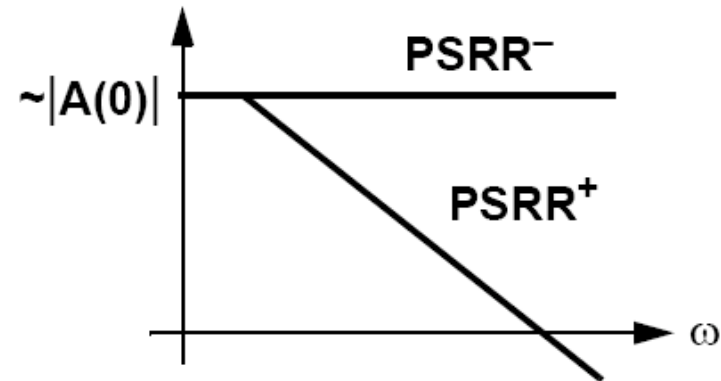
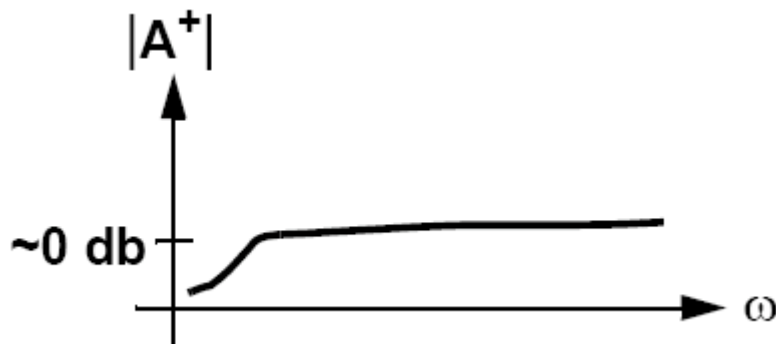
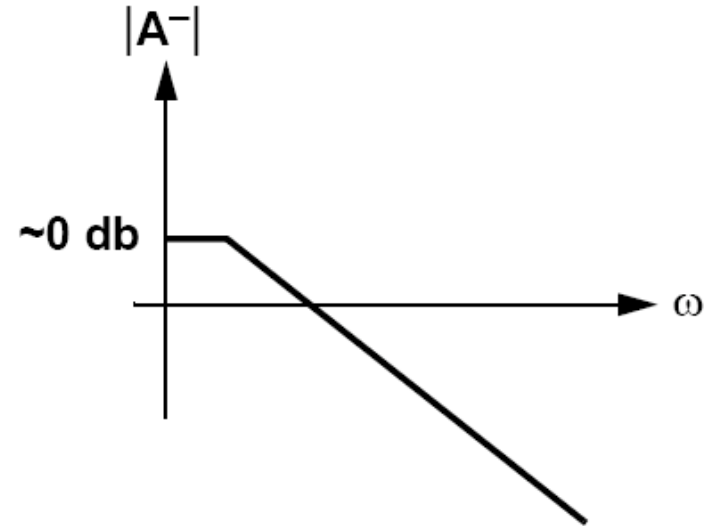
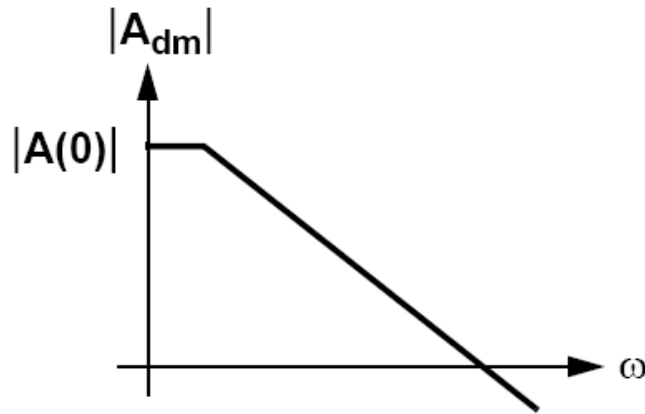
## PSRR of 2-Stage Opamp (cont'd)

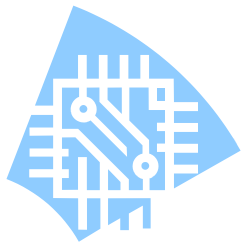
- $A^-$  is largely determined by  $g_{o5}$  &  $g_{o7}$ . It is typically  $\leq$  unity at low frequencies and, more importantly, it rolls off with frequency in the same fashion as the open loop gain.
- $PSRR^-$  remains approximately constant with frequency.
- $A^+ \approx 1$  except at very low frequencies
- $PSRR^+$  falls with frequency along with the open loop gain ( $A_{dm}$ ).
- At frequencies above the dominant pole (which is determined by  $C_C$ ),  $C_C$  “shorts” the gate and drain of M6.





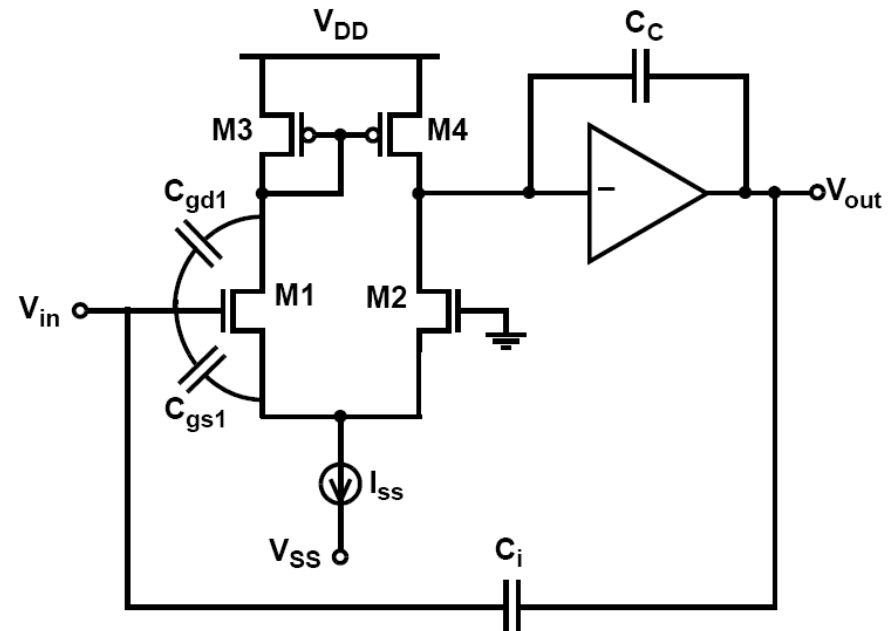
# PSRR of 2-Stage Opamp (cont'd)

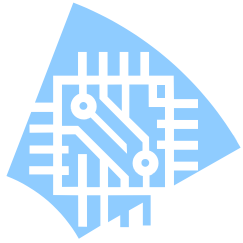




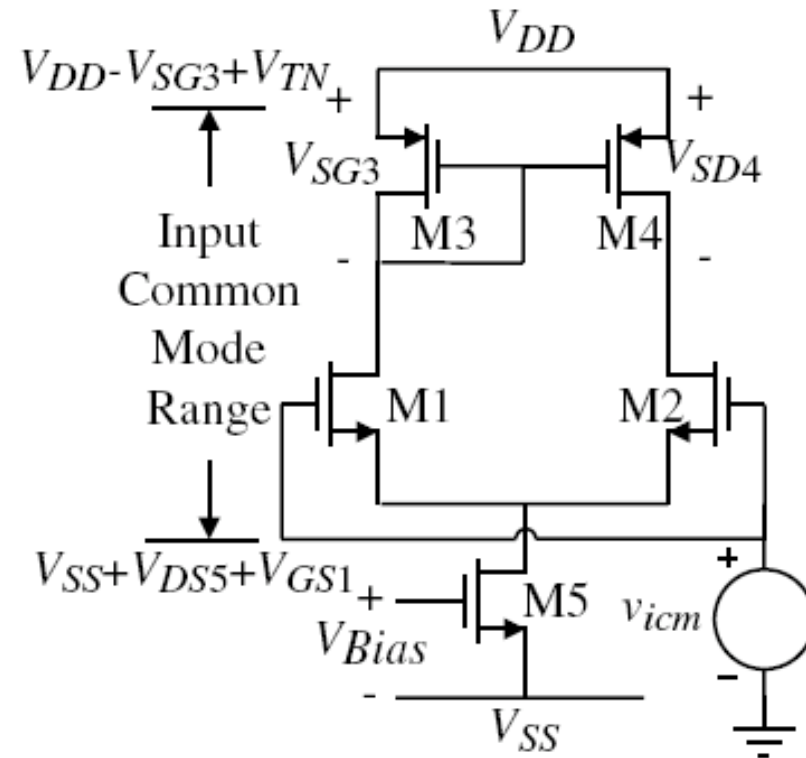
## PSRR of 2-Stage Opamp (cont'd)

- Another significant source of coupling between the supply rails and the output is commonly referred to as “supply” capacitance. This term refers to the coupling from one, or both, of the supply rails into the input nodes of an op amp. It is primarily in circuits such as single-ended sampled-data integrators
- The most important contributors to this type of coupling are displacement currents in the capacitances  $C_{gs1}$  and  $C_{gd1}$ . These currents flow into the summing node and the resulting charge is accumulated on the integration capacitor,  $C_i$ .
- Interconnect crossovers may also couple supply variations into the summing node.
- Fully differential circuits are an obvious means of avoiding the most severe supply capacitance problems.



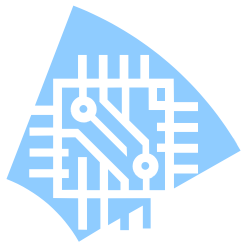


# Input Common Mode Range

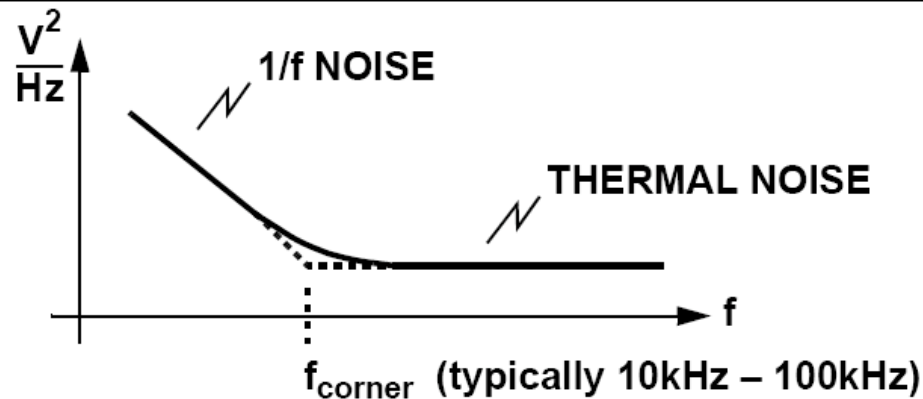


Differential amplifier with a current mirror load.

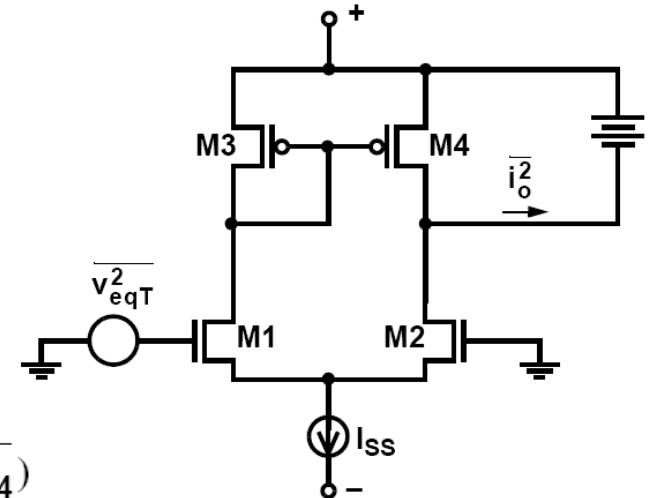
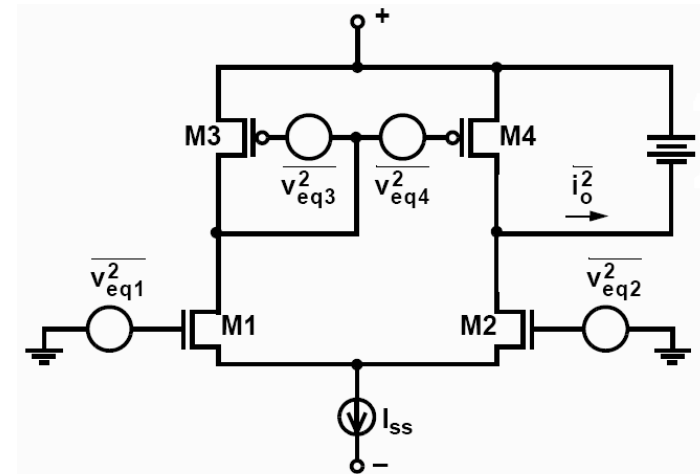




# Noise in CMOS Opamps



The gain of the input stage in a MOS op amp is usually large enough so that the input-referred noise of the overall amplifier is dominated by the noise contributions from the input-stage transistors.

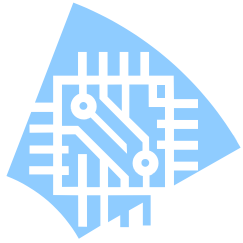


$$\overline{i_o^2} = g_{m1-2}^2 (\overline{v_{eq1}^2} + \overline{v_{eq2}^2}) + g_{m3-4}^2 (\overline{v_{eq3}^2} + \overline{v_{eq4}^2})$$

$$\overline{i_o^2} = g_{m1-2}^2 v_{IT}^2$$

$$\overline{v_{eqT}^2} = \overline{v_{eq1}^2} + \overline{v_{eq2}^2} + \left(\frac{g_{m3}}{g_{m1}}\right)^2 (\overline{v_{eq3}^2} + \overline{v_{eq4}^2})$$





# Noise in CMOS Op Amps (cont'd)

## 1/f NOISE

For an MOS transistor the input-referred 1/f noise can be modeled as:

$$\frac{\overline{v_{1/f}^2}}{\Delta f} = \frac{K_f}{fWLC_{ox}}$$

where  $K_f$  is the FLICKER NOISE COEFFICIENT

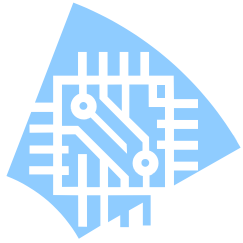
Using this model for each transistor in the input stage, the input-referred 1/f noise for the entire stage is

$$\frac{\overline{v_{1/fT}^2}}{\Delta f} = \frac{2K_{fN}}{fW_1L_1C_{ox}} + \left(\frac{g_{m3}}{g_{m1}}\right)^2 \left(\frac{2K_{fP}}{fW_3L_3C_{ox}}\right)$$

Assuming that  $L_2 = L_1$ ,  $W_2 = W_1$ ,  $L_4 = L_3$  and  $W_4 = W_3$

$$\begin{aligned} \frac{\overline{v_{1/fT}^2}}{\Delta f} &= \frac{2K_{fN}}{fW_1L_1C_{ox}} + \frac{\mu_P(W_3/L_3)}{\mu_N(W_1/L_1)} \left(\frac{2K_{fP}}{fW_3L_3C_{ox}}\right) \\ &= \frac{2K_{fN}}{fW_1L_1C_{ox}} \left[ 1 + \frac{K_{fP}\mu_P L_1^2}{K_{fN}\mu_N L_3^2} \right] \end{aligned}$$





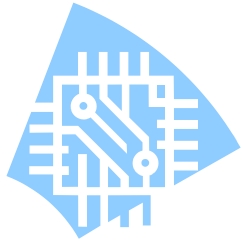
# Noise in CMOS Op Amps (cont'd)

## Thermal NOISE

The input-referred thermal noise for an NMOS transistor is:

$$\begin{aligned}\overline{v_{eq}^2} &= 4kT \left( \frac{2}{3g_m} \right) \\ \overline{v_{eqT}^2} &= 4kT \left( \frac{4}{3g_{m1}} \right) + \left( \frac{g_{m3}}{g_{m1}} \right)^2 \left[ 4kT \left( \frac{4}{3g_{m3}} \right) \right] \\ &= 4kT \left( \frac{4}{3g_{m1}} \right) \left[ 1 + \frac{g_{m3}}{g_{m1}} \right] \\ &= 4kT \left( \frac{4}{3g_{m1}} \right) \left[ 1 + \sqrt{\frac{\mu_P(W_3/L_3)}{\mu_N(W_1/L_1)}} \right] \\ &= 4kT \left( \frac{4}{3\sqrt{2\mu_N C_{ox}(W_1/L_1)I_{d1}}} \right) \left[ 1 + \sqrt{\frac{\mu_P(W_3/L_3)}{\mu_N(W_1/L_1)}} \right]\end{aligned}$$





# Cascode amplifiers

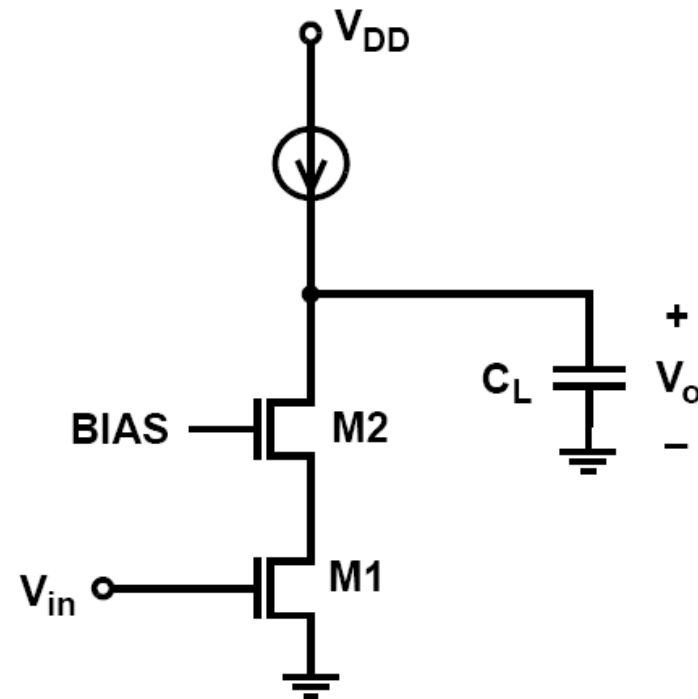
## SIMPLE CASCODE

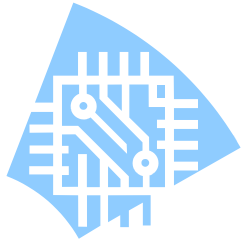
$$A_V(0) = g_{m1} \cdot r_{out}$$

$$r_{out} = (g_{m2}r_{o2} + 1) \cdot r_{o1} + r_{o2}$$

$$\cong g_{m2}r_{o2}r_{o1}$$

$$\therefore A_V(0) \cong g_{m1}g_{m2}r_{o2}r_{o1}$$





# Cascode amplifiers (cont'd)

## Telescopic Opamp

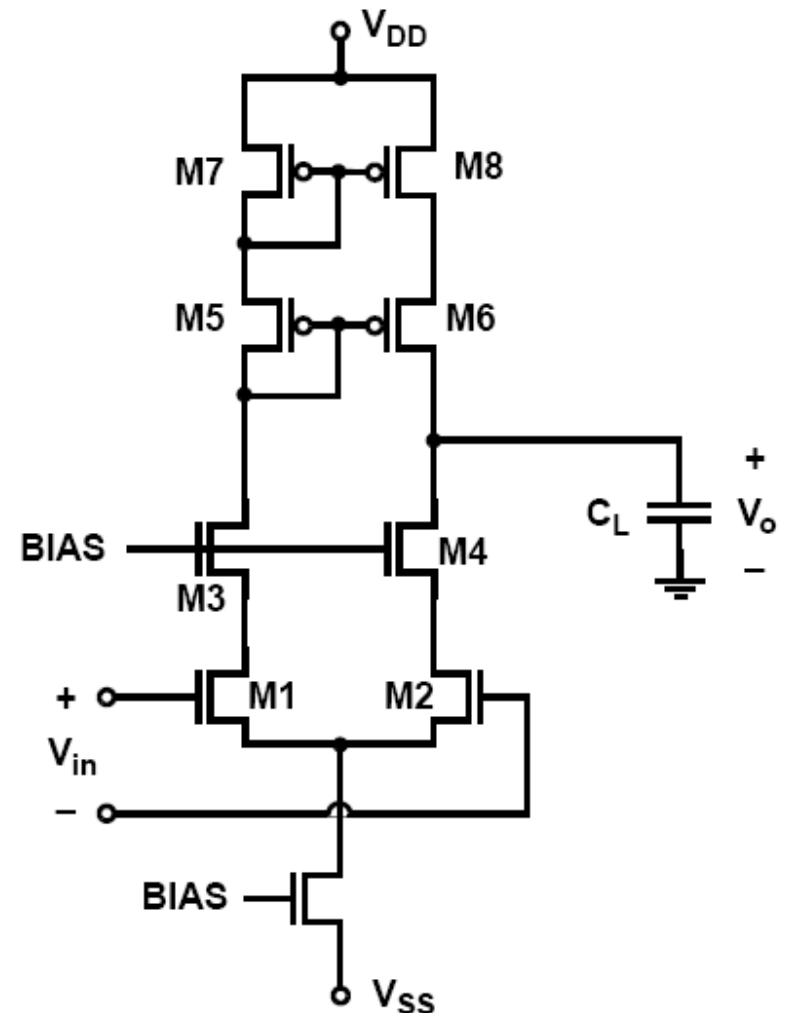
Gain comparable to a 2-stage op amp can also be obtained in a **cascode single stage**

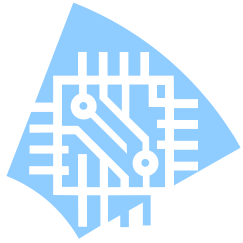
### Advantages

- Single bias current
- High speed

### Disadvantage

- Reduced output swing
- Reduced common-mode input range

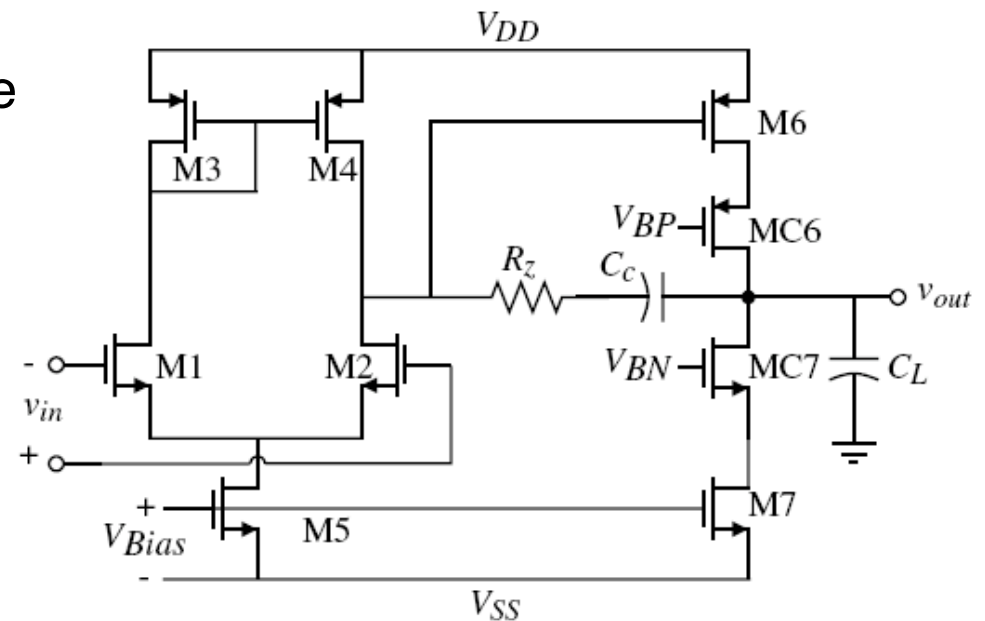




# Cascode amplifiers (cont'd)

## Two-stage opamp with simple cascode

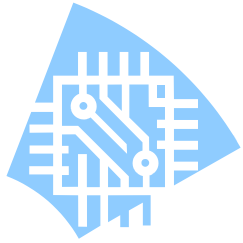
- The second-stage gain has greatly increased improving the Miller compensation
- The overall gain is approximately  $(g_m r_{ds})^3$  or very large
- PSRR+ is improved because  $C_c$  can be smaller.



$$A_v = g_{mI} g_{mII} R_I R_{II} \quad \text{where} \quad g_{mI} = g_{m1} = g_{m2}, \quad g_{mII} = g_{m6},$$

$$R_I = \frac{1}{g_{ds2} + g_{ds4}} = \frac{2}{(\lambda_2 + \lambda_4) I_{D5}} \quad \text{and} \quad R_{II} = (g_{mC6} r_{dsC6} r_{ds6}) \parallel (g_{mC7} r_{dsC7} r_{ds7})$$





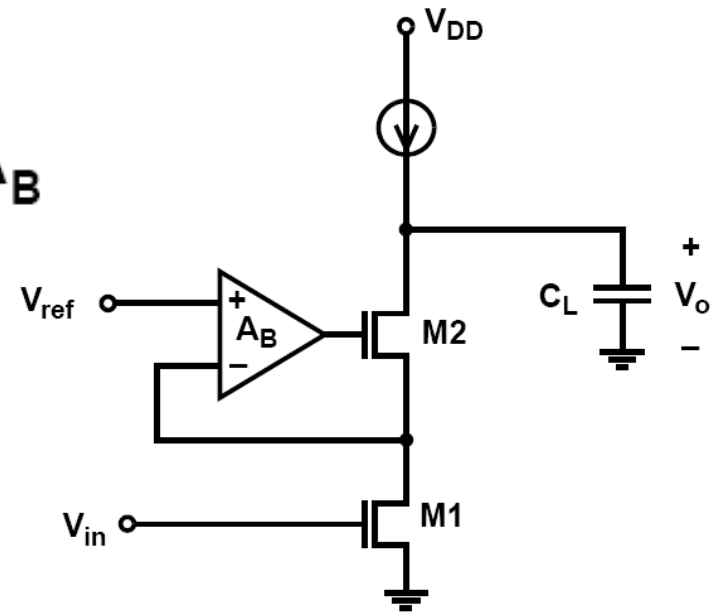
# Gain boosted opamp

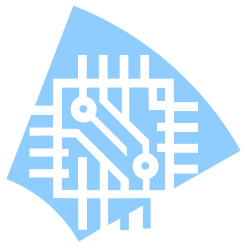
$$r_{out} = [g_{m2}r_{o2}(A_B + 1) + 1] \cdot r_{o1} + r_{o2}$$

$$\cong g_{m2}r_{o2}A_B r_{o1}$$

$$A_V(0) = g_{m1}r_{out} = g_{m1}g_{m2}r_{o1}r_{o2}A_B$$

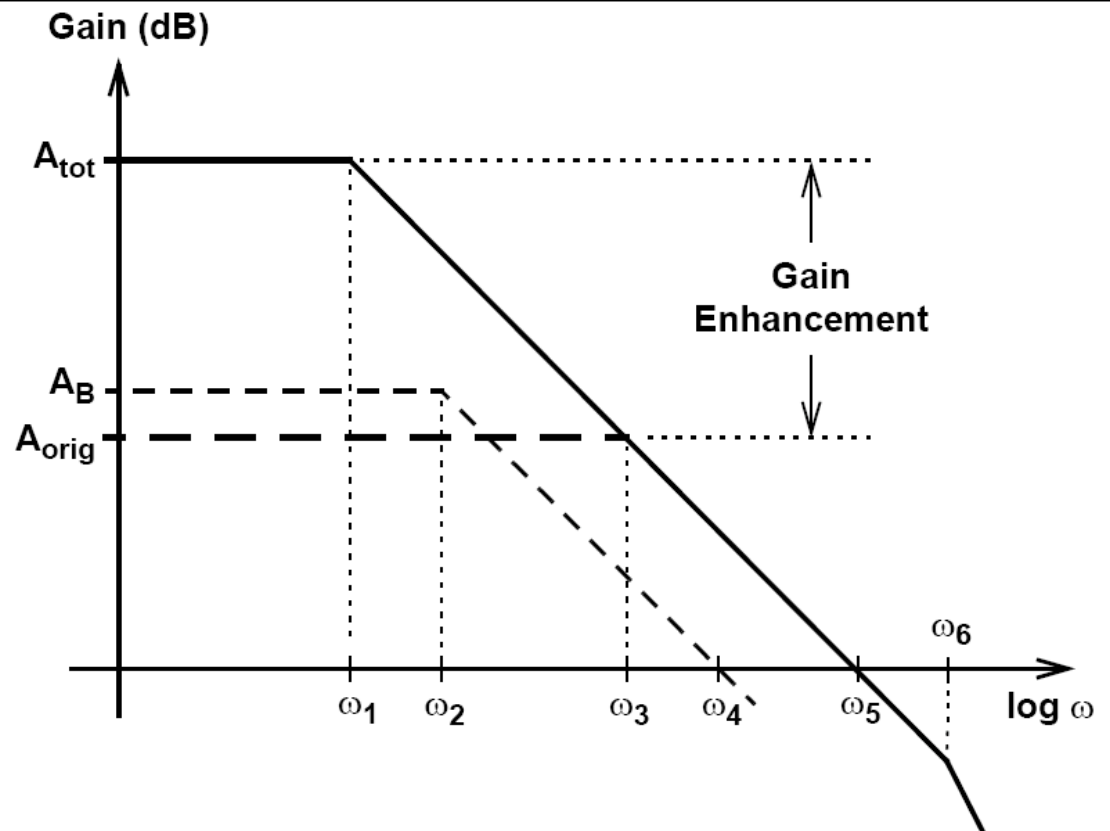
- The “gain-boosted” cascode boosts the output resistance, and thus the low-frequency gain, by  $A_B$ .

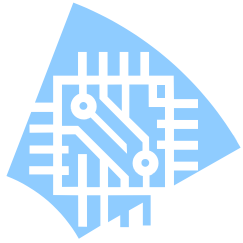




## Gain boosted opamp (cont'd)

- Assume a single-pole response for the gain boosting amplifier with the pole at  $\omega_2$  and a unity gain bandwidth of  $\omega_4$ .
- The unity-gain bandwidth,  $\omega_5$ , of the overall cascode is unchanged and still determined by the load capacitance:  
$$\omega_5 = g_{m1}/C_L$$
- The total gain,  $A_{tot}$ , decreases above  $\omega_1$  due to  $C_L$ .



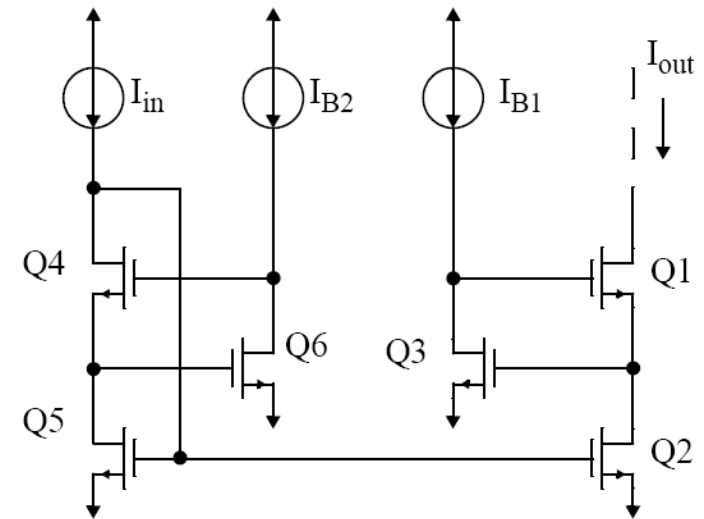


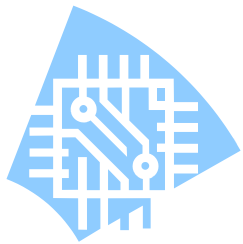
# Gain boosted opamp (cont'd)

- Feedback amplifier realized by common-source amplifier
- Assuming output impedance of  $I_{B1}$  is equal to  $r_{ds3}$ , loop gain will be  $g_{m3}r_{ds3}/2$  resulting in

$$r_{out} \cong \frac{g_{m1} g_{m3} r_{ds1} r_{ds2} r_{ds3}}{2}$$

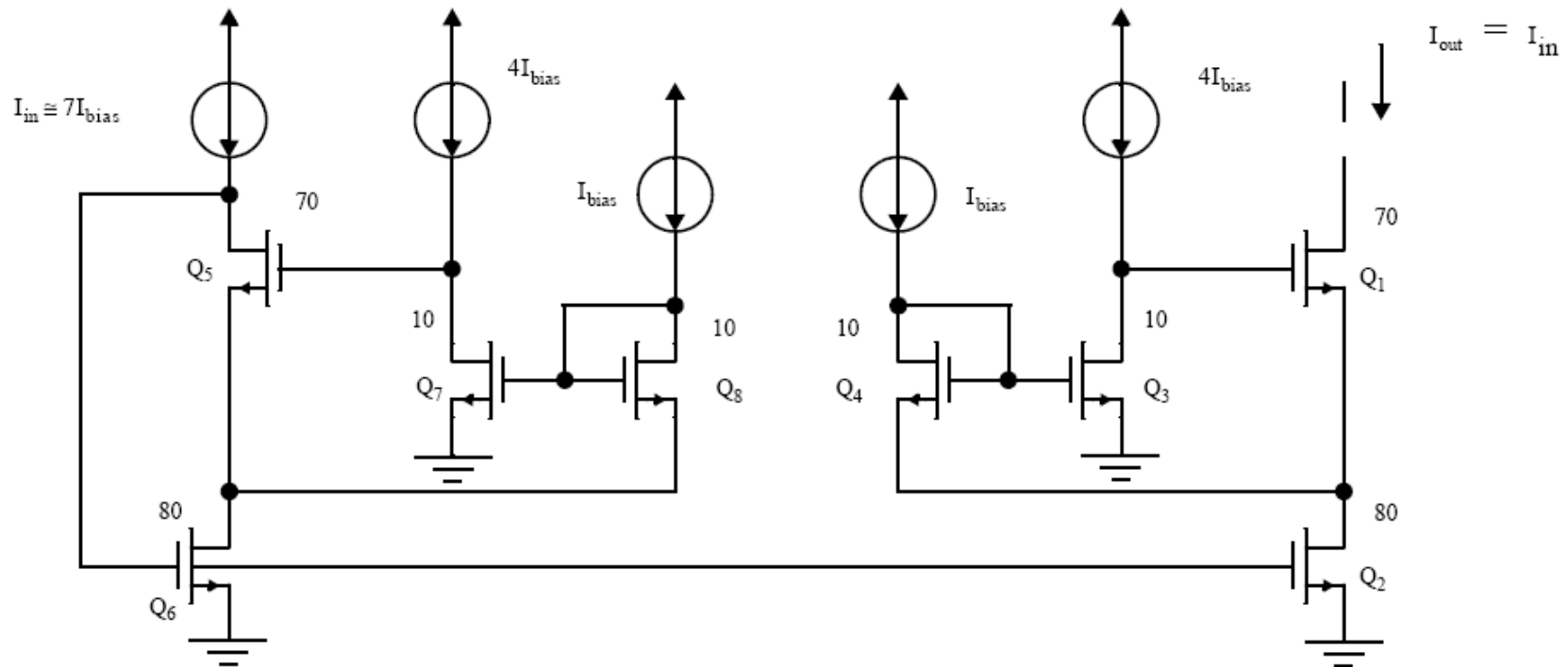
- Circuit consisting of Q4, Q5, Q6. Also  $I_{in}$  and  $I_{B2}$  operate like a diode-connected transistor  $\rightarrow$  results in accurate matching of  $I_{out}$  to  $I_{in}$
- Note that shown amplifier is NOT wide-swing  $\rightarrow$  requires output to be  $2V_{eff} + V_{thn}$  above lower supply.





# Gain boosted opamp (cont'd)

## Improved output voltage swing

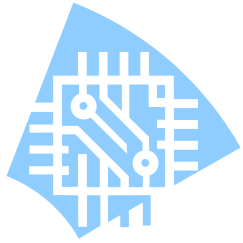


- $Q_3$  and  $Q_7$  are biased at 4 times current density  $\rightarrow 2V_{eff}$
- Requires roughly twice power dissipation.



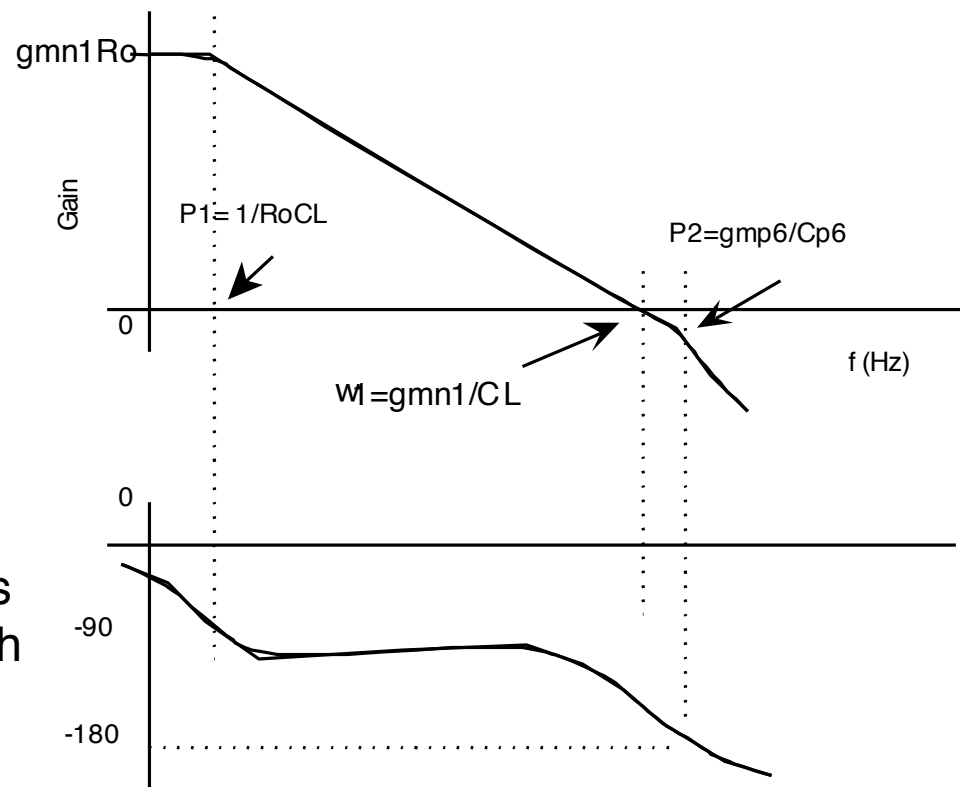




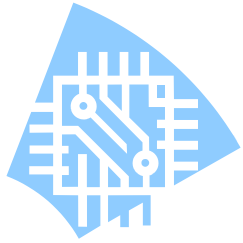


# Folded-Cascode Opamp (cont'd)

- The dominant pole of the folded cascode amplifier is associated with the output node.
- $C_L$  provides the frequency compensation. An increase in  $C_L$  lowers the amplifier's unity-gain bandwidth but does not compromise its phase margin.
- The second nondominant pole in the folded cascode is associated with the cascode devices M5 and M6. This pole is located near the transistor  $\omega_t$  and is much greater in magnitude than the lowest nondominant pole in the 2-stage opamp,  $|p2| = g_{m6}/C_L$ .



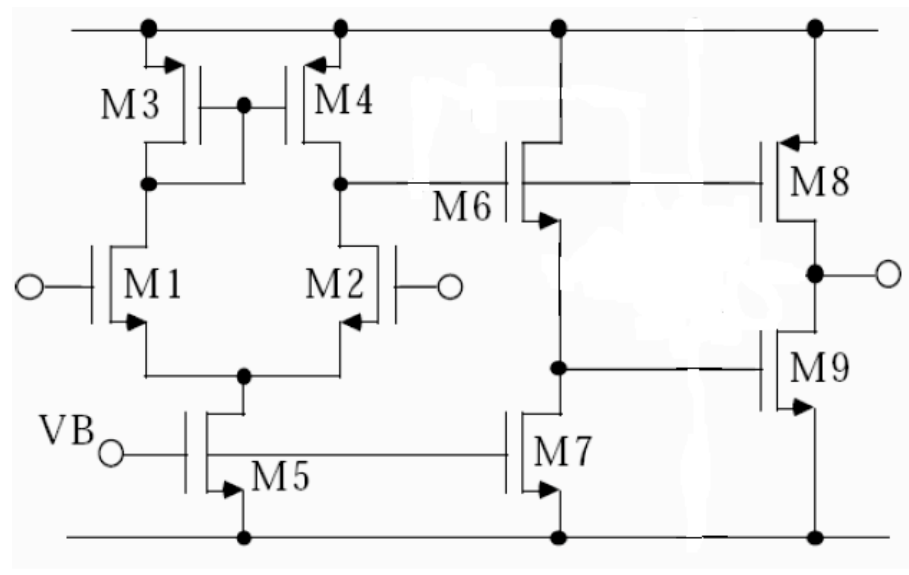
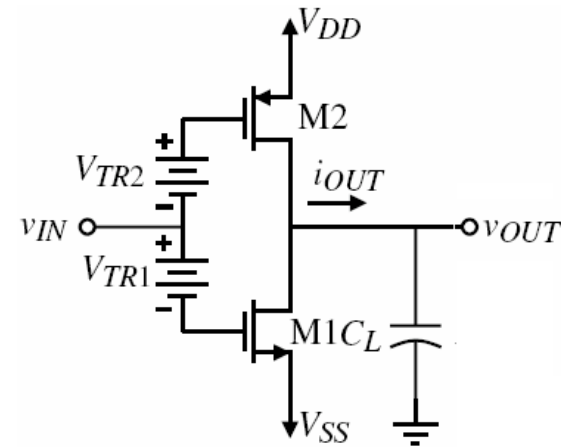


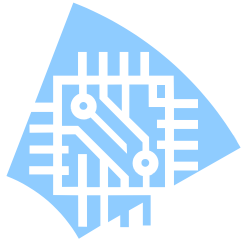


# Class AB amplifier

- “Class AB”: an amplifier that can have an output current which is larger than its DC quiescent current.
- M6 and M7 act as a level shifter, M8 and M9 act as a class AB push-pull amplifier.

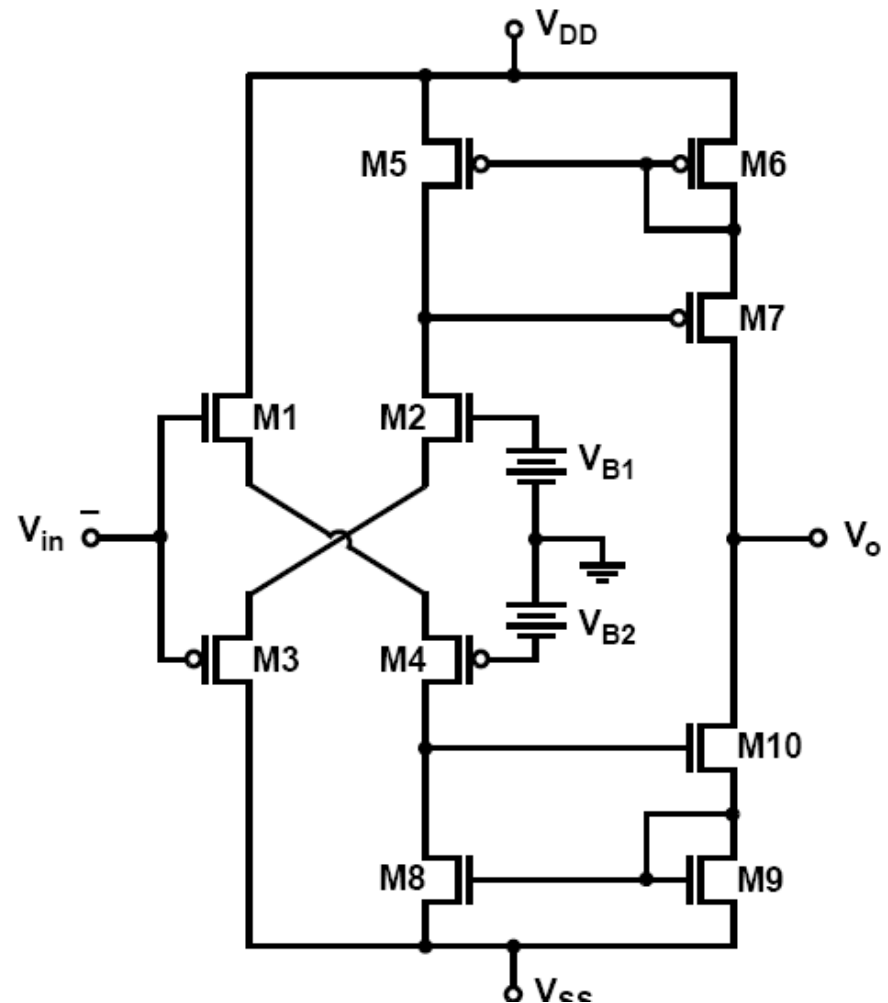
$$A_2 = \frac{g_{m8} + g_{m9}}{g_{ds8} + g_{ds9}}$$

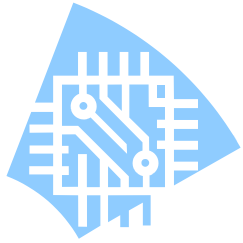




## Class AB amplifier (cont'd)

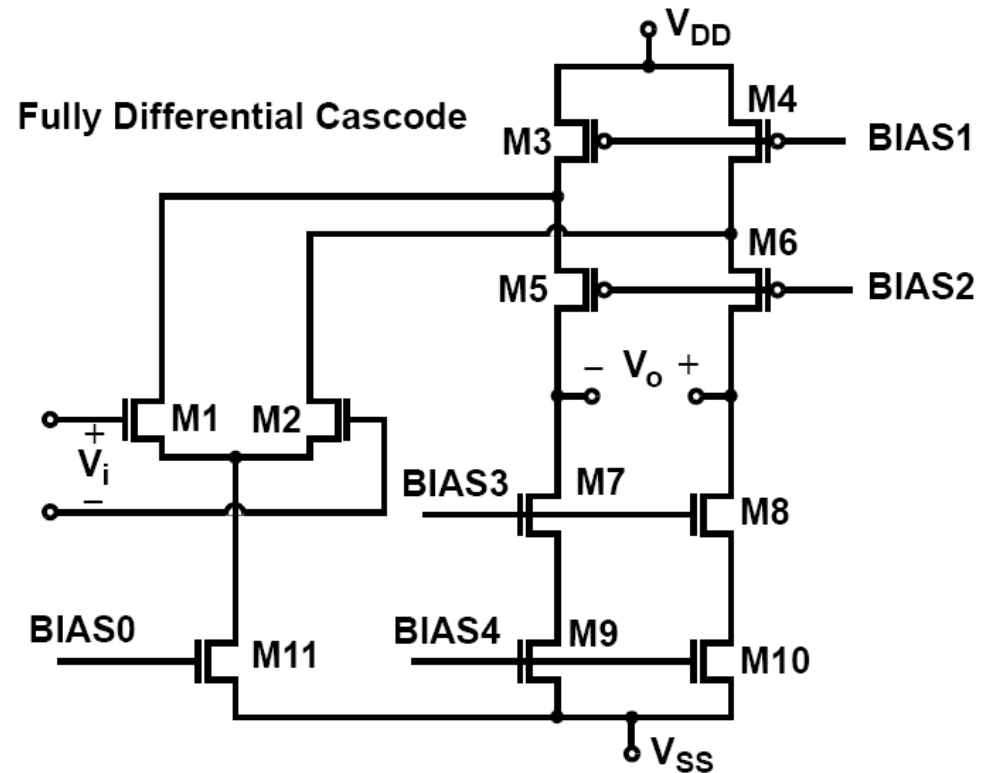
- When  $V_{in} = 0$ , the quiescent currents are set by  $V_{B1}$  &  $V_{B2}$
- As  $V_{in}$  goes positive, the current in M1 & M4 increases until  $V_{in} = V_{DD}$ , while M2 & M3 turn off. Therefore, the mirror circuit M5-M7 turns off, while a very strong drive is supplied to the mirror M8-M10.

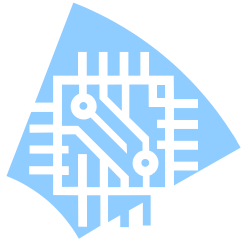




# Fully-differential Opamp

- High PSRR since supply variations appear as common-mode signals
- Effective output swing is doubled
- The input-referred noise is unchanged  $\rightarrow$  6 dB increase in the SNR
- Stable DC bias points at the output of a fully differential amplifier requires common-mode feedback.



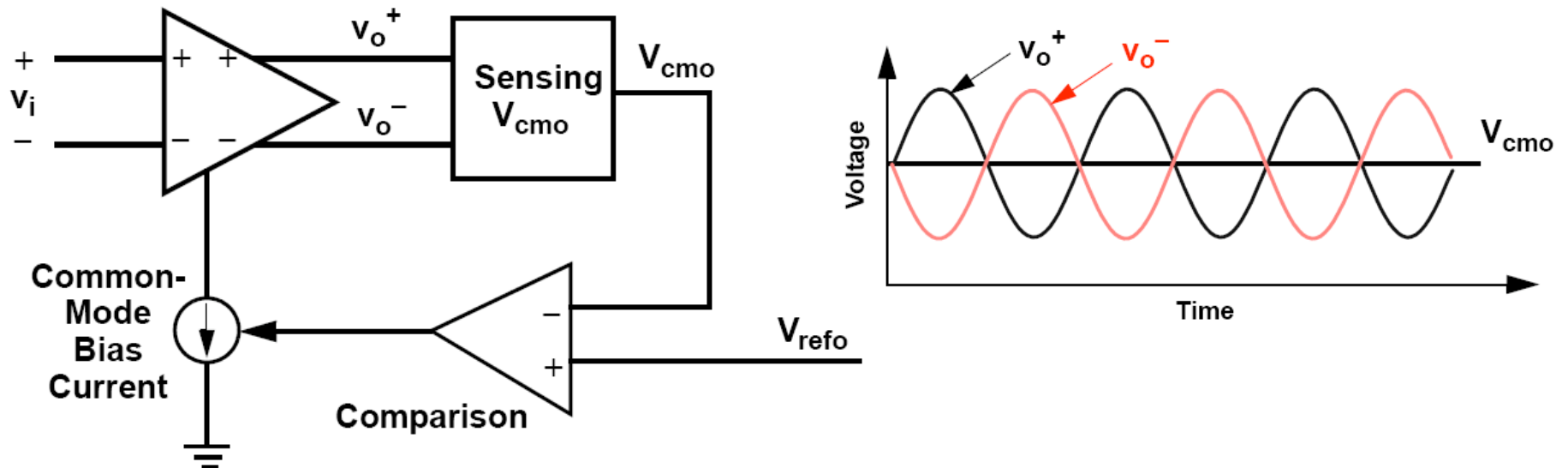


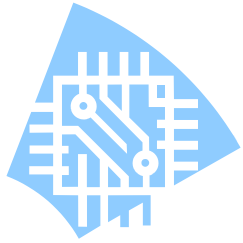
# Fully-differential Opamp (cont'd)

Common-mode feedback has three key components:

- Sampling of the common-mode output voltage:
- Comparison with reference voltage
- Feedback of common-mode error to adjust output common-mode voltage

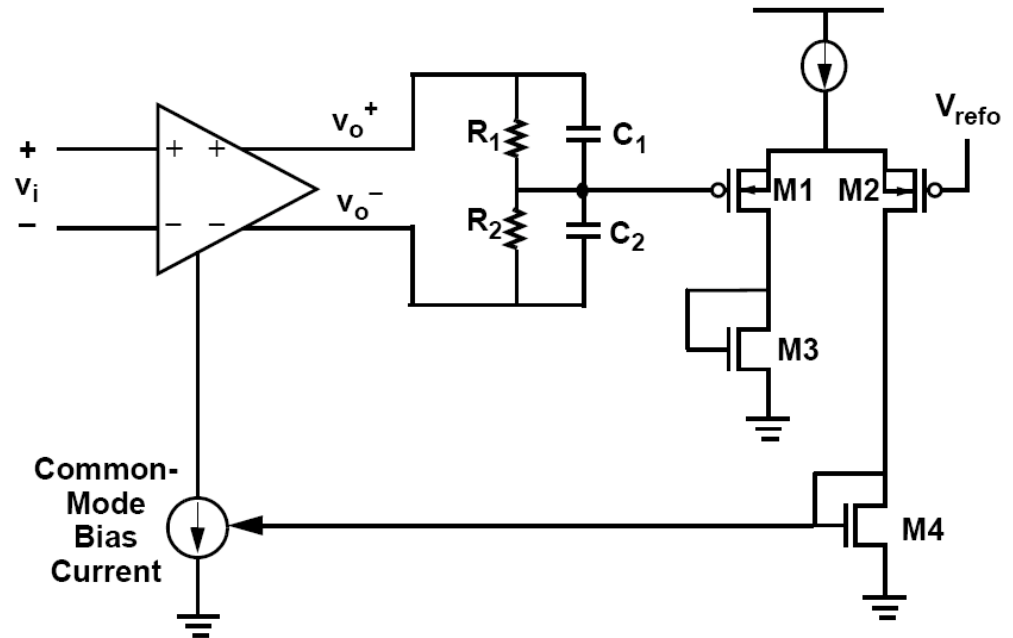
## CONCEPTUAL MODEL





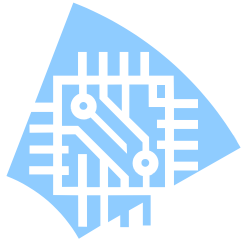
# Fully-differential Opamp (cont'd)

- The common-mode output voltage is sensed using RC filter which takes the average of  $V_{o+}$  and  $V_{o-}$
- The common mode voltage is explicitly compared with a reference voltage  $V_{\text{refo}}$



- The error signal is used to adjust the common-mode bias current via a current mirror (M4).
- The opamp must be able to drive resistive loads. Source followers may be used to buffer the resistive divider if needed.

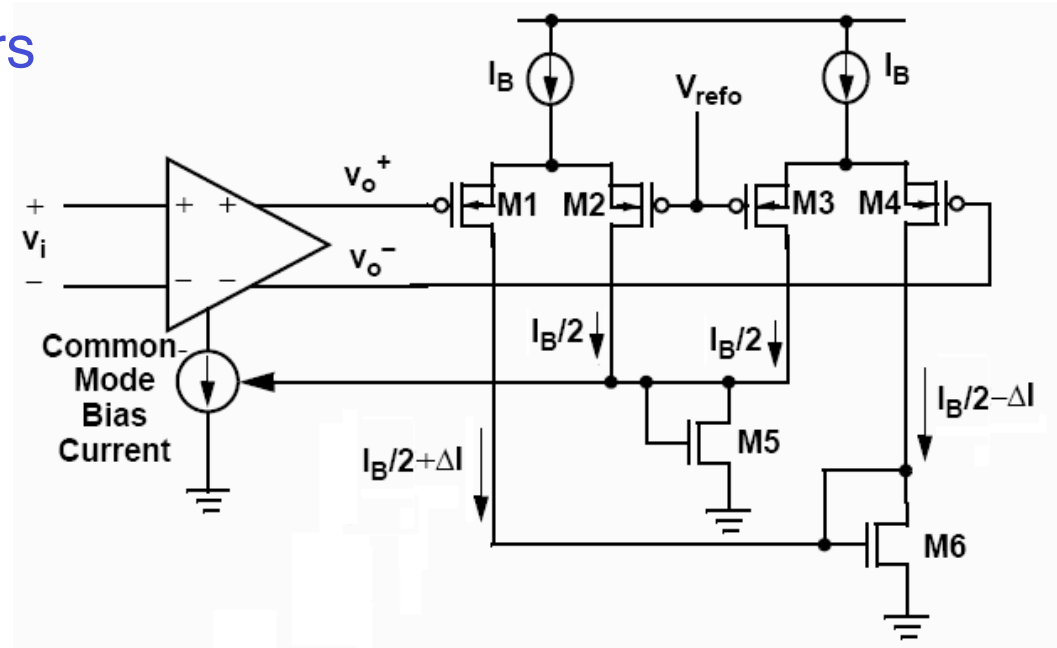




# Fully-differential Opamp (cont'd)

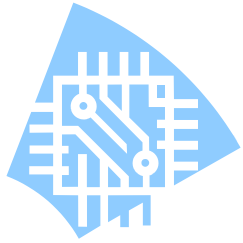
Two PMOS differential pairs used for sensing the common-mode output voltage.

- The common mode voltage is explicitly compared with a reference voltage  $V_{\text{refo}}$ .



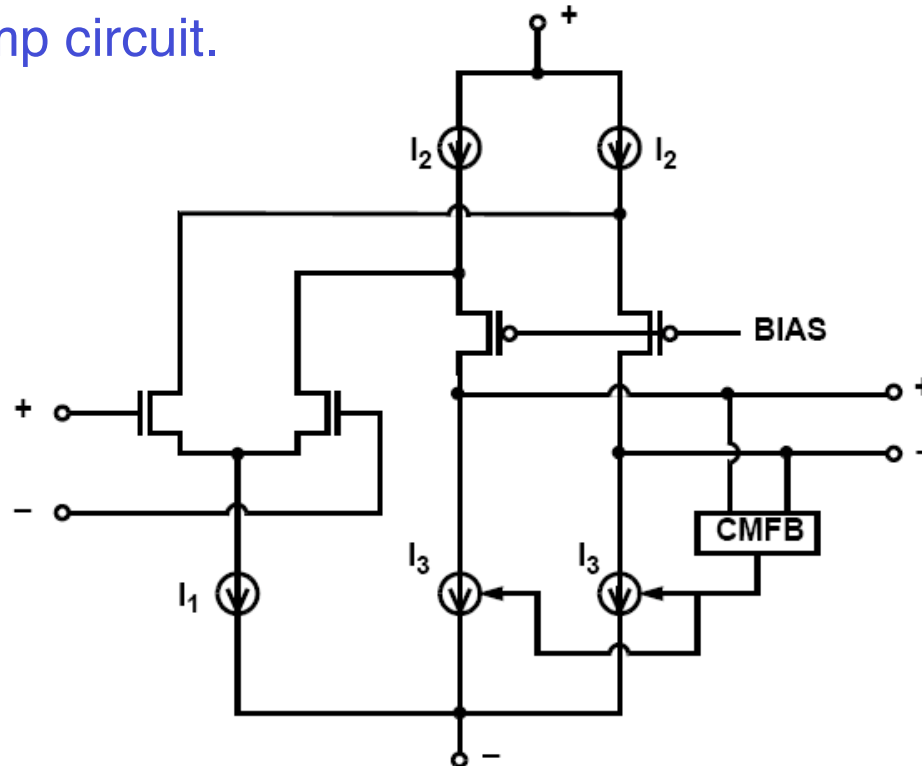
- The error signal is used to adjust the common-mode bias current via a current mirror (M5).
- Maximum output common-mode range is limited by M1- M4.





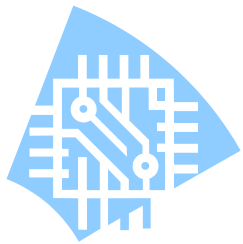
# Fully-differential Opamp (cont'd)

Typical differential opamp circuit.



Common-mode feedback modulates  $I_3$  so as to maintain  $V_{CM}$

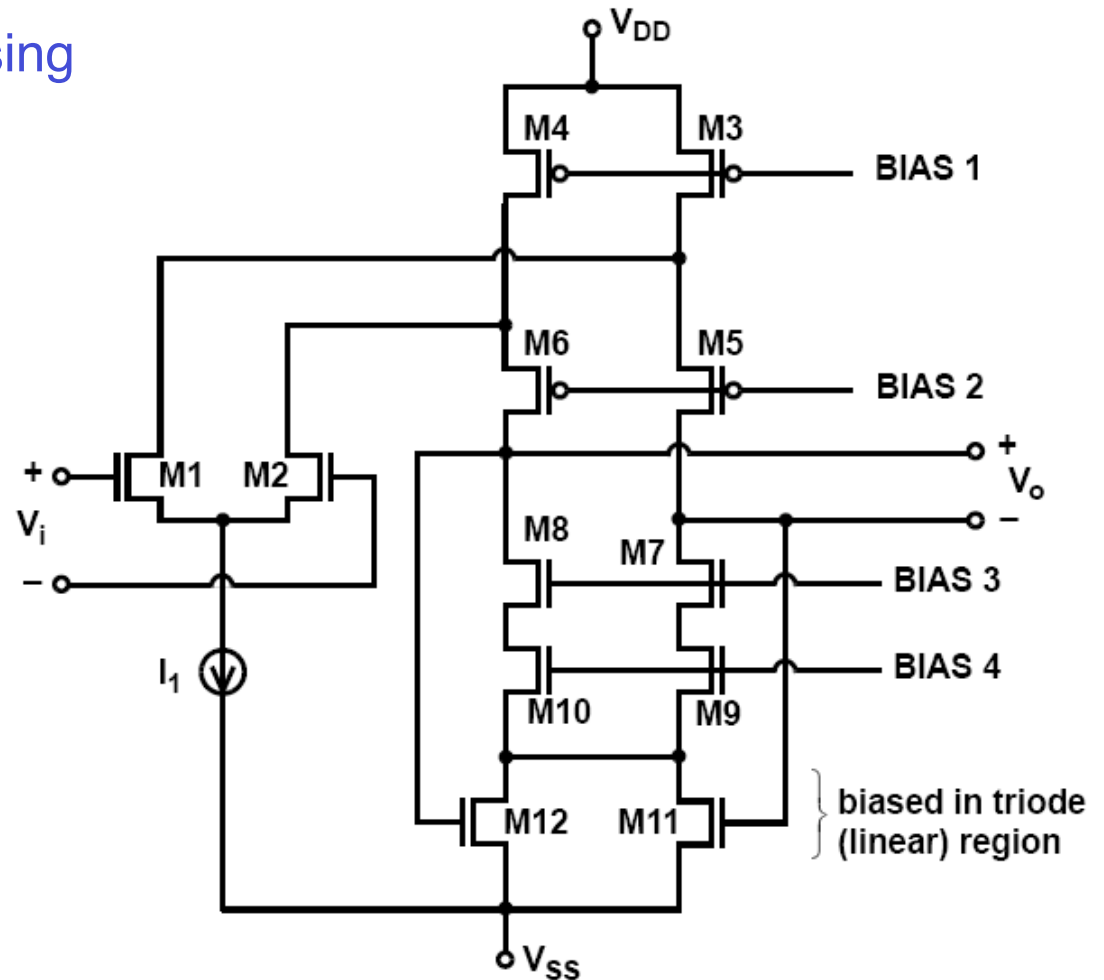


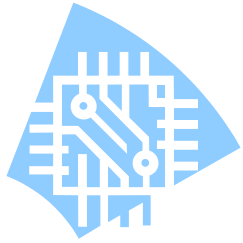


# Fully-differential Opamp (cont'd)

Common-mode voltage sensing using transistors in the linear region.

- M11 and M12, which are biased in the linear region, sense the common-mode output voltage and correspondingly modulate the current in M9 and M10 so as to maintain the desired common-mode output level.

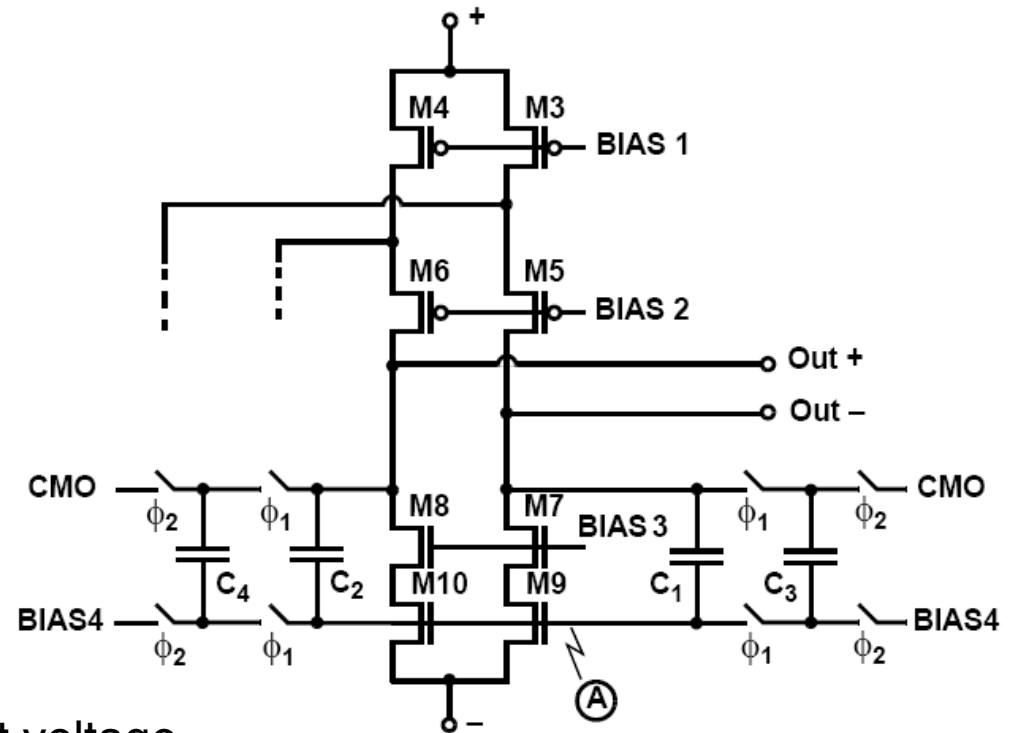


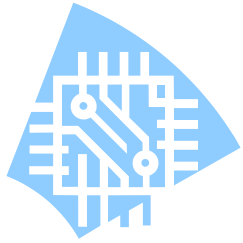


# Fully-differential Opamp (cont'd)

## Dynamic Common-Mode Biasing

- C1 and C2 are nominally equal capacitors that form a voltage divider to sense the common-mode output voltage and level shift that voltage to node A.
- Capacitors C3 and C4, together with the switches controlled by  $\phi_1$  and  $\phi_2$ , are used to establish and maintain the desired DC level shift voltage on C1 and C2.
- CMO = desired common-mode output voltage
- BIAS4 = corresponding bias voltage needed at node A
- This circuit provides a full rail-to-rail common-mode output range and is widely used in switched-capacitor circuits.



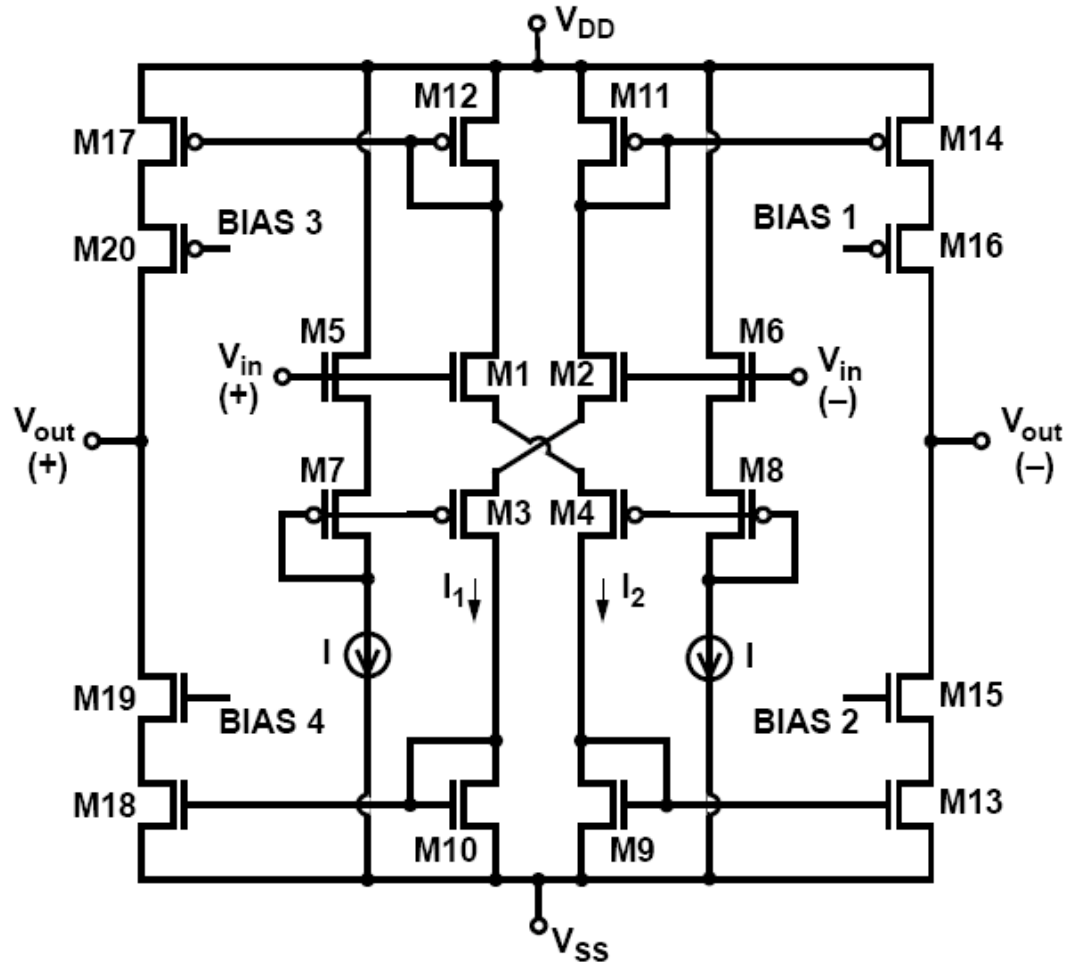


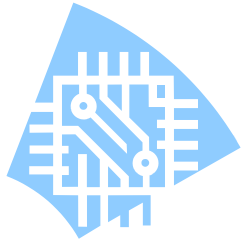
# Fully-differential Opamp (cont'd)

## Fully differential class AB

If M1, M2, M5 and M6 are identical and M3, M4, M7 and M8 are identical, then when  $V_{in}(+) = V_{in}(-) \Rightarrow I_1 = I_2 = I$

- Furthermore, if the current mirrors have a gain of 1, then  $I_{d20} = I_{d16} = I$   
And  $I_{DD} = 6I$ .

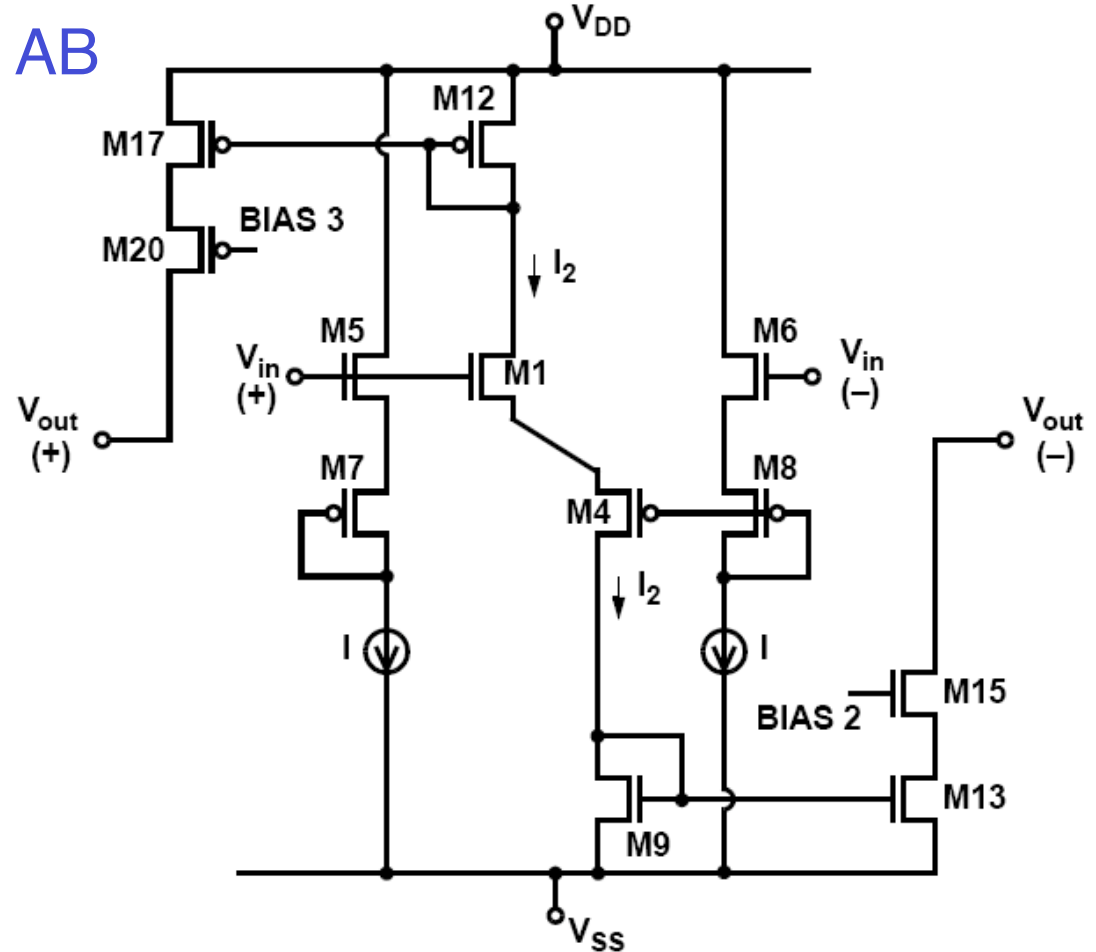


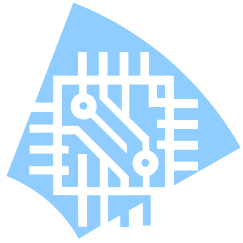


# Fully-differential Opamp (cont'd)

## Fully-differential class AB operation

- For a large positive differential input, half of the circuit is cut off and the active portion of the circuit becomes:





# Fully-differential Opamp (cont'd)

Very high gain  
differential folded  
cascode opamp

