ECE 442
Solid-State Devices & Circuits

18. Advanced Techniques

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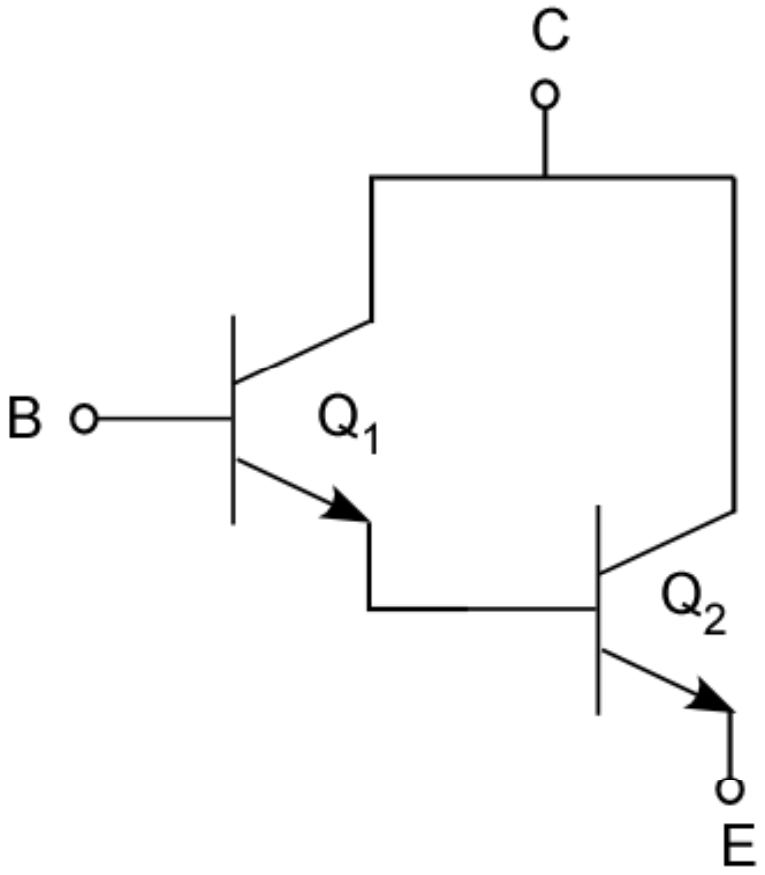
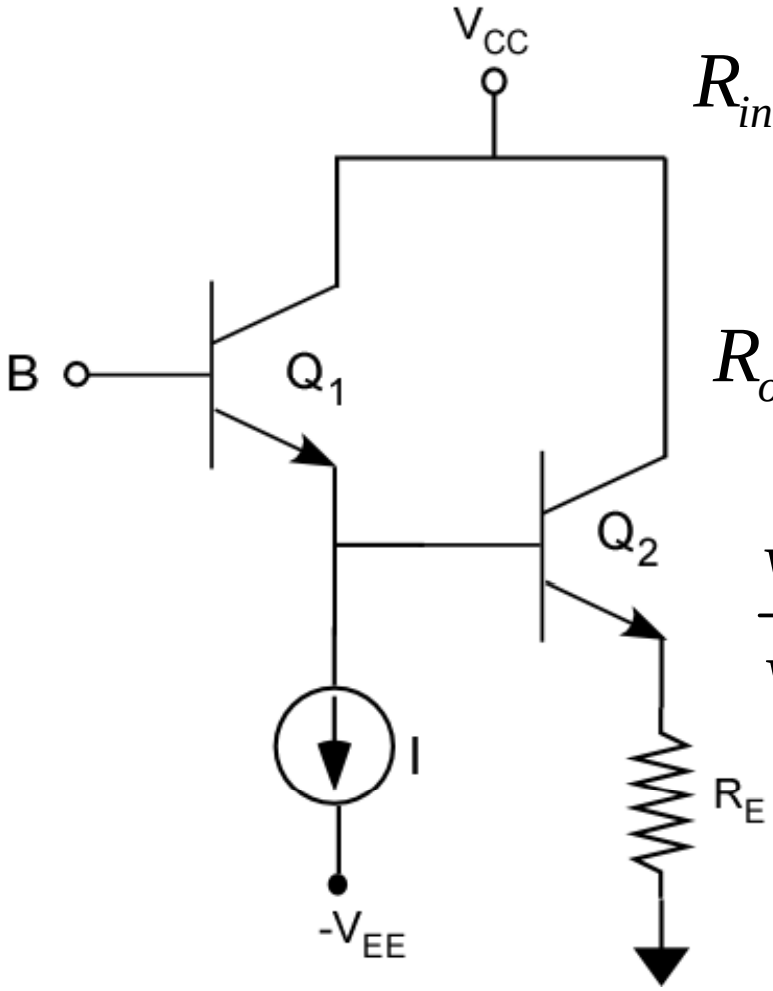
Darlington Configuration



- Popular BJT combination
- Composite transistor with $\beta=\beta_1\beta_2$
- Can be used as the cascade of two CC

Darlington Voltage Follower

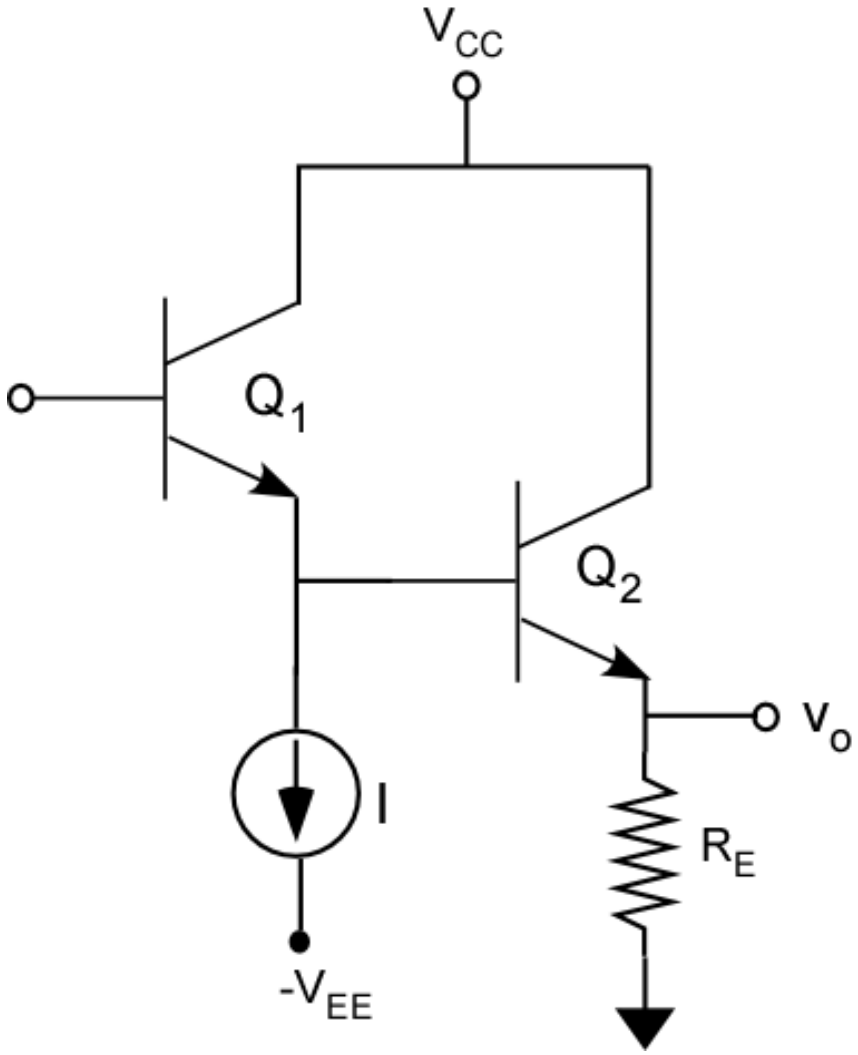


$$R_{in} = (\beta + 1)\left[r_{e1} + (\beta_2 + 1)(r_{e2} + R_E) \right]$$

$$R_{out} = R_E \,//\left[r_{e2} + \frac{r_{e1} + R_{sig}/(\beta_1 + 1)}{\beta_2 + 1} \right]$$

$$\frac{v_{out}}{v_{sig}} = \frac{R_E}{R_E + r_{e2} + \dfrac{r_{e1} + R_{sig}/(\beta_1 + 1)}{\beta_2 + 1}}$$

Darlington Voltage Follower



Darlington follower presents high input impedance

Darlington Voltage Follower

Input impedance

$$R_{in} = (\beta + 1)\left[r_{e1} + (\beta_2 + 1)(r_{e2} + R_E) \right]$$

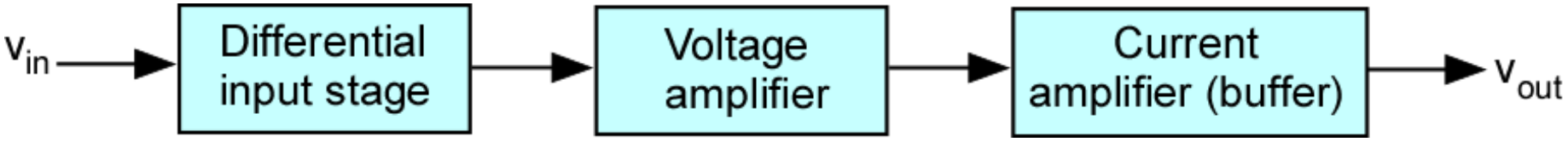
Output impedance

$$R_{out} = R_E \,//\left[r_{e2} + \frac{r_{e1} + \left[R_{sig} /(\beta_1 + 1) \right]}{\beta_2 + 1} \right]$$

Voltage gain:

$$A_{MB} = \frac{R_E}{R_E + r_{e2} + \left[r_{e1} + R_{sig} /(\beta_1 + 1) \right]/(\beta_2 + 1)}$$

Op Amp Architecture



- **Concepts**
  - Many op amps consist of 3 amplifying stages
  - The first stage is always a high-gain differential stage
  - The second stage has moderate value of voltage gain
  - The last stage is often a buffer stage with high current gain and voltage gain near unity
  - The high-frequency poles of each stage introduce phase shift at higher frequencies➔may lead to oscillations

Op Amp Specifications

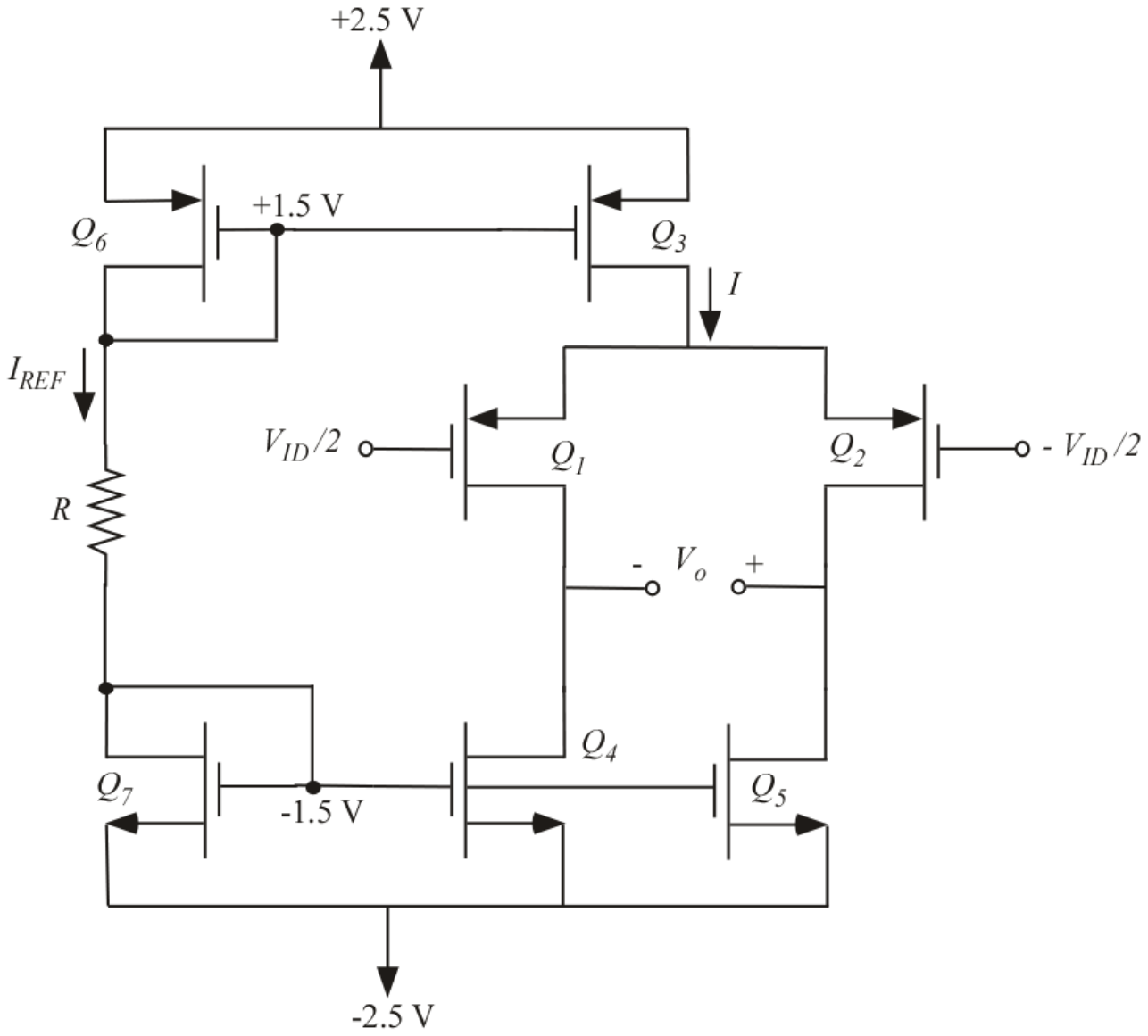
- **Specifications**
  - Input Offset Voltage (V_{os})
  - Input Offset Voltage Drift (TCV_{os})
  - Input Bias Current (I_B)
  - Input Offset Current (I_{os})
  - Common-Mode Input Voltage Range ($CMVR$)
  - Common-Mode Rejection Ratio ($CMRR$)
  - Power Supply Rejection Ratio ($PSRR$)

CMOS OP Amp Example

In the differential amplifier shown, Q_1 and Q_2 form the differential pair while the current source transistors Q_4 and Q_5 form the active loads for Q_1 and Q_2 respectively. The dc bias circuit that establishes an appropriate dc voltage at the drains of Q_1 and Q_2 is not shown. The following specifications are desired: differential gain A_d = 80V/V, I_{REF} = 100 μA, the dc voltage at the gates of Q_6 and Q_3 is +1.5V; the dc voltage at the gates of Q_7, Q_4 and Q_5 is –1.5V.

The technology available is specified as follows: $\mu_n C_{ox} = 3\mu_p C_{ox}$ = 90μA/V^2; $V_{tn} = |V_{tp}| = 0.7$V, $V_{An} = |V_{Ap}|$ = 20V. Specify the required value of R and the W/L ratios for all transistors. Also, specify I_D and V_{GS} at which each transistor is operating. For dc bias calculations, you may neglect channel-length modulation. Fill in the entries in the table provided to show your results.

CMOS OP Amp Example



CMOS OP Amp Example

$$I_{REF} = 100\mu A = \frac{1.5-(-1.5)}{R} \Rightarrow R = \frac{3V}{0.1mA} = 30k\Omega$$

Drain currents are determined by symmetry and inspection V_{GS} values are also determined by inspection for all transistors except Q_1 and Q_2. To determine V_{GS} for Q_1 and Q_2, we do the following: the equivalent load resistance will consist of r_{o1} in parallel with r_{o4} for Q_1 and r_{o2} in parallel with r_{o5} for Q_5. Since the r_o's are equal, this corresponds to $r_o/2$.

We have:

$$g_m \frac{r_o}{2} = A_d \Rightarrow g_m = \frac{2A_d}{r_o} = \frac{2\times 80}{400k\Omega} = 0.4mA/V$$

CMOS OP Amp Example

$$g_m = \frac{2I_D}{V_{ov}} \Rightarrow V_{ov} = \frac{2I_D}{g_m} = \frac{2 \times 0.05}{0.4} = 0.25$$

Take polarity into account for PMOS

$$V_{GS1,2} = -0.25 - V_T = -0.95\,V$$

To find W/L ratios, use

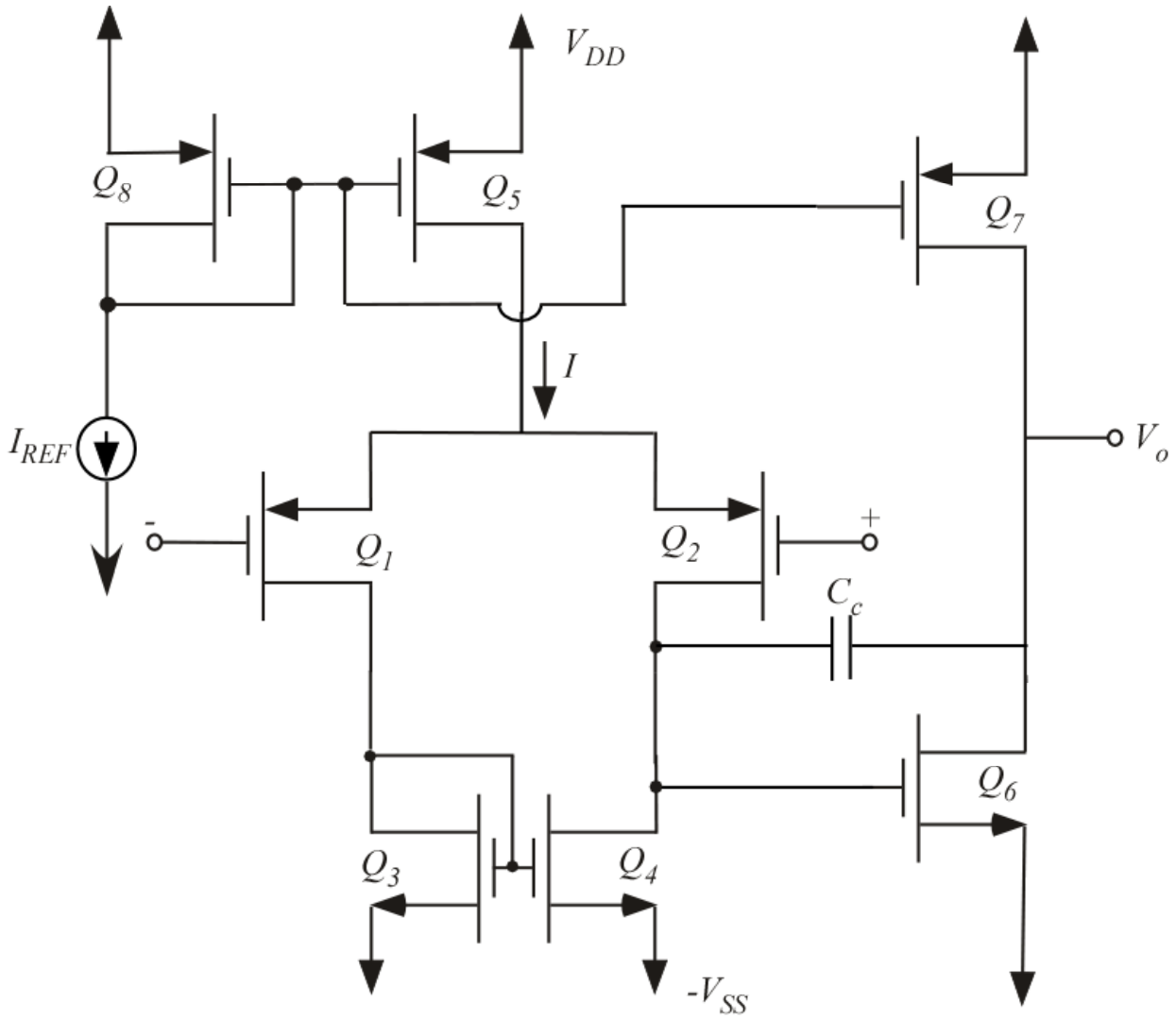
$$I_D = \mu C_{ox} \frac{W}{2L}(V_{GS} - V_T)^2 \Rightarrow \frac{W}{L} = \frac{2I_D}{\mu C_{ox}(V_{GS} - V_T)^2}$$

taking into account PMOS and NMOS devices separately

CMOS OP-AMP DESIGN TABLE

	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Units
μC_{ox}	30	30	30	90	90	30	90	$\mu A/V^2$
I_D	50	50	100	50	50	100	100	μA
V_{GS}	-.95	-.95	-1	+1	+1	-1	+1	V
W/L	57.3	57.3	74 1.	12.3	12.3	73.1	24.7	

2-Stage CMOS Op Amp



2-Stage CMOS Op Amp

Two-stage configuration with two power supplies which can range from +/- 2.5 V for 0.5 μm technology to +/- 0.9 V for 0.18 μm technology. I_{REF} is generated either externally or using on-chip CKT.

Current mirror formed by Q_5-Q_8 supplies differential pair Q_1-Q_2 with bias current. The W/L of Q_5 is selected to control I. The diff pair is actively loaded by current mirror Q_3-Q_4

2-Stage CMOS Op Amp

Second stage is Q_6 which is a CS amplifier for which Q_7 is the current source. A capacitor C_C is included for negative feedback to enhance the Miller effect through Q_6 ➔ compensation

This op amp does not have a low output impedance and is thus not suited for driving a low-impedance load

$$Let\ I_{REF} = 90\ \mu A,\quad V_{tn} = 0.7\,V,\ V_{tp} = -0.8\,V$$

$$\mu_n C_{ox} = 160\ \mu A/V^2,\ \ \mu_p C_{ox} = 40\ \mu A/V^2$$

2-Stage CMOS Op Amp

$$|V_A| \; for \; all \; devices = 10\,V, \quad V_{DD} = V_{SS} = 2.5\,V$$

Voltage Gain

First stage: $A_1 = -g_{m1}\left(r_{o2} \,//\, r_{o4}\right)$

Since Q_8 and Q_5 are matched, $I = I_{REF}$, Q_1, Q_2, Q_3 and Q_4 will have $I/2$ = 45 μA.

I_{Q7}=I_{REF} = 90 μA = I_{Q6}

Let V_{GS}-V_T = V_{ov} (overdrive voltage)

2-Stage CMOS Op Amp

$$From\ I_D = \frac{1}{2}\left(\mu C_{ox}\right)\left(W/L\right)V_{ov}^2$$

We find V_{ov} for each transistor.

Transconductance is: $g_m = \dfrac{2I_D}{|V_{ov}|}$

$$r_o = \frac{|V_A|}{I_D}$$

2-Stage CMOS Op Amp – Voltage Gain

Gain for first stage: $A_1 = -g_{m1}\left(r_{o2} \,//\, r_{o4}\right)$

$$A_1 = -0.3\left(222 \,//\, 222\right) = -33.3\,V/V$$

Gain for second stage: $A_2 = -g_{m6}\left(r_{o6} \,//\, r_{o7}\right)$

$$A_2 = -0.6\left(111 // 111\right) = -33.3\,V/V$$

Overall dc open loop gain is (-33.3)(-33.3) = 1109 V/V

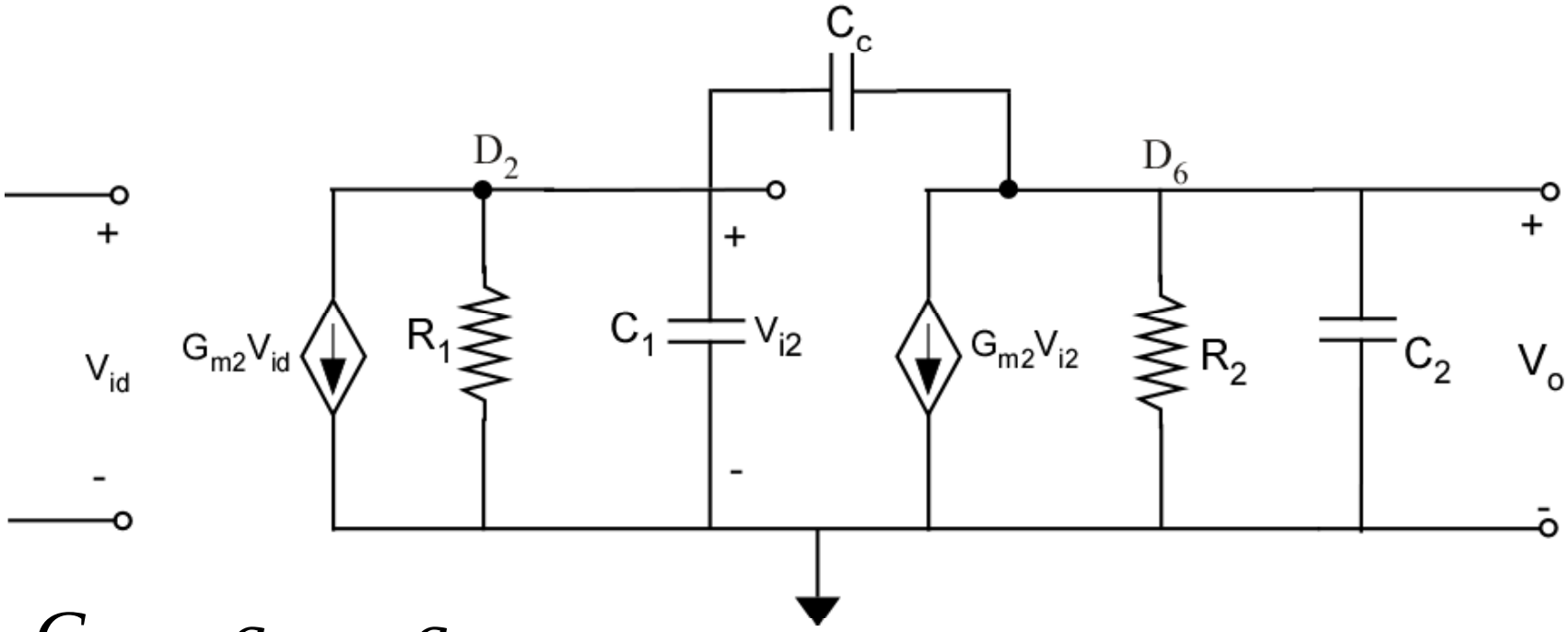
20 log(1109) = 61 dB

2-Stage Op Amp Design Table

	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
W/L	20/0.8	20/0.8	5/0.8	5/0.8	40/0.8	10/0.8	40/0.8	40/0.8
$I_D(\mu A)$	45	45	45	45	90	90	90	90
$\lvert V_{ov}\rvert$ (v)	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3
$\lvert V_{GS}\rvert$ (v)	1.1	1.1	1.0	1.0	1.1	1.0	1.1	1.1
g_m(mA/V)	0.3	0.3	0.3	0.4	0.6	0.6	0.6	0.6
$r_o(k\Omega)$	222	222	222	222	111	111	111	111

2-Stage Op Amp – Frequency Response

Incremental Circuit



$$G_{m1} = g_{m1} = g_{m2}$$

$$R_1 = r_{o2} \,//\, r_{o4}, \quad C_1 = C_{gd4} + C_{db4} + C_{gd2} + C_{db2} + C_{gs6}$$

2-Stage Op Amp – Frequency Response

$$G_{m2} = g_{m6}$$

$$R_2 = r_{o6} // r_{o7}, \; C_2 = C_{db6} + C_{db7} + C_{gd7} + C_L$$

C_L is the load capacitance (usually large) $\Rightarrow C_2 \gg C_1$

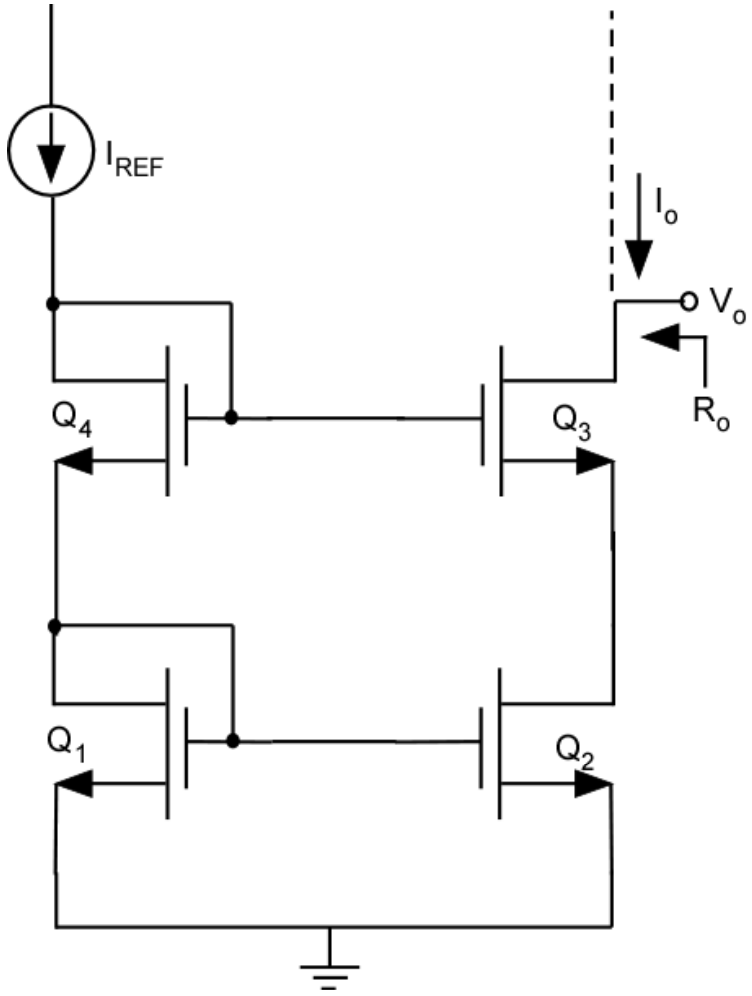
$$\frac{V_o}{V_{id}} = \frac{G_{m1}\left(G_{m2} - sC_C\right)R_1R_2}{1 + sA + s^2B}$$

Cascode Current Mirror

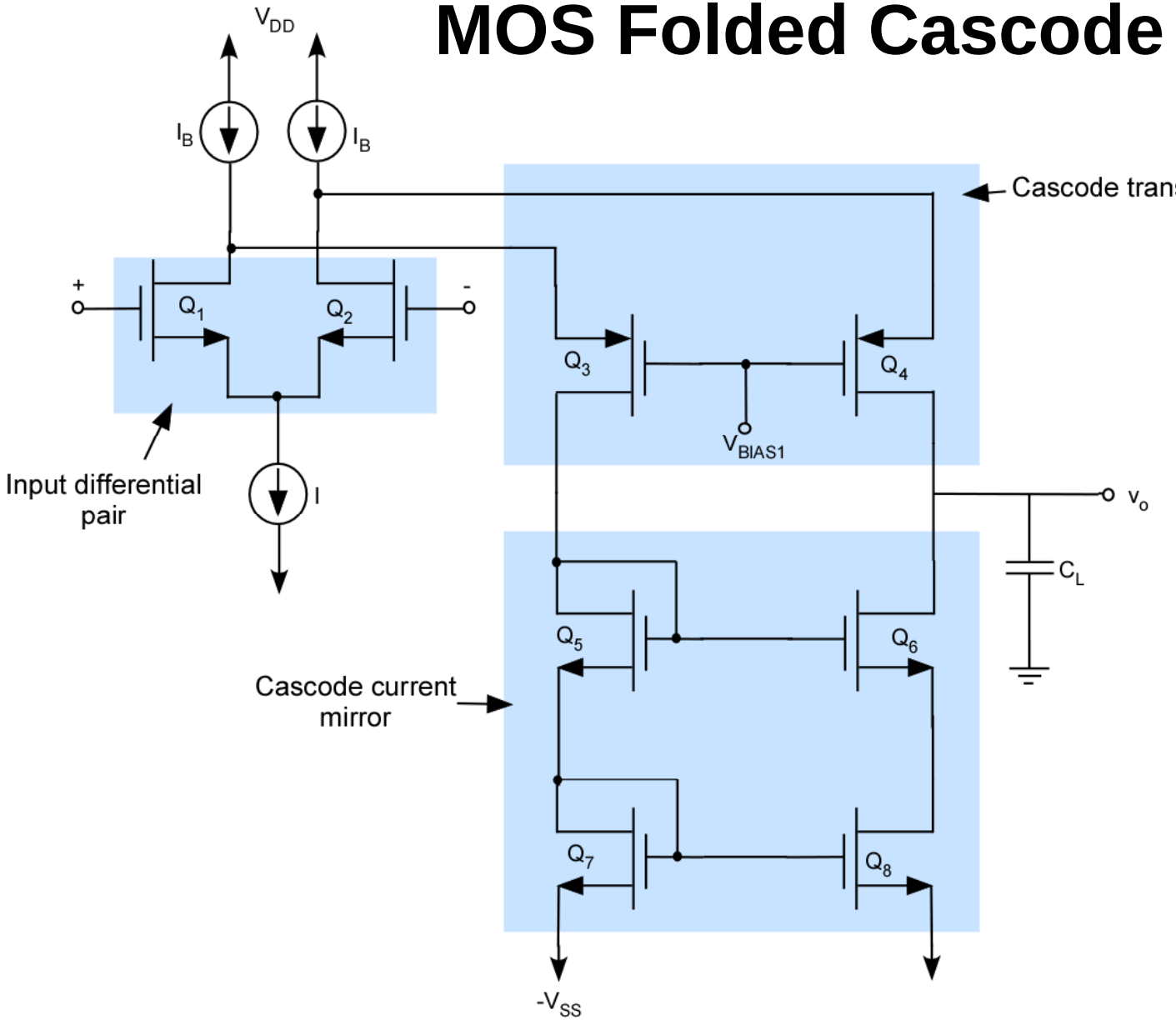
In addition to diode-connected transistor Q_1, Q_4 is used to provide suitable bias gate voltage for Q_3

$$R_o \cong g_{m3} r_{o3} r_{o2}$$

The cascode mirror current has a very high output impedance



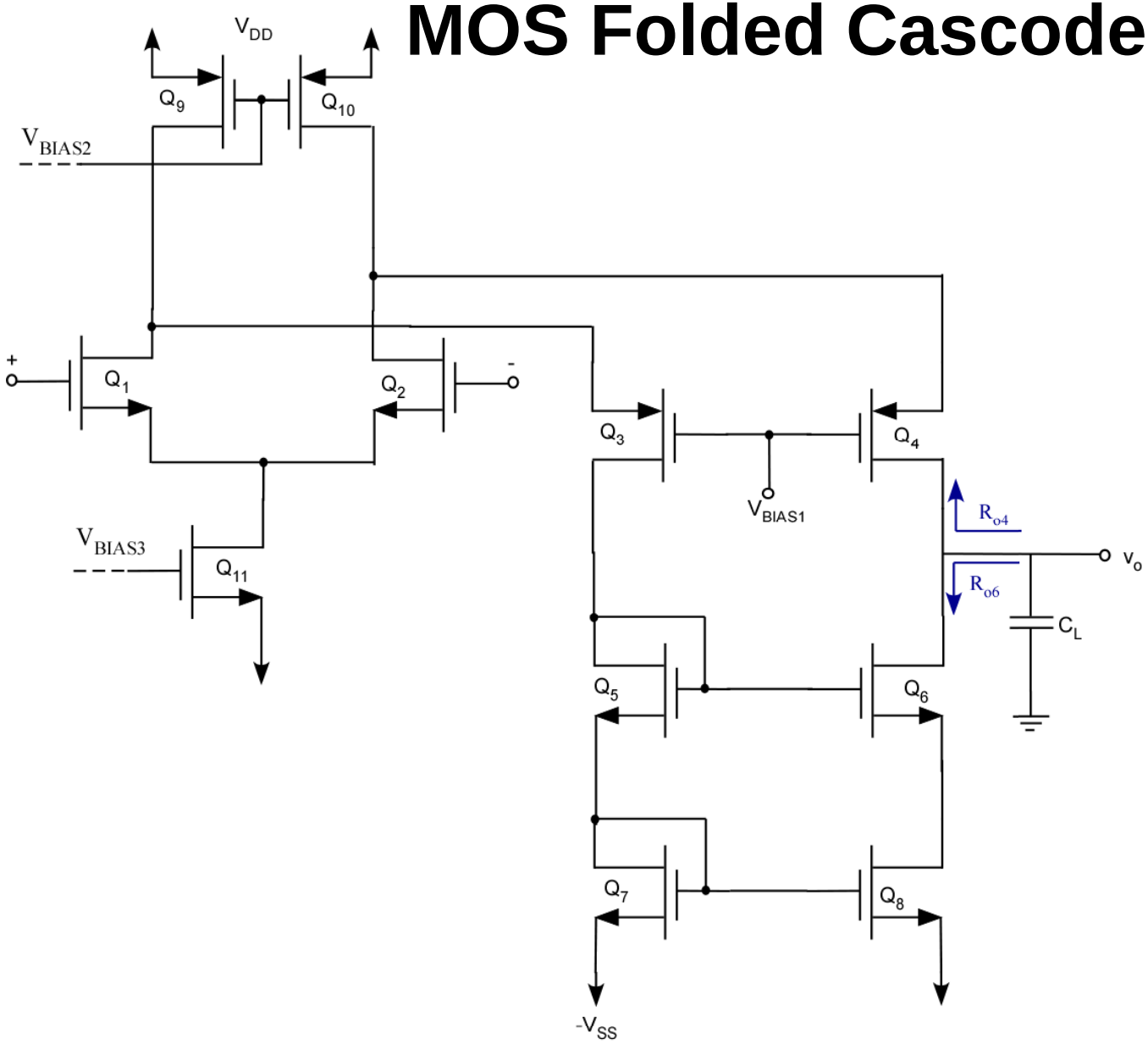
MOS Folded Cascode Amp



MOS Folded Cascode

1. CS transistor with CG transistor of opposite polarity
2. Q_1 and Q_2 for the differential input pair and act as CS amplifiers
3. Q_3 and Q_4 are the cascode transistors with their gates tied to incremental ground
4. Output resistance of current source needed to be high ➔ use cascode current mirror
5. Transistors Q_5-Q_8 make up cascode current mirror
6. Selecting $I_B=I$ forces all transistors to operate at current $I/2$

MOS Folded Cascode Amp



Input Common-Mode Range

Connect both input together to a source V_{ICM}. Q_1 and Q_2 operate in saturation at all times➔V_{ICMmax} should be V_{tn} above voltage at drains of Q_1-Q_2

$$V_{ICM\,\max} = V_{DD} - \left|V_{OV9}\right| + V_{tn}$$

This value can be larger than V_{DD}➔significant improvement over the case of the 2-stage circuit. Minimum value of V_{ICM} is

$$V_{ICM\,\min} = -V_{SS} + V_{OV11} + V_{OV1} + V_{tn}$$

Input Common-Mode Range

Value of V_{ICMmin} is not sufficiently low. V_{BIAS3} should be selected to provide required current I while operating Q_{11} at low overdrive voltage

$$-V_{SS} + V_{OV11} + V_{OV1} + V_{tn} \leq V_{ICM} \leq V_{DD} - \left|V_{OV9}\right| + V_{tn}$$

To maximize the allowable positive swing of v_o (and V_{ICMmax}), select the value of V_{BIAS1} so that Q_{10} operates at the edge of saturation

$$V_{BIAS1} = V_{DD} - \left|V_{0V10}\right| - V_{SG4}$$

Output Voltage Swing

The upper limit of v_o will be

$$v_{o\max} = V_{DD} - |V_{OV10}| - |V_{OV4}|$$

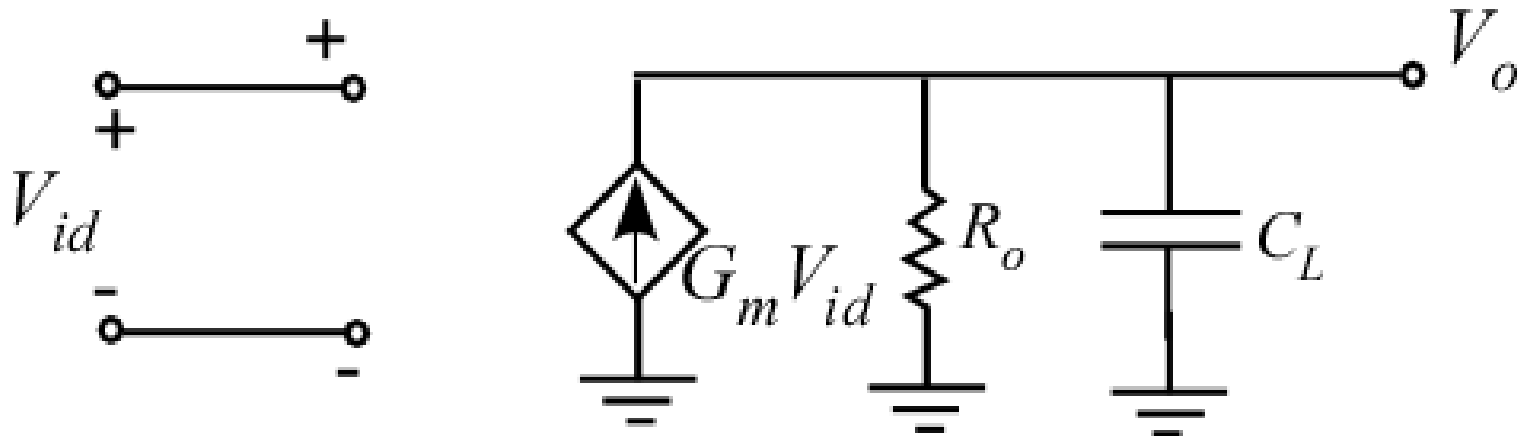
This is two overdrive voltages below V_{DD} ➔ not good. However, lowest possible v_o is when Q_6 reaches the edge of saturation

$$v_{o\min} = -V_{SS} + V_{OV7} + V_{OV5} + V_{tn}$$

This is two overdrive voltages plus a threshold voltage above $-V_{SS}$. Can be alleviated by using modified mirror circuit.

MOS Folded Cascode Amp

Small-Signal Incremental Circuit



Voltage Gain

Amp is a transconductance amplifier with an infinite input resistance a transconductance G_m and an output resistance R_o

$$G_m = g_{m1} = g_{m2} = \frac{2(I/2)}{V_{OV1}} = \frac{I}{V_{OV1}}$$

Output resistance is

$$R_o = R_{o4} \,//\, R_{o6}$$

R_{o4} is the output resistance of the CG transistor Q_4

$$R_{o4} \cong \left(g_{m4} r_{o4}\right)\left(r_{o2} \,//\, r_{o10}\right)$$

Voltage Gain

R_{o6} is given by $R_{o6} \cong g_{m6} r_{o6} r_{o8}$

From which

$$R_o = \left[g_{m4} r_{o4} \left(r_{o2} \,//\, r_{o10} \right) \right] // \left(g_{m6} r_{o6} r_{o8} \right)$$

The DC open-loop gain is $A_v = G_m R_o$

$$A_v = g_{m1} \left\{ \left[g_{m4} r_{o4} \left(r_{o2} \,//\, r_{o10} \right) \right] // \left(g_{m6} r_{o6} r_{o8} \right) \right\}$$

Output Impedance

Output impedance of folded cascode amp is in the order of

$$R_o \propto g_m r_o^2$$

This is high. However, with negative feedback using voltage sampling, it becomes

$$R_{of} = 1/g_{m1}$$

which is much lower

Frequency Dependence

1. Cascode configuration has excellent high-frequency response
2. The first two poles are at very high frequencies
3. Primary purpose of op amp is to feed highly capacitive loads ➔ pole at the output becomes dominant.

$$\frac{V_o}{V_{id}} = \frac{G_m R_o}{1 + sC_L R_o}$$

Frequency Dependence

The dominant pole has a frequency f_P given by

$$f_P = \frac{1}{2\pi C_L R_o}$$

And the unity-gain frequency f_t is given by

$$f_t = G_m R_o f_P = \frac{G_m}{2\pi C_L}$$

Folded Cascode Design

Design a folded with I = 200 μA, I_B= 250 μA, and $|V_{ov}|$ = 0.25 V for all devices. Use k_n'=100 μA/V^2, k_p'=40 μA/V^2, $|V_A'|$ = 20 V/μm, $V_{DD} = V_{SS}$ = 2.5 V, and $|V_t|$=0.75 V. All devices have L=1 μm. use C_L= 5 pF. Find I_D, g_m, r_o and W/L for all transistors

From I and I_B, we can determine I_D for each transistor.The transconductance is given by:

$$g_m = \frac{2I_D}{V_{ov}} = \frac{2I_D}{0.25}$$

Folded-Cascode Amp Design

and the output resistance from

$$r_o = \frac{|V_A|}{I_D} = \frac{20}{I_D}$$

The *W/L* ratio for the devices is given by:

$$\left(\frac{W}{L}\right)_i = \frac{2I_{Di}}{k'V_{ov}^2}$$

Folded-Cascode Amp Design Table

	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_9	Q_{10}	Q_{11}
ID (μA)	100	100	150	150	150	150	150	150	250	250	200
g_m (mA/V)	0.8	0.8	1.2	1.2	1.2	1.2	1.2	1.2	2.0	2.0	1.6
r_o (kΩ)	200	200	133	133	133	133	133	133	80	80	100
W/L	32	32	120	120	48	48	48	48	200	200	64

Folded-Cascode Amp Design

Note that for all transistors,

$$g_m r_o = 160\,V/V$$

$$V_{GS} = 1.0\,V$$

Input common-mode range is

$$-1.25\,V \le V_{ICM} \le 3\,V$$

Output voltage swing is

$$-1.25\,V \le v_o \le 2\,V$$

Folded-Cascode Amp Design

Calculate R_{o4}

$$R_{o4} = 160\left(200 \,//\, 80\right) = 9.14\, M\Omega$$

Calculate R_{o6}

$$R_{o6} \cong g_{m6} r_{o6} r_{o8} = 21.28\, M\Omega$$

The output resistance R_o can then be found as

$$R_o = R_{o4} \,//\, R_{o6} = 6.4\, M\Omega$$

Folded-Cascode Amp Design

Voltage gain is

$$A_v = G_m R_o = 0.8\times10^{-3}\times6.4\times10^{6} = 5120\,V/V$$

Unity gain bandwidth

$$f_t = \frac{G_m}{2\pi C_L} = \frac{0.8\times10^{-3}}{2\pi\times5\times10^{-12}} = 25.5\,MHz$$

Dominant-pole frequency is

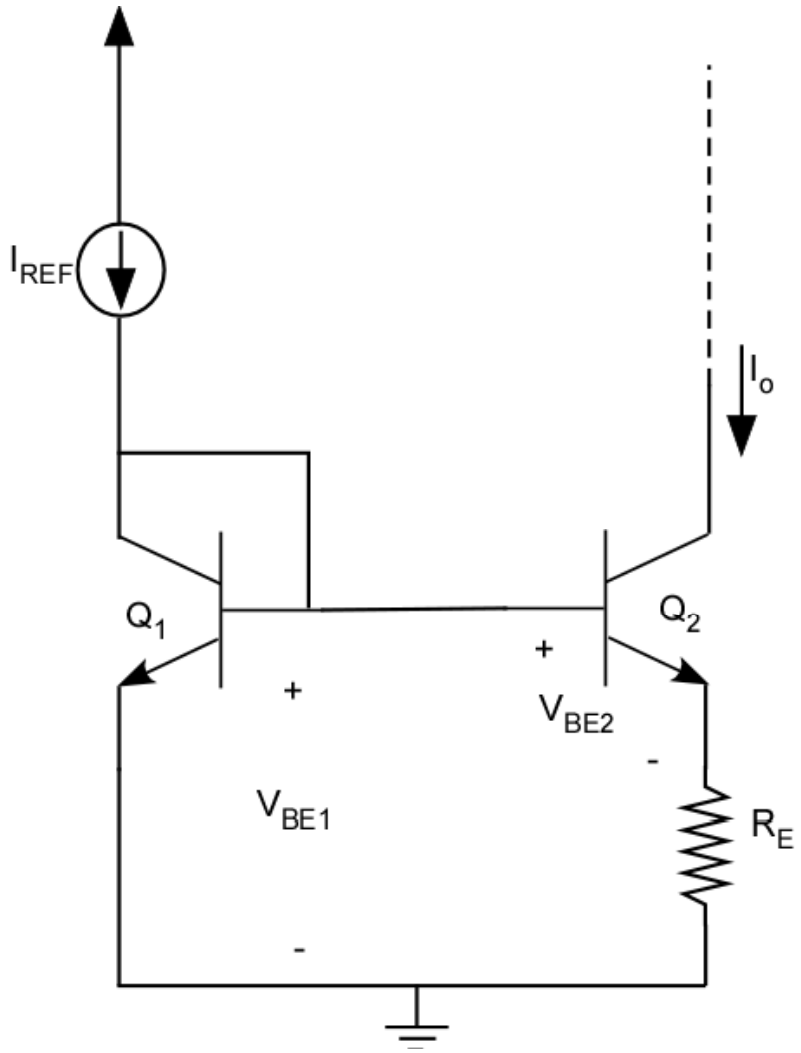
$$f_P = \frac{f_t}{A_v} = \frac{25.5\,MHz}{5120} = 5\,kHz$$

Widlar Current Source

A resistor R_E is included in the emitter lead of Q_2

$$I_O R_E = V_T \ln\left(\frac{I_{REF}}{I_O}\right)$$

The Widlar circuit provides small constant current using relatively small resistors
➔savings in chip area



Design of Op Amps

1. Designer starts with building blocks whose performance can be analyzed to a first order approximation by hand

2. This step provides insight to the designer as the design of the circuit develops

3. At some point designer must turn to computer analysis programs such as SPICE. This will provide speed and accuracy to the design process

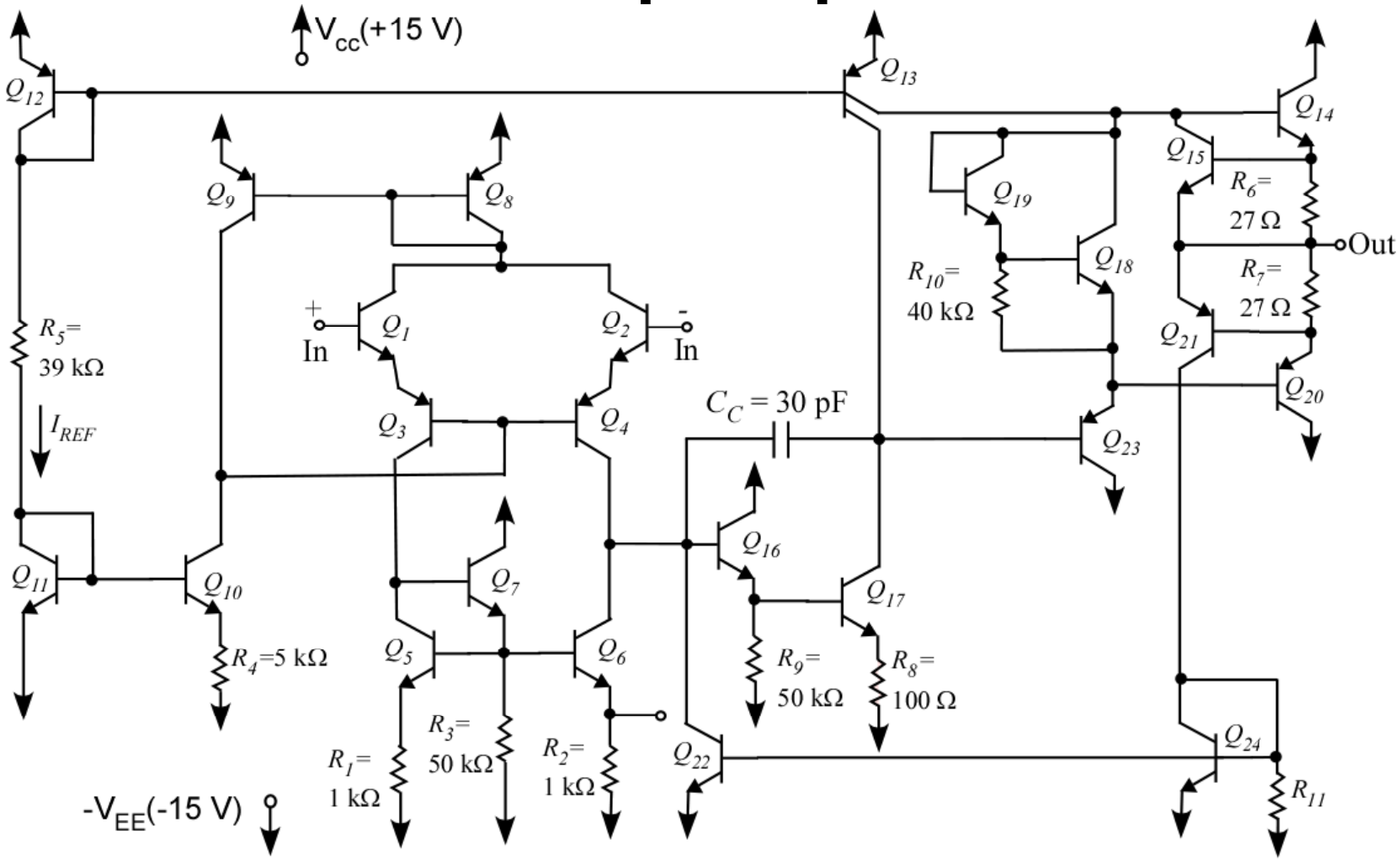
The 741 Op Amp

1. Three-stage amplifier: differential input, single-ended high-gain stage and output buffering stage

2. Several transistors, few resistors and only one capacitor

3. General-purpose op amp that requires two power supplies

741 Op Amp


V_{cc}(+15 V)
Q_{12}
Q_{13}
Q_{14}
Q_{15}
Q_9
Q_8
Q_{19}
R_6= 27 Ω
Out
R_{10}= 40 kΩ
Q_{18}
R_7= 27 Ω
Q_{21}
Q_{20}
R_5= 39 kΩ
Q_1
Q_2
In
In
I_{REF}
Q_3
Q_4
C_C = 30 pF
Q_{23}
Q_{16}
Q_{11}
Q_{10}
Q_7
Q_{17}
R_4=5 kΩ
Q_5
Q_6
R_9= 50 kΩ
R_8= 100 Ω
R_3= 50 kΩ
R_1= 1 kΩ
R_2= 1 kΩ
Q_{22}
Q_{24}
R_{11}
-V_{EE}(-15 V)

General Strategy for Analyzing the 741

1. Identify the individual stages with their respective transistors. For each stage determine the role of the transistors

2. Perform a stage by stage DC analysis of the circuit. Determine the bias points and mode of operation for each transistor.

3. Perform the small-signal analysis of each stage. Develop an incremental model model and find the parameters of the model

General Strategy for Analyzing the 741 (cont')

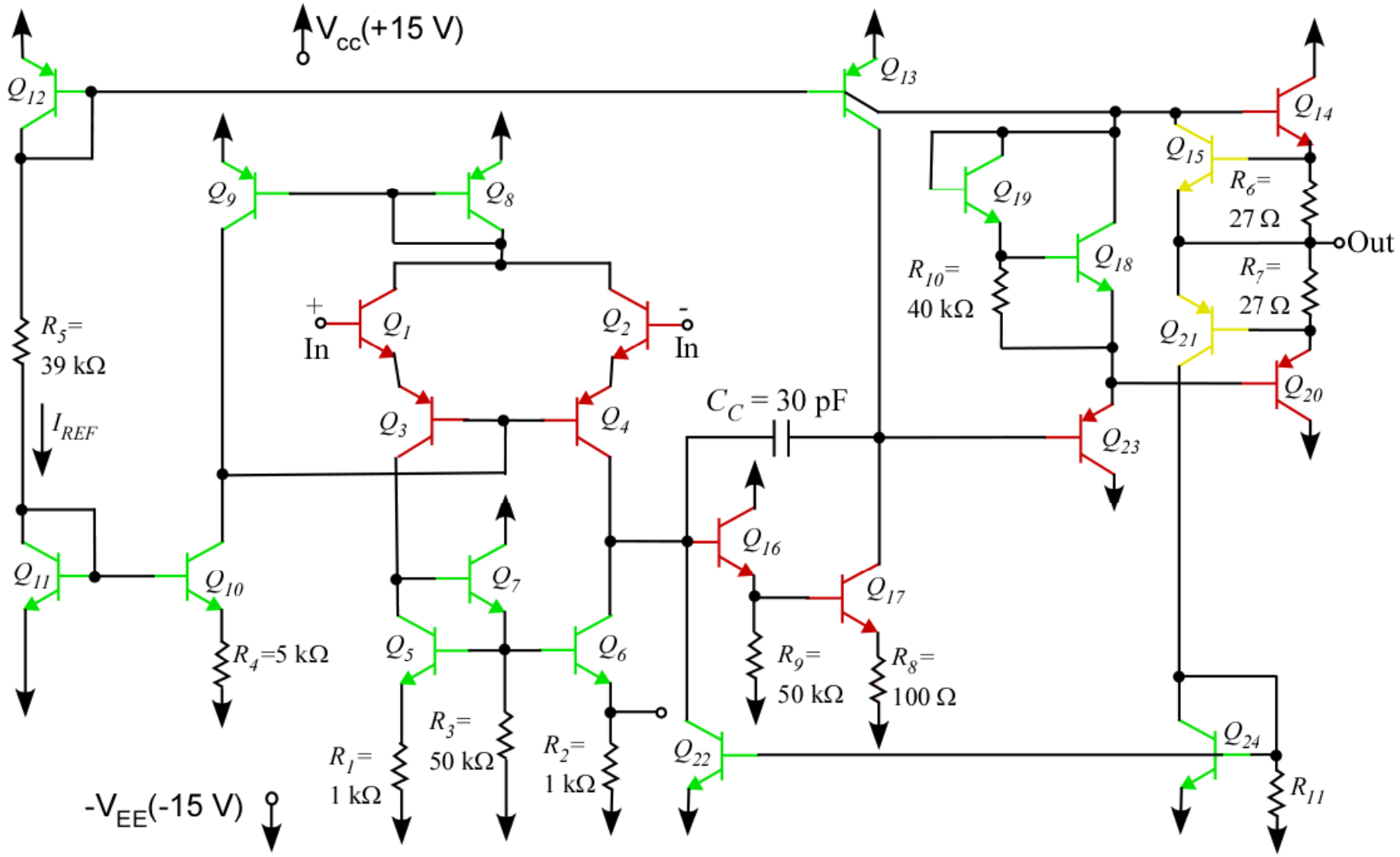
1. For each equivalent circuit, calculate gain, input and output resistances.

2. Determine overall gain of circuit as well as input and output impedance

3. Perform high-frequency analysis of circuit to get an estimate for the poles.

4. Use SPICE to fine tune analysis

741 Op Amp


V_{cc}(+15 V)
Q_{12}
Q_{13}
Q_{14}
Q_9
Q_8
Q_{19}
Q_{15}
R_6= 27 Ω
Out
R_{10}= 40 kΩ
Q_{18}
R_7= 27 Ω
R_5= 39 kΩ
+ In
Q_1
Q_2
- In
Q_{21}
Q_{20}
I_{REF}
Q_3
Q_4
C_C = 30 pF
Q_{23}
Q_{16}
Q_{11}
Q_{10}
Q_7
Q_{17}
R_4=5 kΩ
Q_5
Q_6
R_9= 50 kΩ
R_8= 100 Ω
R_3= 50 kΩ
R_1= 1 kΩ
R_2= 1 kΩ
Q_{22}
Q_{24}
R_{11}
-V_{EE}(-15 V)

741 Op Amp

- **Bias Strategy**
  - I_{REF} is generated by mirror Q_{11}-Q_{12} and R_5
  - Q_8-Q_9 current mirror
  - Q_{13} double-collector lateral *pnp* device; Q_{12} and Q_{13} form a two-output current mirror
  - Q_{13B} provides bias current Q_{17}
  - Q_{13A} provides bias current for the output stage
  - Q_{18} and Q_{19} provide V_{BE} drops to Q_{14} and Q_{20}

741 Op Amp – Input Stage

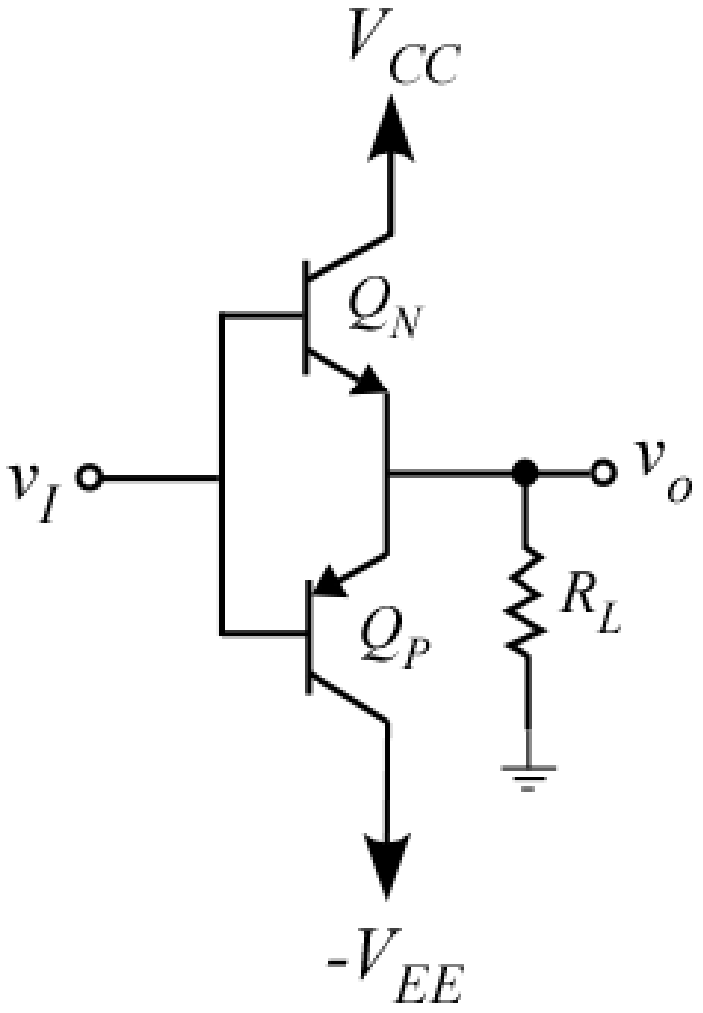
- **Input Stage**
  - Transistors Q_1 through Q_7 make up the input stage
  - Bias is performed by transistors Q_8, Q_9 and Q_{10}
  - Q_1 and Q_2 form a differential emitter-follower pair
  - Q_3 and Q_4 form a differential common-base pair
  - Q_5, Q_6 and Q_7 form the load/current mirror to the input stage
  - Q_3 and Q_4 also perform dc level shifting to allow both positive and negative swings

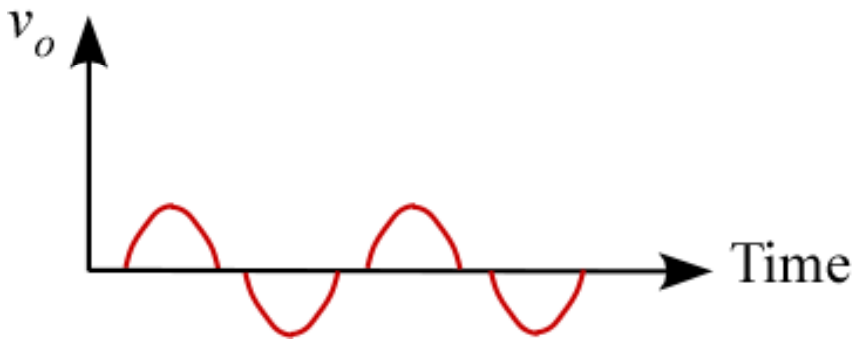
741 Op Amp – Second Stage

- **Second Stage**
  - Transistors Q_{16}, Q_{17} and Q_{13B} make up the intermediate stage
  - Q_{16} acts as an emitter follower
  - Q_{17} is a common emitter amplifier
  - Output of second stage is at collector of Q_{17}
  - Capacitor C_C provides Miller compensation
  - Capacitor C_C occupies large area in chip

Amplifier - Class B Operation

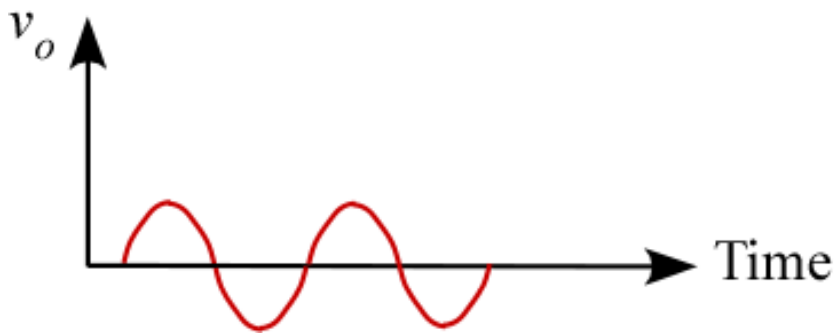
- **Class B Amp**
  - Arrangement saves power
  - Transistors turn on only when signal is applied
  - *npn* sources current and *pnp* sinks current
  - Both transistors are cutoff when $v_I = 0$ ➔ crossover distortion

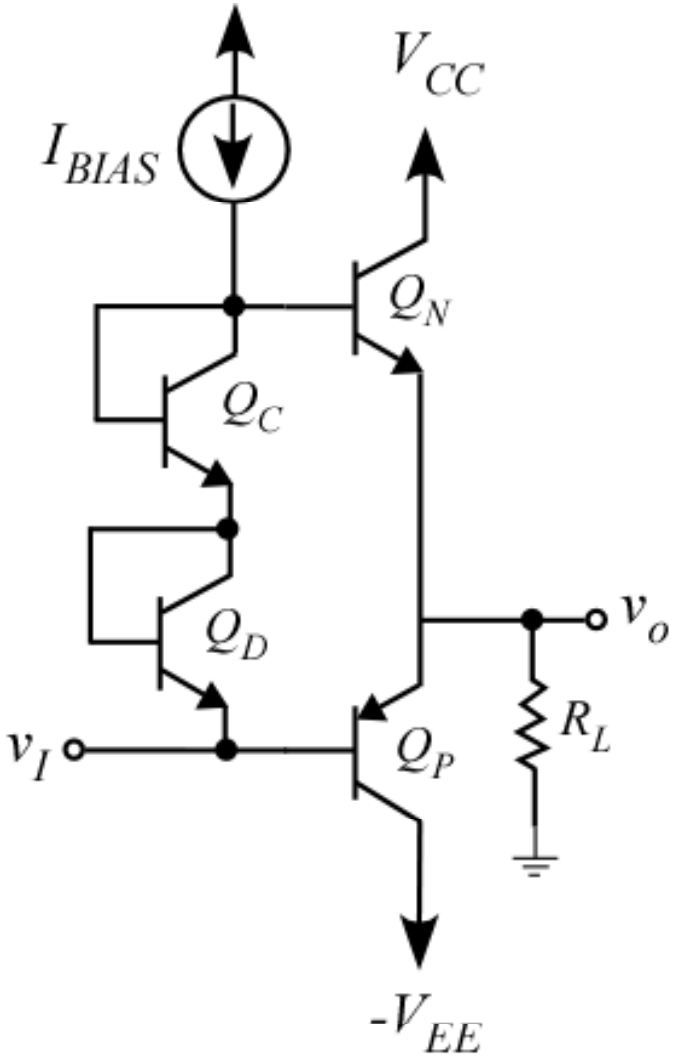




741 Op Amp – Output Stage

- **Output Stage**
  - Class AB operation that reduces crossover distortion
  - Transistors Q_{14} and Q_{20} make up output stage
  - Q_{18} and Q_{19} provide bias to Q_{14} and Q_{20}





741 Op Amp – DC Analysis

$$NPN: I_S = 10^{-14}\,A,\ \beta = 200,\ V_A = 125\,V$$

$$PNP: I_S = 10^{-14}\,A,\ \beta = 50,\ V_A = 50\,V$$

Q_{13}, Q_{14} and Q_{20} are nonstandard devices.
Q_{13} has Q_{13A} and Q_{13B}

$$I_{SA} = 0.25\times10^{-14}\,A, \qquad I_{SB} = 0.75\times10^{-14}\,A$$

$$I_{REF} = \frac{V_{CC} - V_{EB12} - V_{BE11} - (V_{EE})}{R_5} = 0.73\,mA$$

741 Op Amp – Input Stage DC Analysis

- **Input Stage**
  - Q_{11} & Q_{10} are a Widlar current source

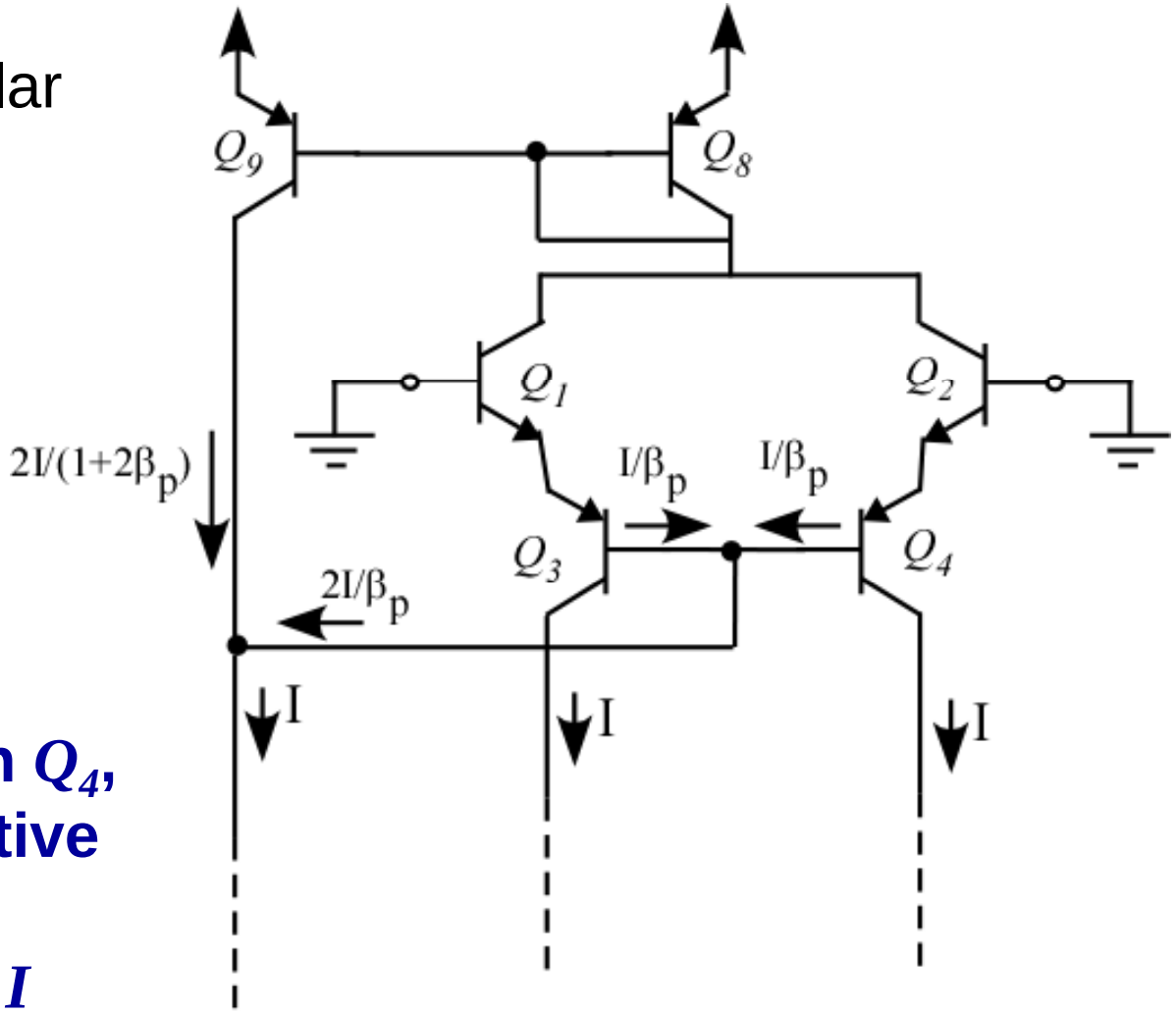
$$V_{BE11} - V_{BE10} = I_{C10} R_4$$

$$(Assume\ I_{S10} = I_{S11})$$

$$V_T \ln \frac{I_{REF}}{I_{C10}} = I_{C10} R_4$$

$$I_{C10} = 19\ \mu A$$

Transistors Q_1 through Q_4, Q_8 and Q_9 form a negative feedback loop that stabilizes the value of I



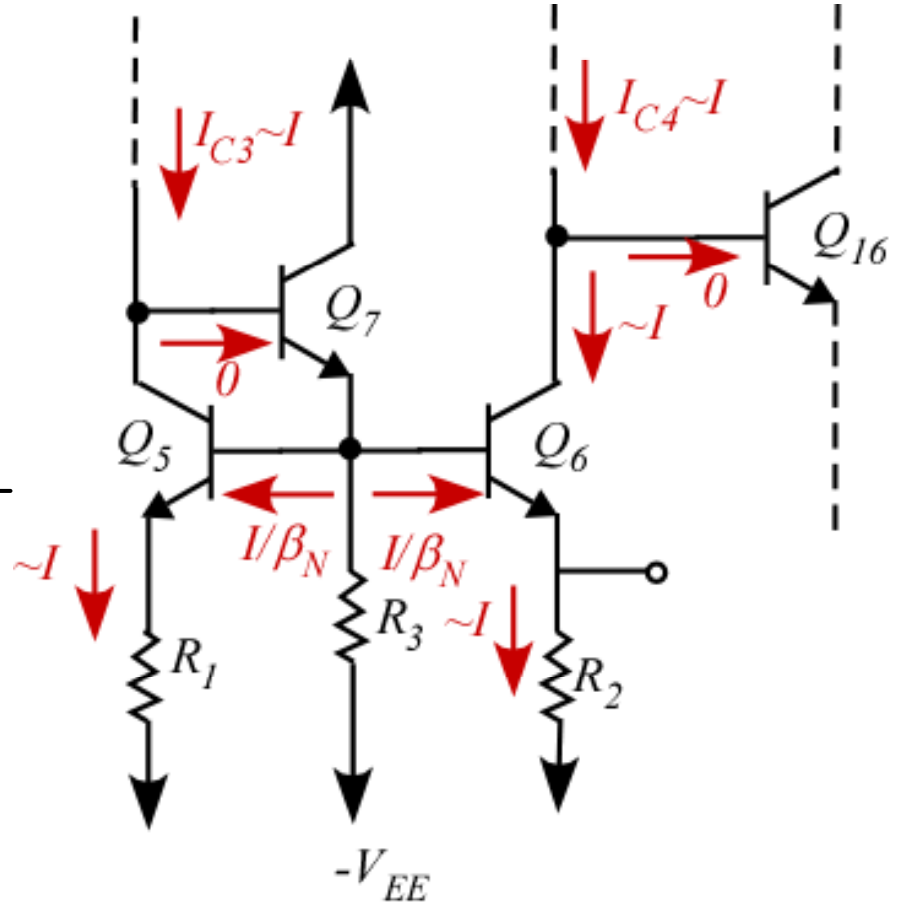
741 Op Amp – Input Stage DC Analysis

$$I_{C6} \approx I$$

$$I_{C5} \approx I$$

$$I_{C7} \approx I_{E7} = \frac{2I}{\beta_N} + \frac{V_{BE6} + IR_2}{R_3}$$

$$V_{BE6} = V_T \ln \frac{I}{I_S}$$



741 Op Amp – Output Stage DC Bias

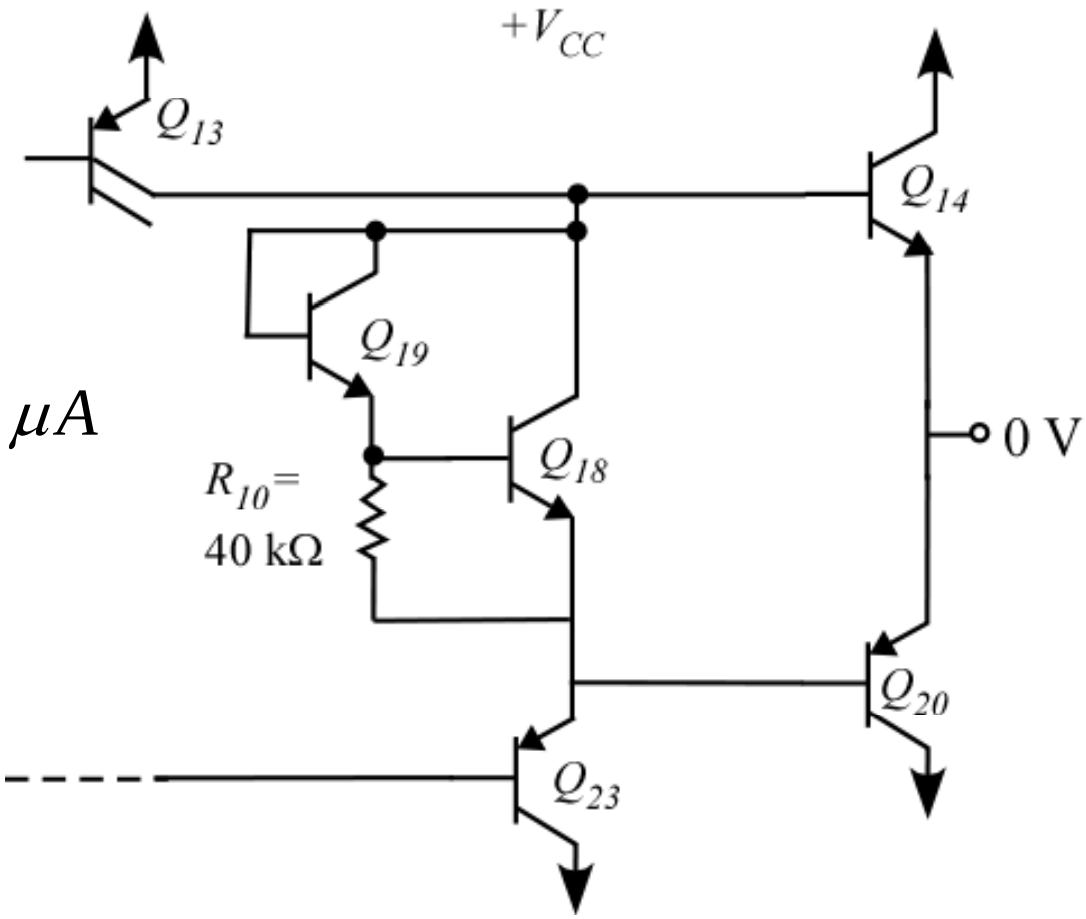
- **Output Stage**
  - Q_{13} delivers a current of 0.25 I_{REF}
  - Class AB operation

$$I_{C23} \simeq I_{E23} \simeq 0.25 I_{REF} = 180\ \mu A$$

$$I_{E18} = 165\ \mu A$$

$$I_{C19} \simeq 15.8\ \mu A$$

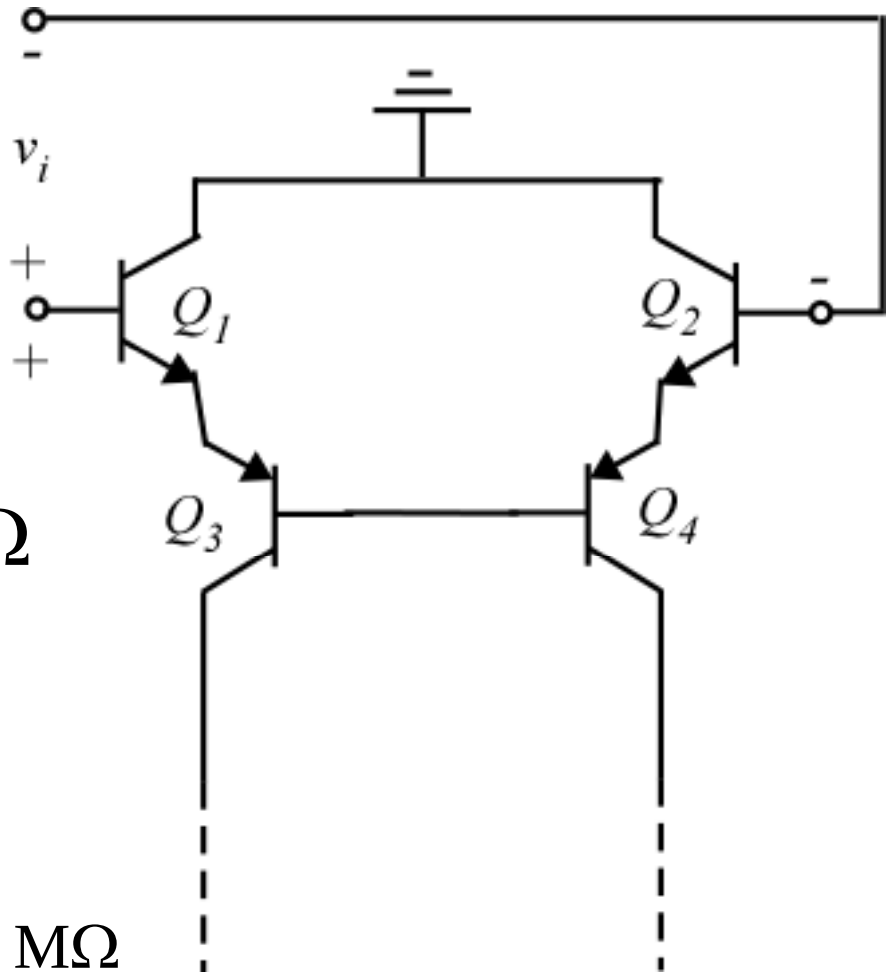
$$I_{C14} \simeq 154\ \mu A$$



Small-Signal Analysis – Input Stage

$$i_e = \frac{v_i}{4r_e}$$

r_e is the emitter resistance of Q_1-Q_4



$$r_e = \frac{V_T}{I} = \frac{25\,mV}{9.5\,\mu A} = 2.63\,k\Omega$$

$$R_{id} = 4\left(\beta_N + 1\right) r_e$$

For $\beta_N = 200$, we obtain $R_{id} = 2.1$ MΩ

Small-Signal Analysis – Input Stage

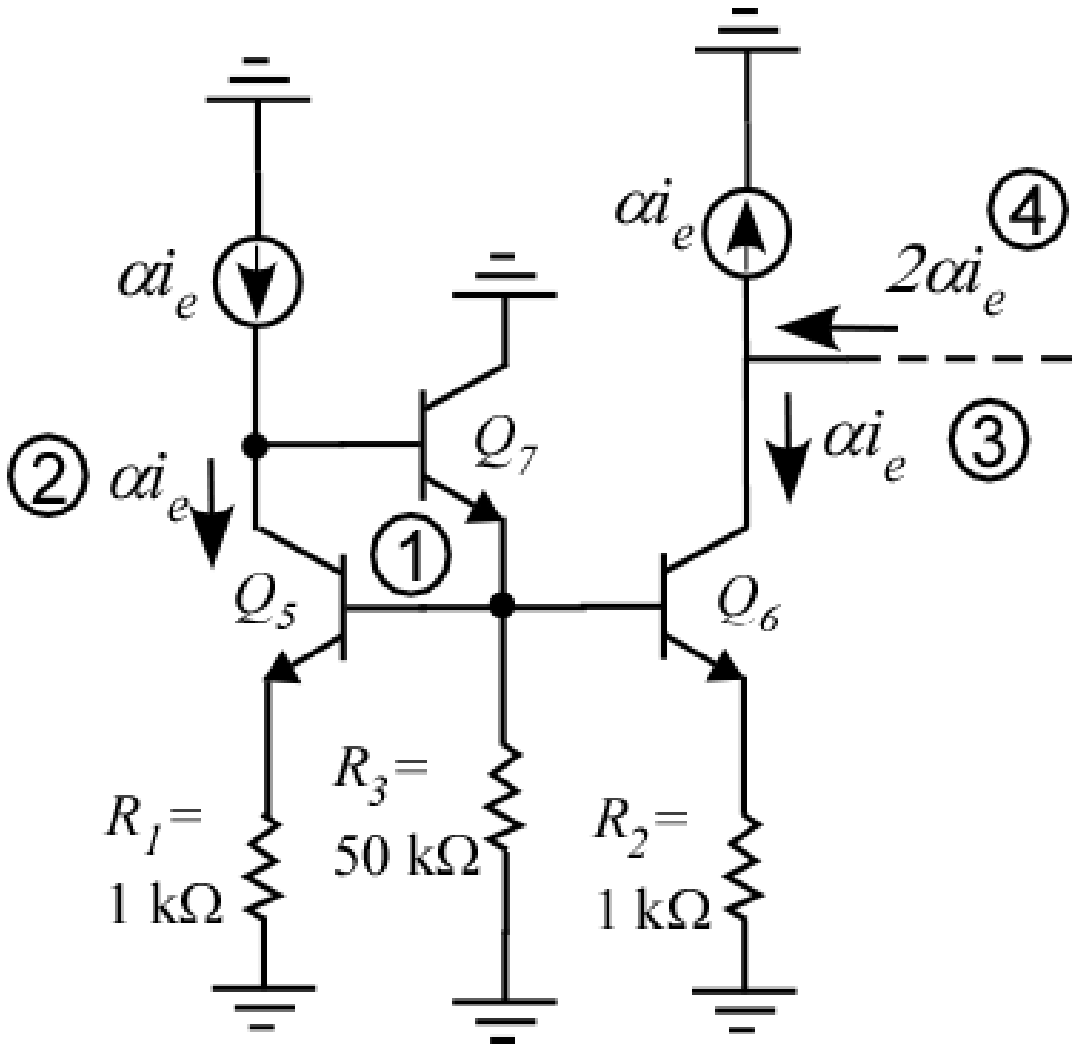
$$i_o = 2\alpha i_e$$

$$G_{m1} \equiv \frac{i_o}{v_i} = \frac{\alpha}{2r_e}$$

$$r_e = 2.63\,k\Omega$$

$$\alpha \approx 1$$

$$G_{m1} = 1/5.26\,mA/V$$

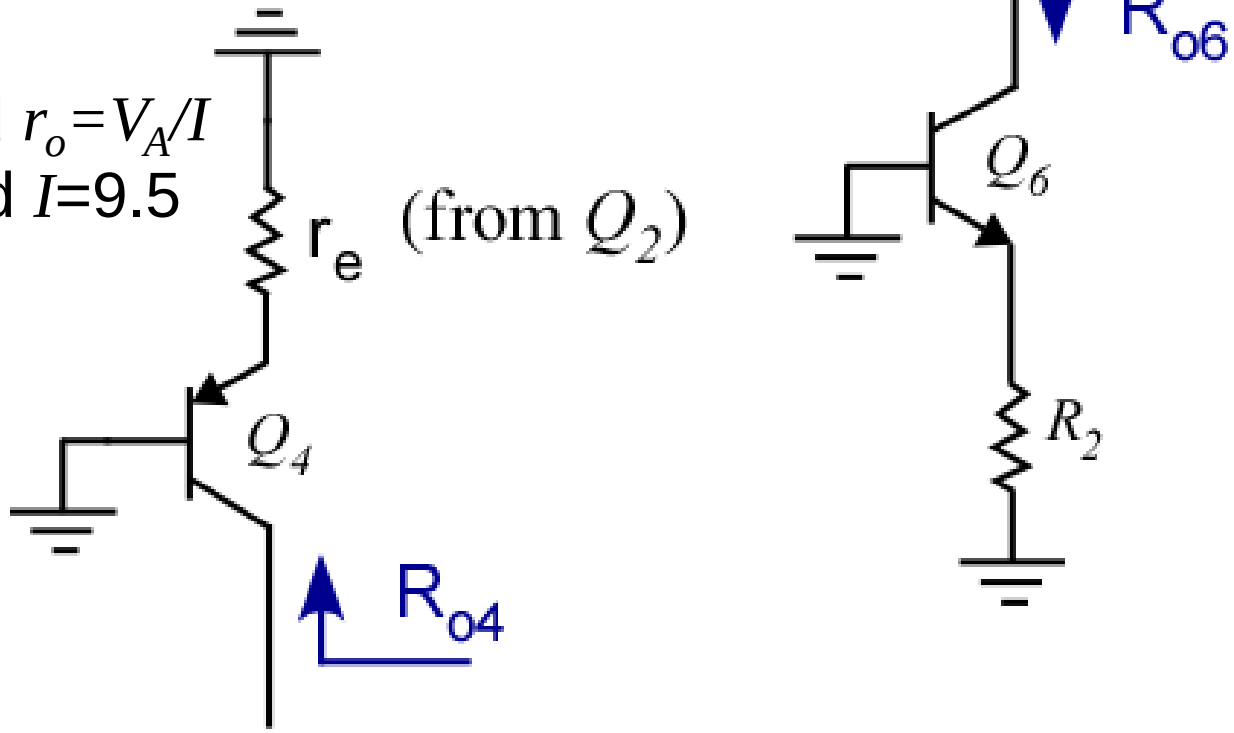


Small-Signal Analysis – Input Stage

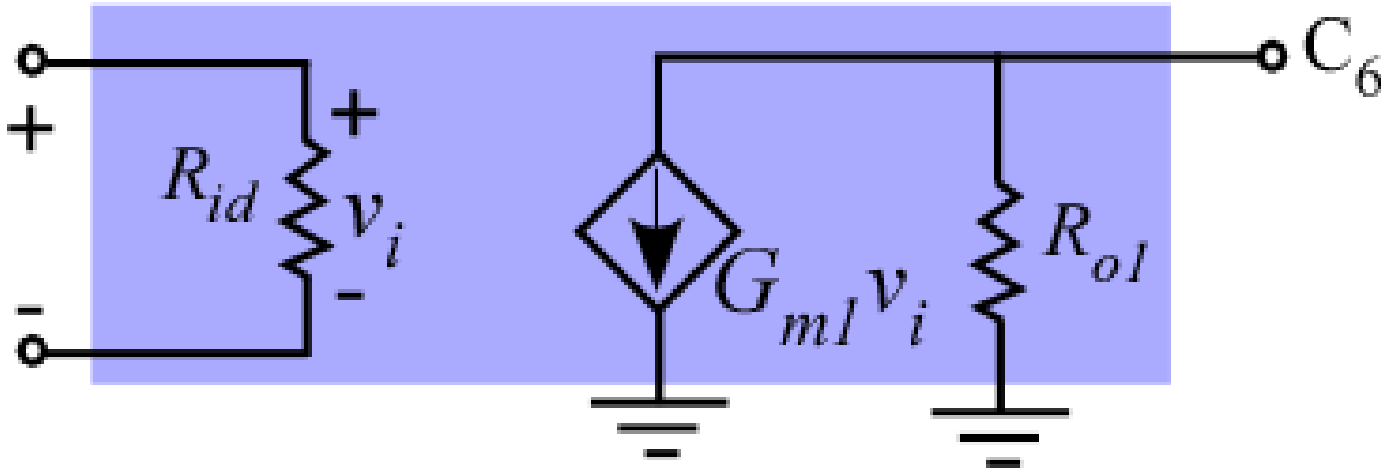
Output resistance of input stage. Seen from collector of Q_6

$$R_o = r_o\left[1 + g_m\left(R_E \,//\, r_\pi\right)\right]$$

$R_E = r_e$=2.63 kΩ and $r_o = V_A/I$ where V_A=50 V and I=9.5 μA➔r_o=5.26 MΩ

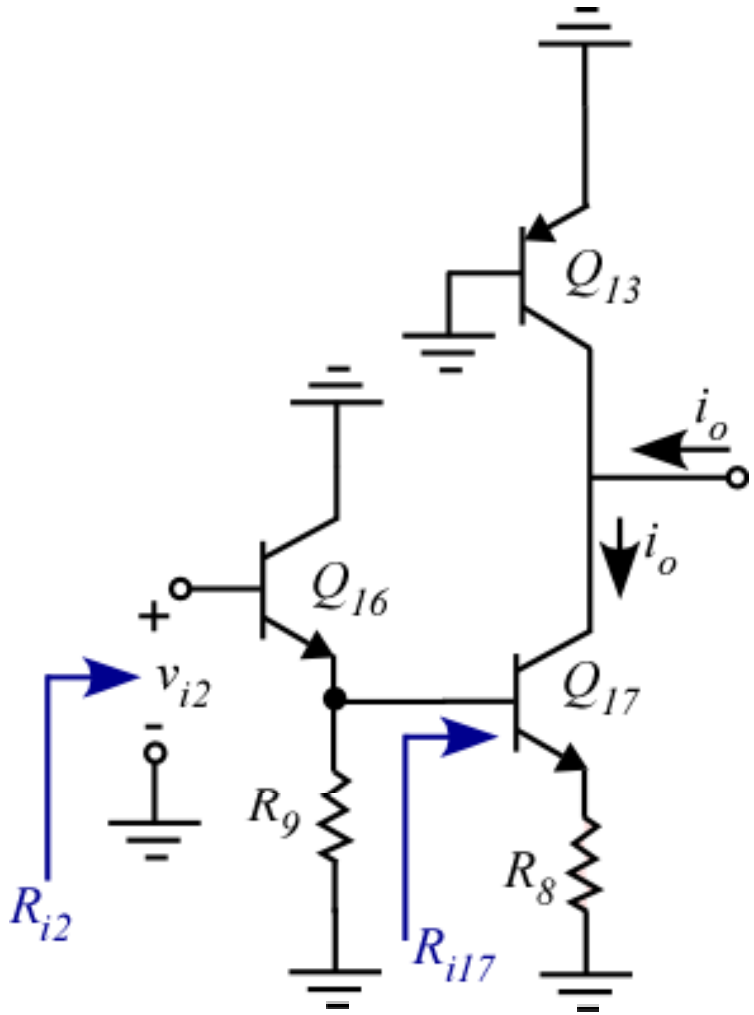


Input Stage – Incremental Model

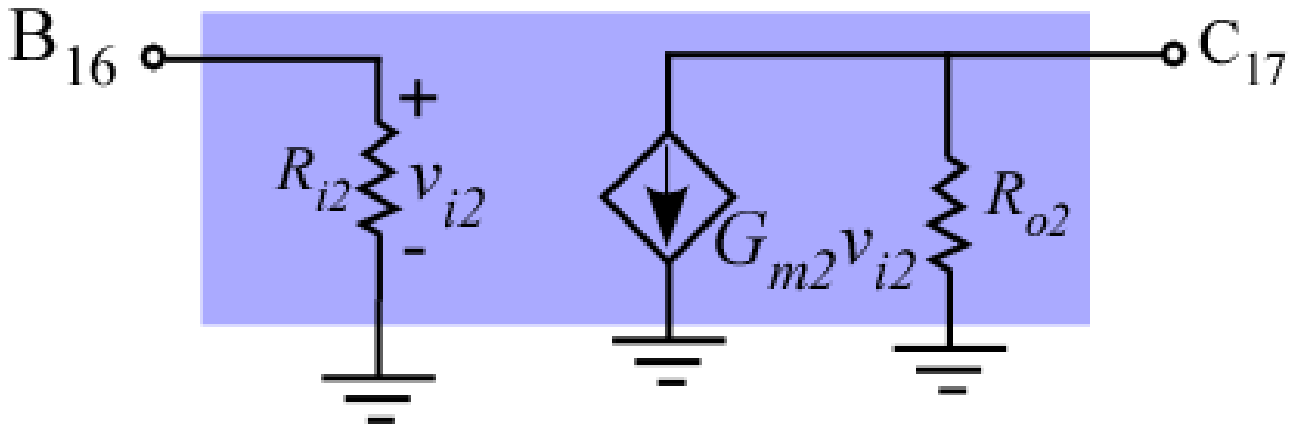


Develop equivalent circuit for input stage

Small-Signal Analysis – Second Stage



Second Stage – Incremental Model

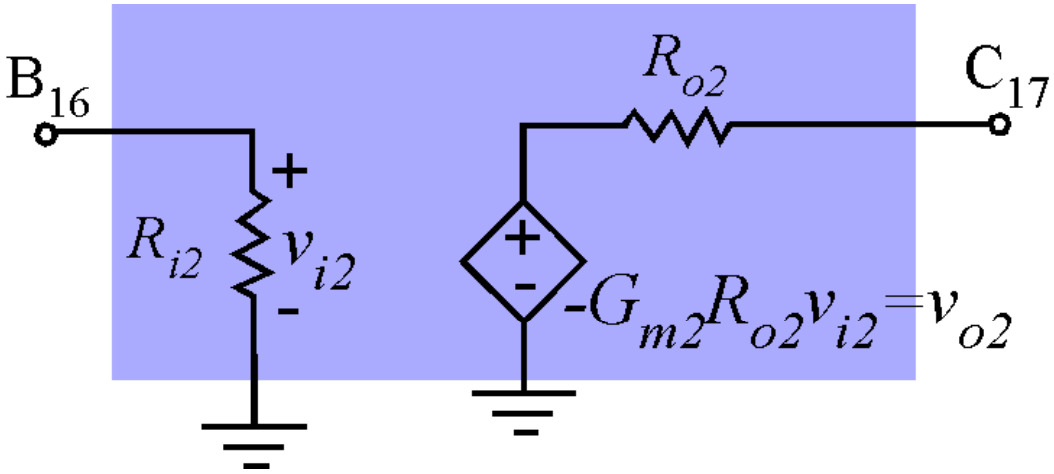


Develop equivalent circuit for second stage

Small-Signal Analysis – Second Stage

Input Resistance

R_{i2} is found by inspection:



$$R_{i2} = (\beta_{16}+1)\left[r_{e16} + R_9 \,||\, (\beta_{17}+1)(r_{e17}+R_8)\right]$$

$$R_{i2} = 4\,M\Omega$$

Small-Signal Analysis – Second Stage

Transconductance

The transconductance G_{m2} is the output current to input voltage

$$i_{c17} = \frac{\alpha v_{b7}}{r_{e17} + R_8}$$

$$v_{b17} = v_{12} \frac{\left(R_9 \,//\, R_{i17} \right)}{\left(R_9 \,//\, R_{i17} \right) + r_{e16}}$$

$$R_{i17} = \left(\beta_{17} + 1 \right) \left(r_{e17} + R_8 \right)$$

$$G_{m2} \equiv \frac{i_{c17}}{v_{i2}} = 6.5\, mA/V$$

Small-Signal Analysis – Second Stage

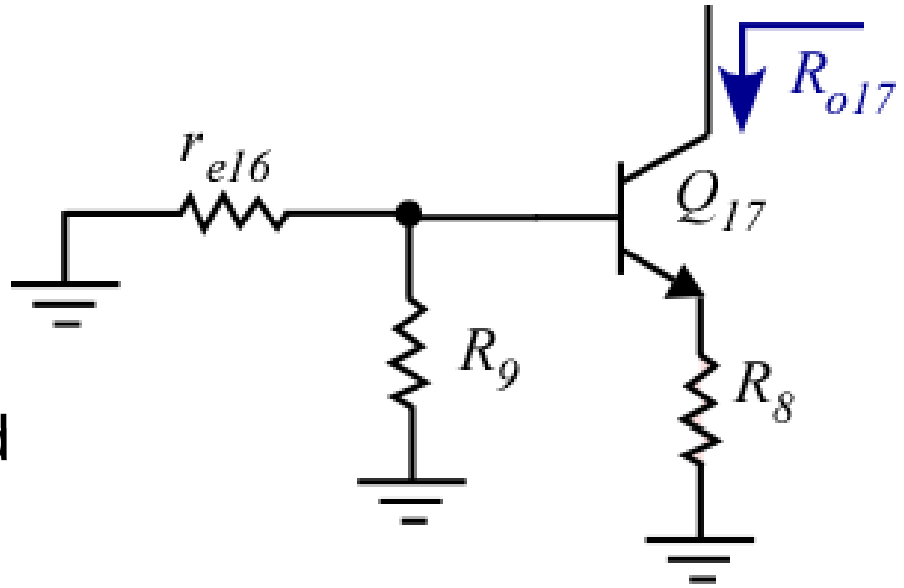
Output Resistance

Find resistance looking into into output terminal

$$R_{o2} = \left(R_{o13B} \,//\, R_{o17} \right)$$

First component

$$R_{o13B} = r_{o13B} = 90.9\, k\Omega$$

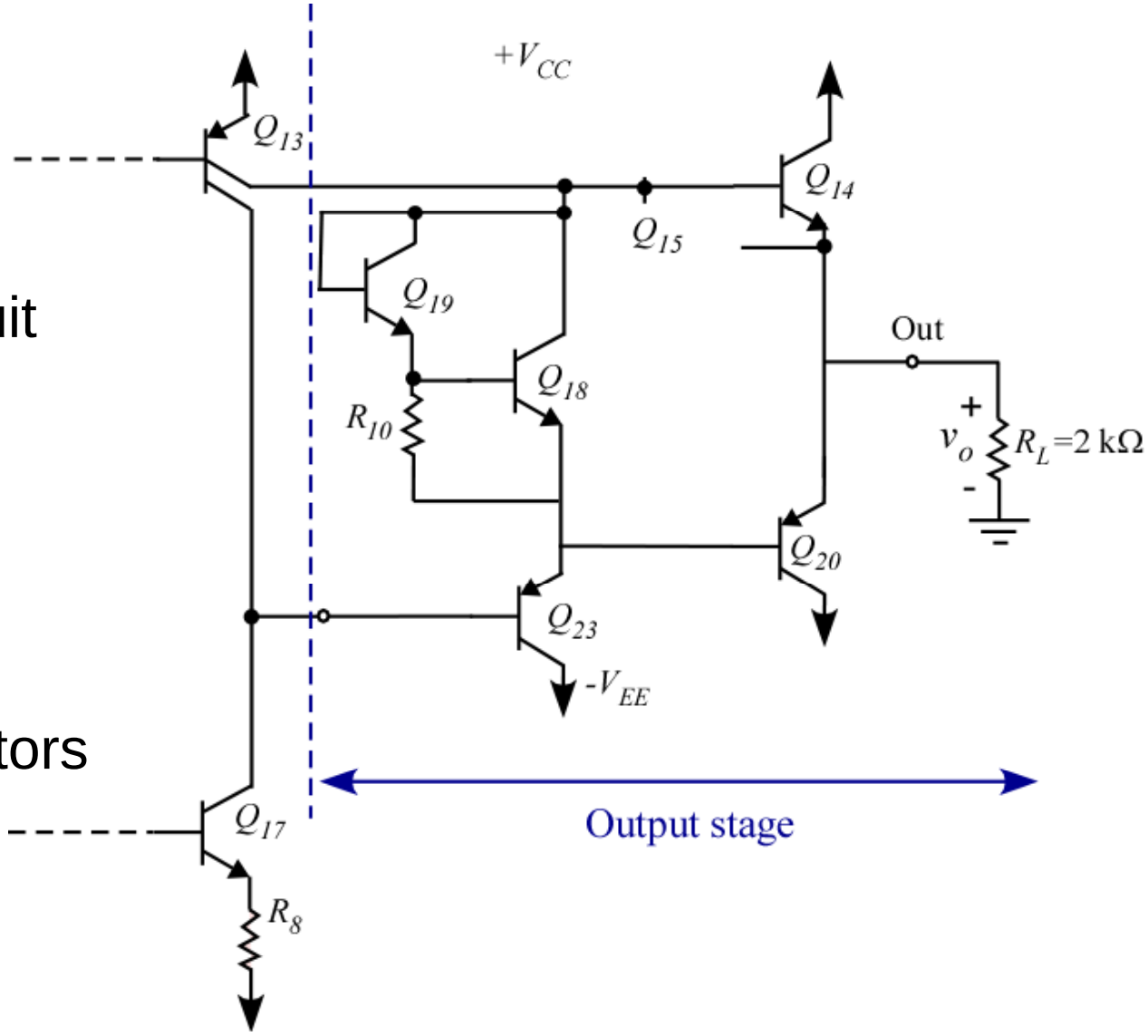


Second component is found looking into collector of Q_{17}

$$R_{o17} = 787\, k\Omega \qquad R_{o2} = 81\, k\Omega$$

Small-Signal Analysis – Output Stage

- **Characteristics**
  - AB class circuit
  - Driven by Q_{17}
  - Q_{23} is follower
  - Q_{18} & Q_{19} providing bias
  - Q_{14} & Q_{20} are output transistors



Output Stage

Output Voltage Limits

Maximum positive voltage limited by saturation of Q_{13}

$$v_{o\max} = V_{CC} - V_{CEsat} - V_{BE14}$$

About 1V below V_{CC}

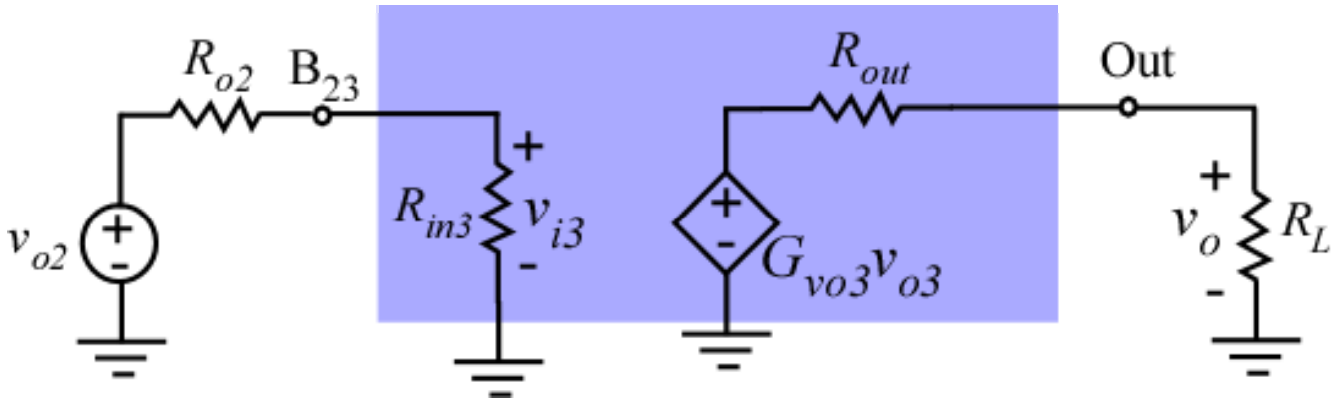
Minimum output voltage limited by saturation of Q_{17}

$$v_{o\min} = -V_{EE} + V_{CEsat} + V_{EB23} + V_{EB20}$$

About 1.5 V above -V_{EE}

Output Stage – Incremental Circuit

Construct model



$$v_{o2} = -G_{m2}R_{o2}v_{i2}$$

G_{m2}=6.5 mA/V and R_{o2}=81 kΩ

Output Stage – Incremental Model

- **Finding R_{in3}**
  - Assume Q_{20} to have 5 mA
  - Resistance looking into base of Q_{20} is about $\beta_{20}R_L$
  - Assume β_{20}=50 and R_L=2 kΩ➔resistance into Q_{20}=100 kΩ Q_{18} & Q_{19} providing bias
  - Place above resistance in parallel with resistance of Q_{13A} (about 280 kΩ) [resistance of Q_{18}-Q_{19} network small and can be neglected]

Assuming β_{23}=50

$$R_{in3} \approx \beta_{23}\left(100\ k\Omega // 280\ k\Omega\right) = 50 \times 74 = 3.7\ M\Omega$$

Output Stage – Incremental Model

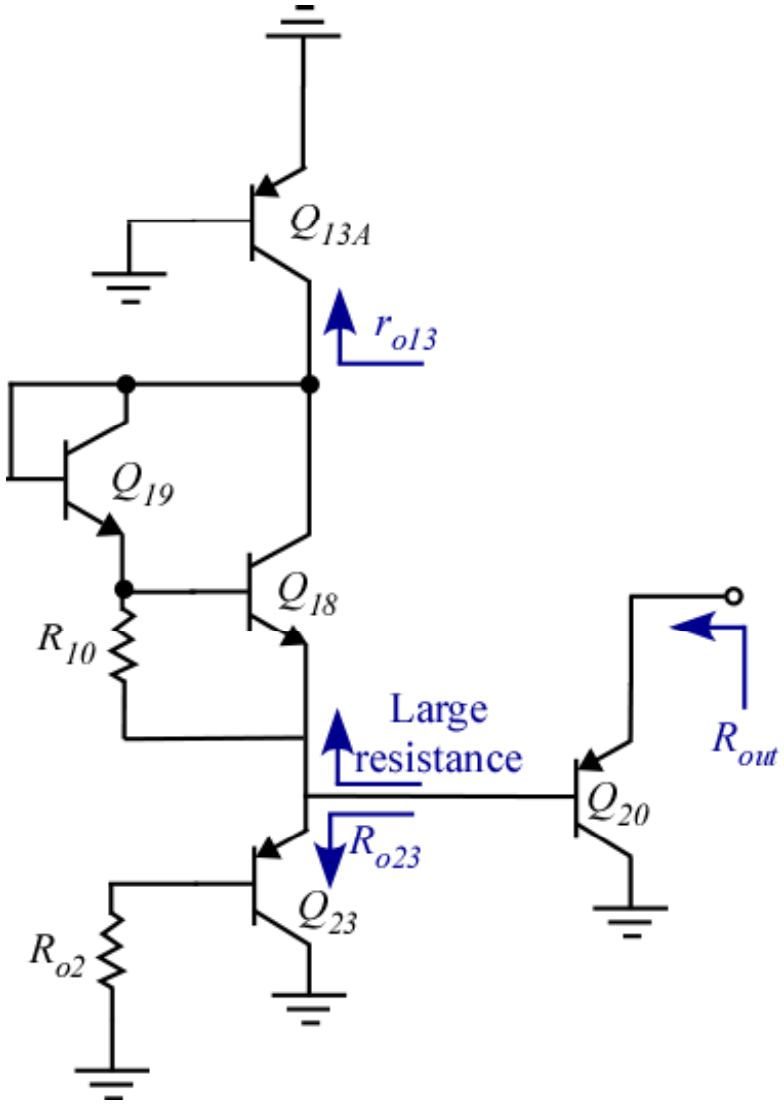
Looking into emitter of Q_{23}

$$R_{o23} = \frac{R_{o2}}{\beta_{23}+1} + r_{e23}$$

Using R_{o2}=81 kΩ, β_{23}=50, r_{e23}=25/0.18 = 139 Ω gives R_{o23}=1.73 kΩ

$$R_{out} = \frac{R_{o23}}{\beta_{20}+1} + r_{e20}$$

For β = 50, R_{out}=34 Ω



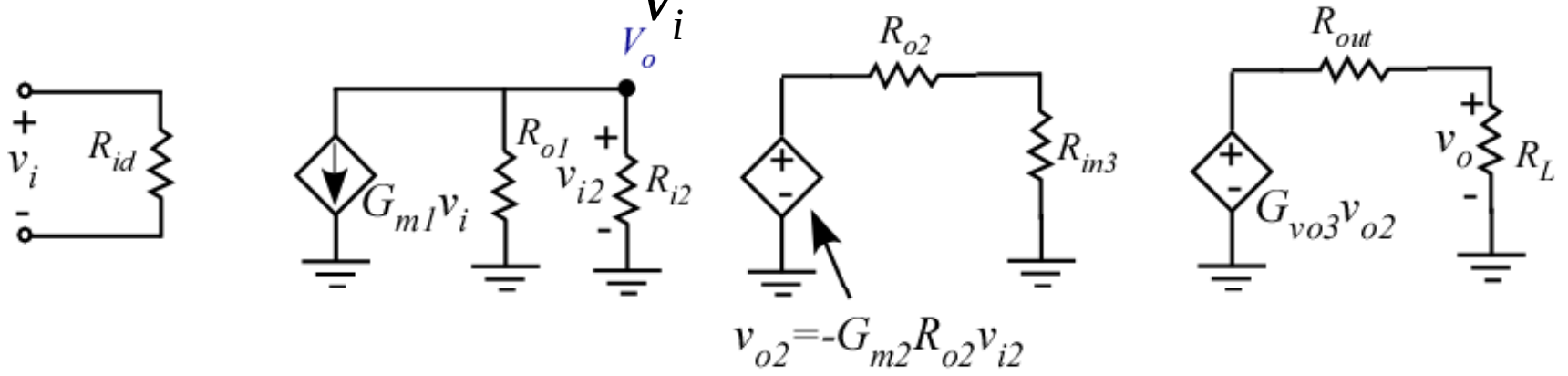
Overall Gain

$$\frac{v_o}{v_i} = \frac{v_{i2}}{v_i}\frac{v_{o2}}{v_{i2}}\frac{v_o}{v_{o2}}$$

$$\frac{v_o}{v_i} = -G_{m1}\left(R_{o1} \,//\, R_{12}\right)\left(-G_{m2}R_{o2}\right)G_{vo3}\frac{R_L}{R_L + R_{out}}$$

$$A_o \equiv \frac{v_o}{v_i} = -476.1\times\left(-526.5\right)\times 0.97 = 243{,}147\ V/V$$

$$A_o \equiv \frac{v_o}{v_i} = 107.7\ dB$$



741 Op Amp - Frequency Response

Miller capacitance due to C_C between the base of Q_{16} and ground is

$$C_{in} = C_C\left(1+\left|A_2\right|\right)$$

Resistance between the base of Q_{16} and ground is

$$R_t = \left(R_{o1} \,//\, R_{i2}\right) = \left(6.7\ M\Omega \,//\, 4\ M\Omega\right)$$

Dominant pole is at

$$f_P = \frac{1}{2\pi C_{in} R_t} = 4.1\ Hz$$

Unity gain-bandwith is

$$f_t = A_0 f_{3dB} = 243{,}147 \times 4.1 \approx 1\ MHz$$

Conclusion - Design of Op Amps

1. Designer starts with building blocks whose performance can be analyzed to a first order approximation by hand

2. This step provides insight to the designer as the design of the circuit develops

3. At some point designer must turn to computer analysis programs such as SPICE. This will provide speed and accuracy to the design process