ECE 442
Solid-State Devices & Circuits

15. Differential Amplifiers

Jose E. Schutt-Aine
Electrical & Computer Engineering
University of Illinois
jschutt@emlab.uiuc.edu

Background

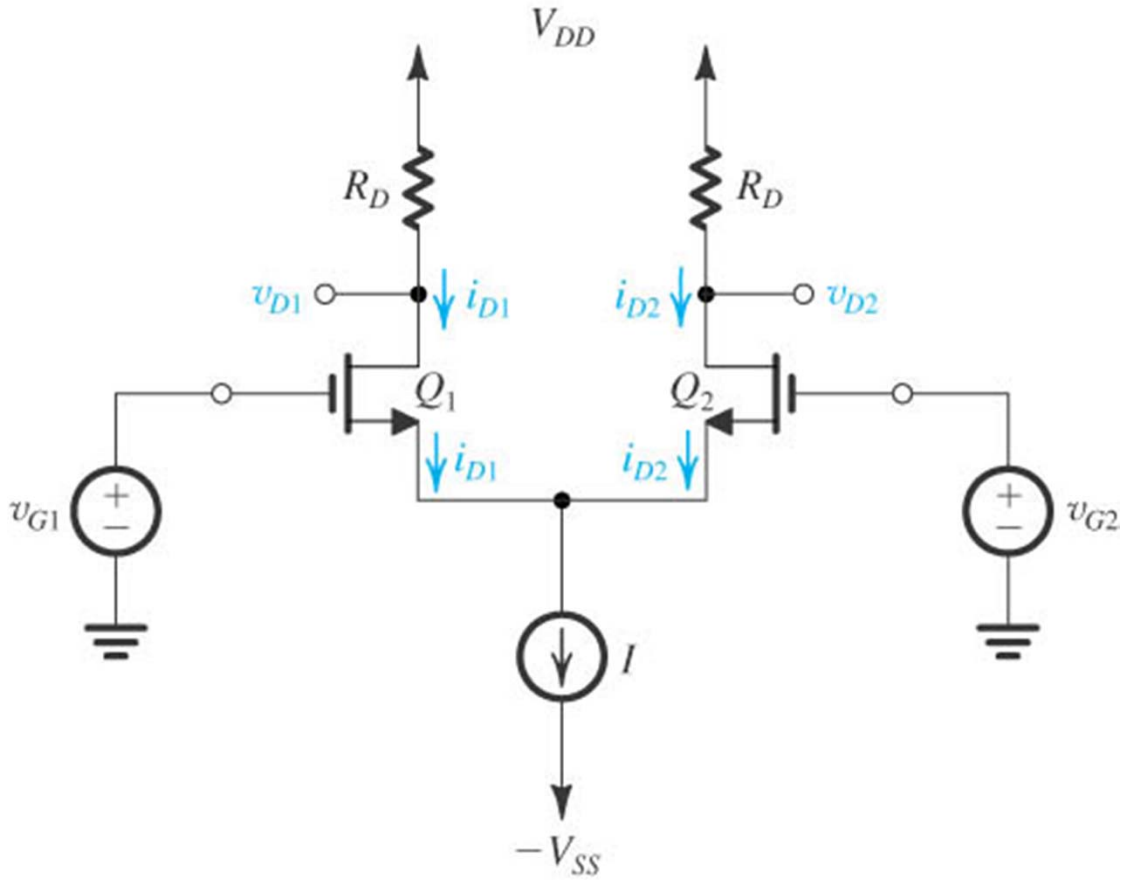
- **Differential Amplifiers**
  - The input stage of every op amp is a differential amplifier
  - Immunity to temperature effects
  - Ability to amplify dc signals
  - Well-suited for IC fabrication because
    - (a) they depend on matching of elements
    - (b) they use more components
  - Less sensitive to noise and interference
  - Enable to bias amplifier and connect to other stage without the use of coupling capacitors

Differential Amplifiers

- **Practical Considerations**
  - Both inputs to a differential amplifier may have different voltages applied to them
  - In the ideal situation with perfectly symmetric stages, the common-mode input would lead to zero output
  - Temperature drifts in each stage are often common-mode signals
  - Power supply noise is a common-mode signal and has little effect on the output signal

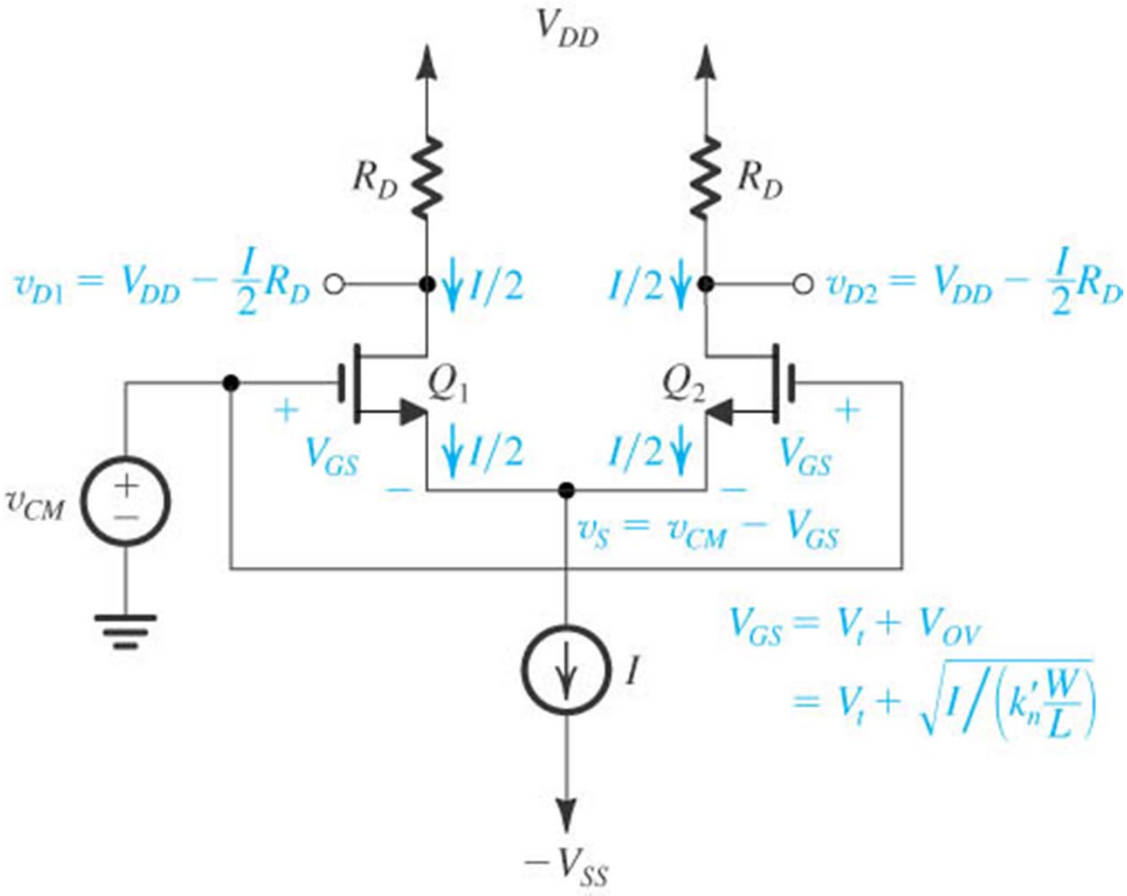
MOS Differential Pair

- Assume current source is ideal
- Transistors should not enter triode region



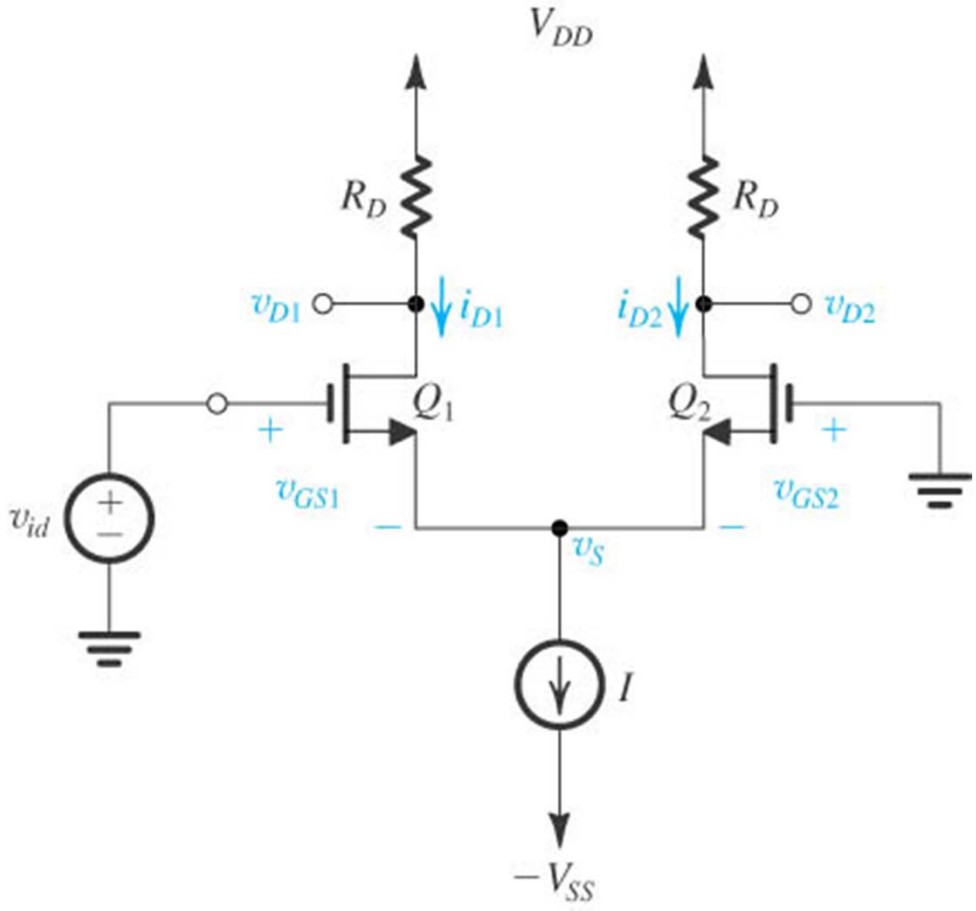
Common-Mode Operation

- Input voltage v_{cm} to both gates
- Difference in voltage between the two drains is zero

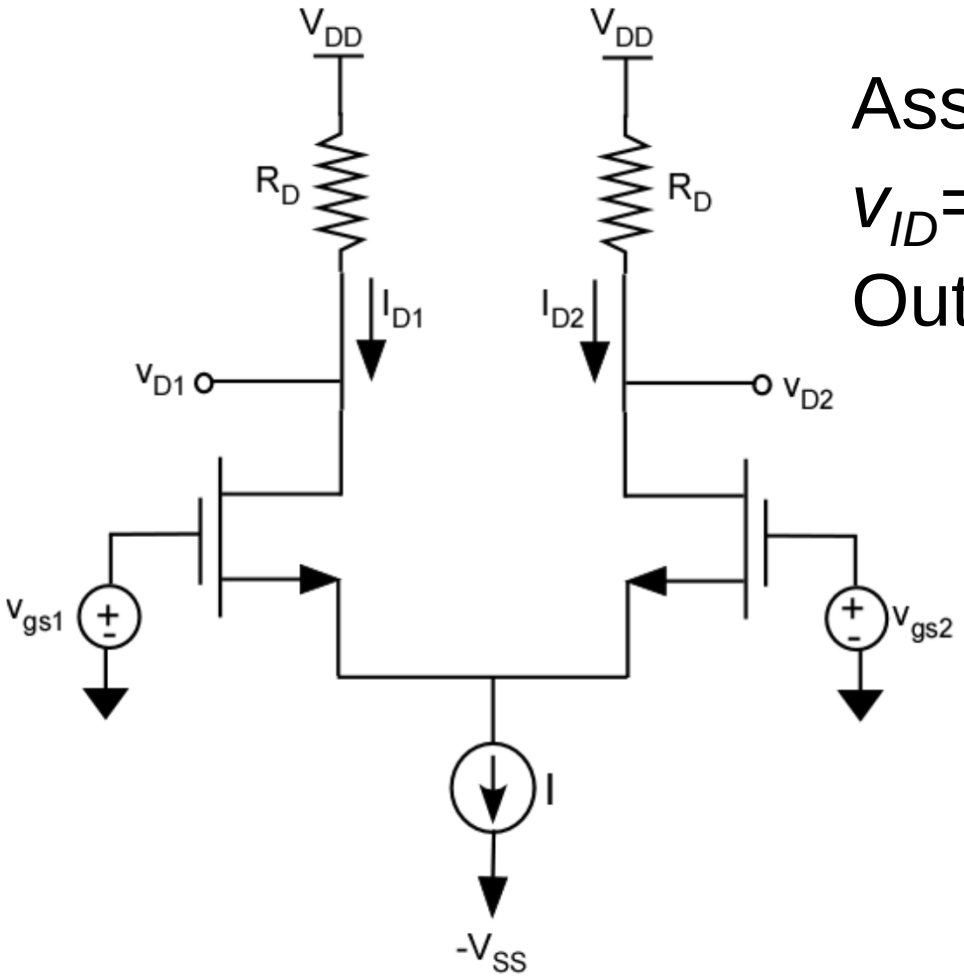


Differential Input Voltage

- Differential pair responds to differntial input signals by providing corresponding differential output signal between the two drains.



MOS Differential Pair

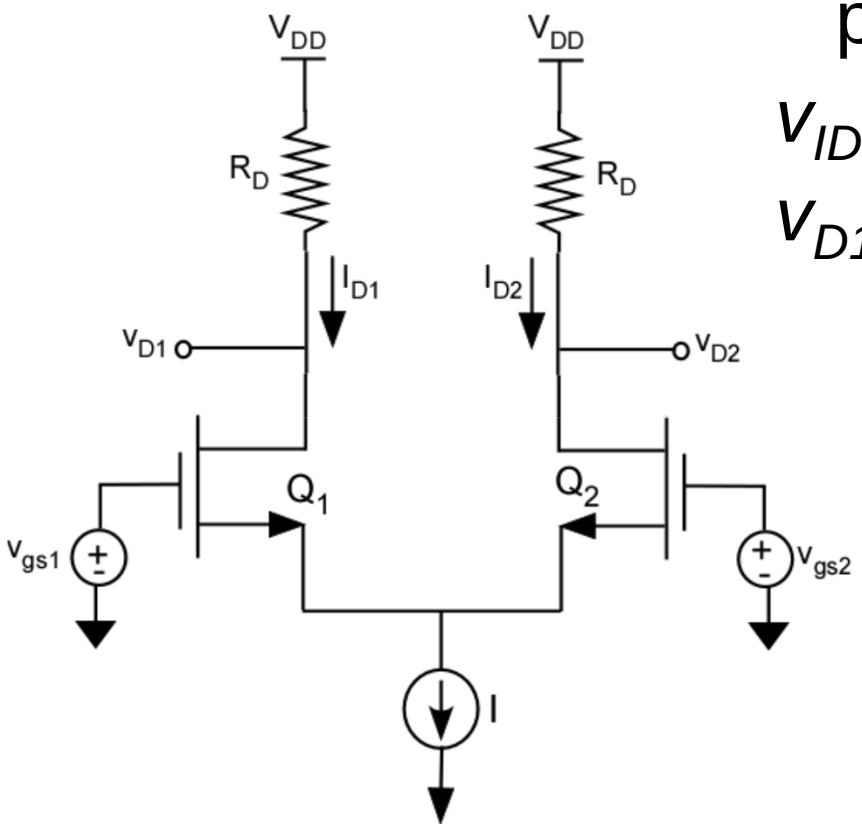


Assume current source is ideal

$v_{ID}=v_{gs1}-v_{gs2}$

Output is collected as $v_{D2}-v_{D1}$

MOS Differential Pair



- If v_{ID} is positive, v_{D2}-v_{D1} is positive

$v_{ID}>0 \rightarrow v_{gs1}>v_{gs2} \rightarrow I_{D1} > I_{D2}$

v_{D1} lower voltage point than v_{D2}

For proper operation, MOSFETS should not enter triode region

DC Analysis

$$V_{D1} = V_{DD} - \frac{IR_D}{2} \qquad V_{D2} = V_{DD} - \frac{IR_D}{2}$$

$$I_D = \frac{\mu C_{ox} W}{2L}\left(V_{GS} - V_T\right)^2 \qquad I_D = \frac{I}{2}$$

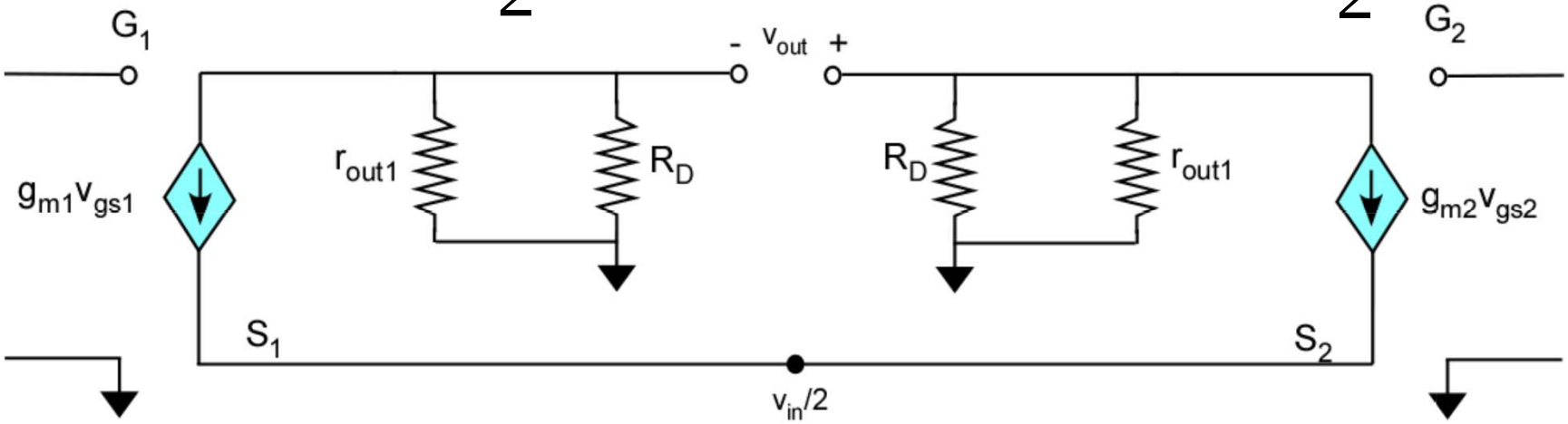
$$V_{GS} = V_T + \sqrt{\frac{LI}{\mu C_{ox} W}} \qquad V_{SQ} = -\left[V_T + \sqrt{\frac{LI}{\mu C_{ox} W}}\right]$$

Incremental Analysis

$$v_{g1} = v_{cm} + \frac{1}{2}v_{id} \qquad v_{g2} = v_{cm} - \frac{1}{2}v_{id}$$

Neglecting the body effect

$$v_{o1} = -g_m R_D' \frac{v_{in}}{2} \qquad v_{o2} = g_m R_D' \frac{v_{in}}{2}$$



$$R_D' = R_D \parallel r_{out} \qquad A_D = \frac{v_{o2} - v_{o1}}{v_{in}} = g_m R_D'$$

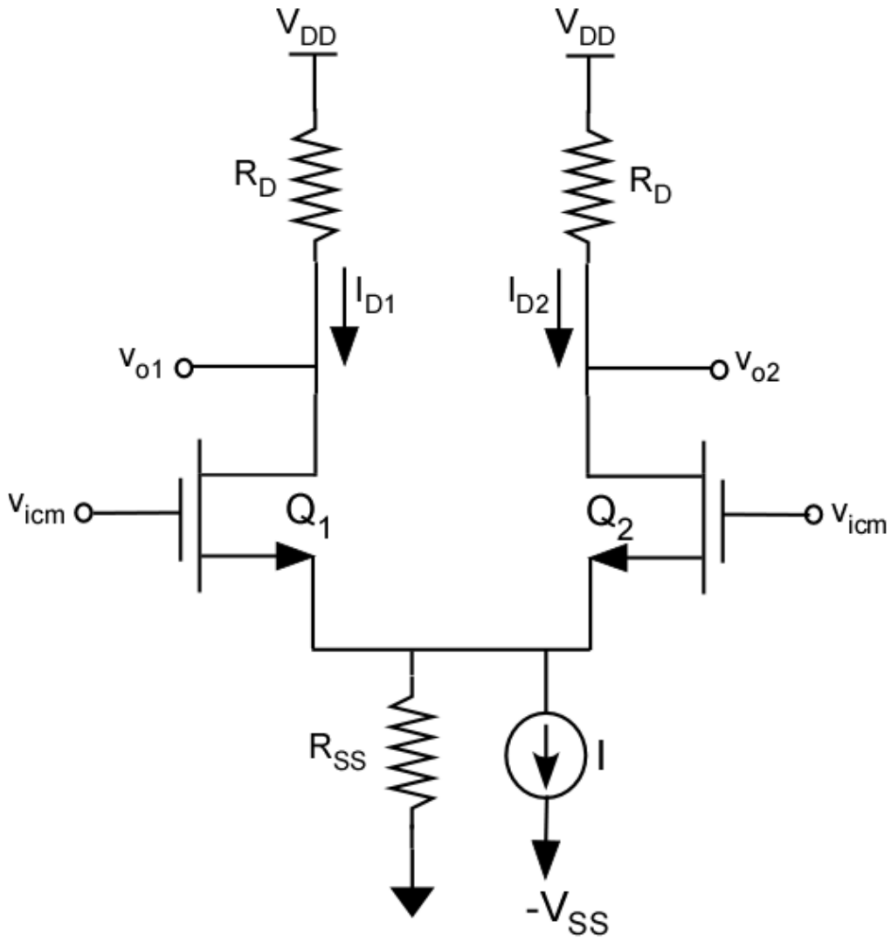
Frequency Response

When driven by a low-impedance signal source, the upper corner frequency is determined by the output circuit

$$f_{high} = \frac{1}{2\pi C_{out} R_D^{'}}$$

Common-Mode Rejection Ratio

$$\frac{v_{o1}}{v_{icm}} = \frac{v_{o2}}{v_{icm}} = \frac{R_D}{\frac{1}{g_m} + 2R_{SS}}$$



Assume $R_{SS} >> 1/g_m$

Common-Mode Rejection Ratio

(a) For ***single-ended*** output:

$$\frac{v_{o1}}{v_{icm}} = \frac{v_{o2}}{v_{icm}} \simeq \frac{R_D}{2R_{SS}}$$

$$\left|A_{cm}\right| = \frac{R_D}{2R_{SS}}, \quad \left|A_d\right| = \frac{1}{2} g_m R_D$$

$$CMRR = \left|\frac{A_d}{A_{cm}}\right| = g_m R_{SS}$$

Common-Mode Rejection Ratio

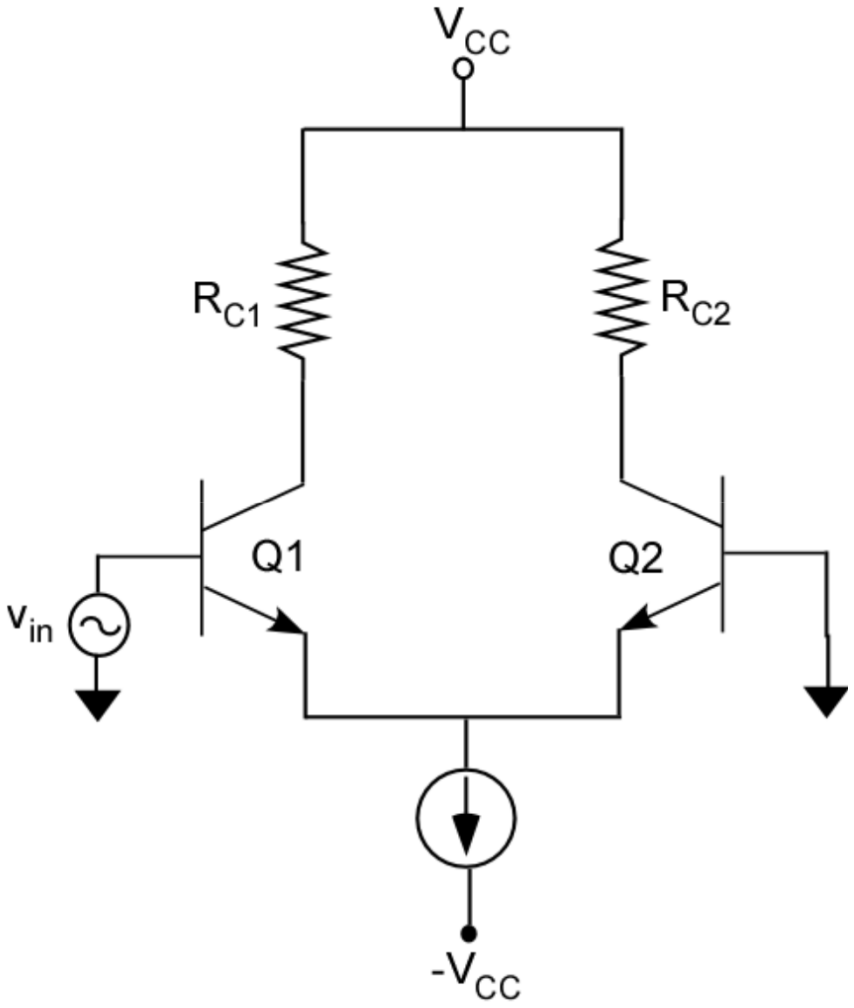
(b) For ***differential*** output:

$$A_{cm} = \frac{v_{o2} - v_{o1}}{v_{icm}} = 0$$

$$A_d = \frac{v_{o2} - v_{o1}}{v_{id}} = g_m R_D$$

$$CMRR = \infty$$

BJT Differential Pair



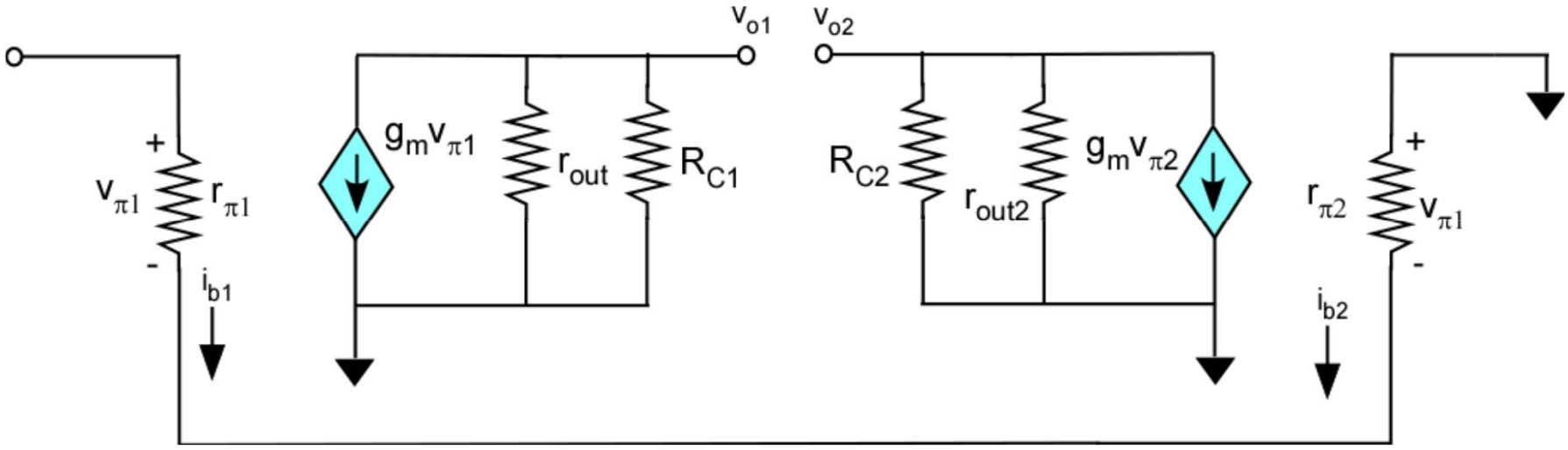
Assume perfect match between the devices and symmetry in the circuit

BJT Differential Pair

$$R_{in} = 2r_\pi \qquad i_{in} = \frac{v_{in}}{2r_\pi} \qquad R_C' = r_{out1} \parallel R_{c1} = r_{out2} \parallel R_{c2}$$

$$R_{c1} = R_{c2} = R_C$$

Base currents: $i_{b1} = \frac{v_{in}}{2r_\pi}$ $i_{b2} = \frac{-v_{in}}{2r_\pi}$



BJT Differential Pair – Incremental Model

$$v_{o1} = -g_m v_{\pi 1} R_C^{'} = -g_m R_C^{'} \frac{v_{in} r_\pi}{r_\pi} = -\frac{g_m R_C^{'}}{2} v_{in}$$

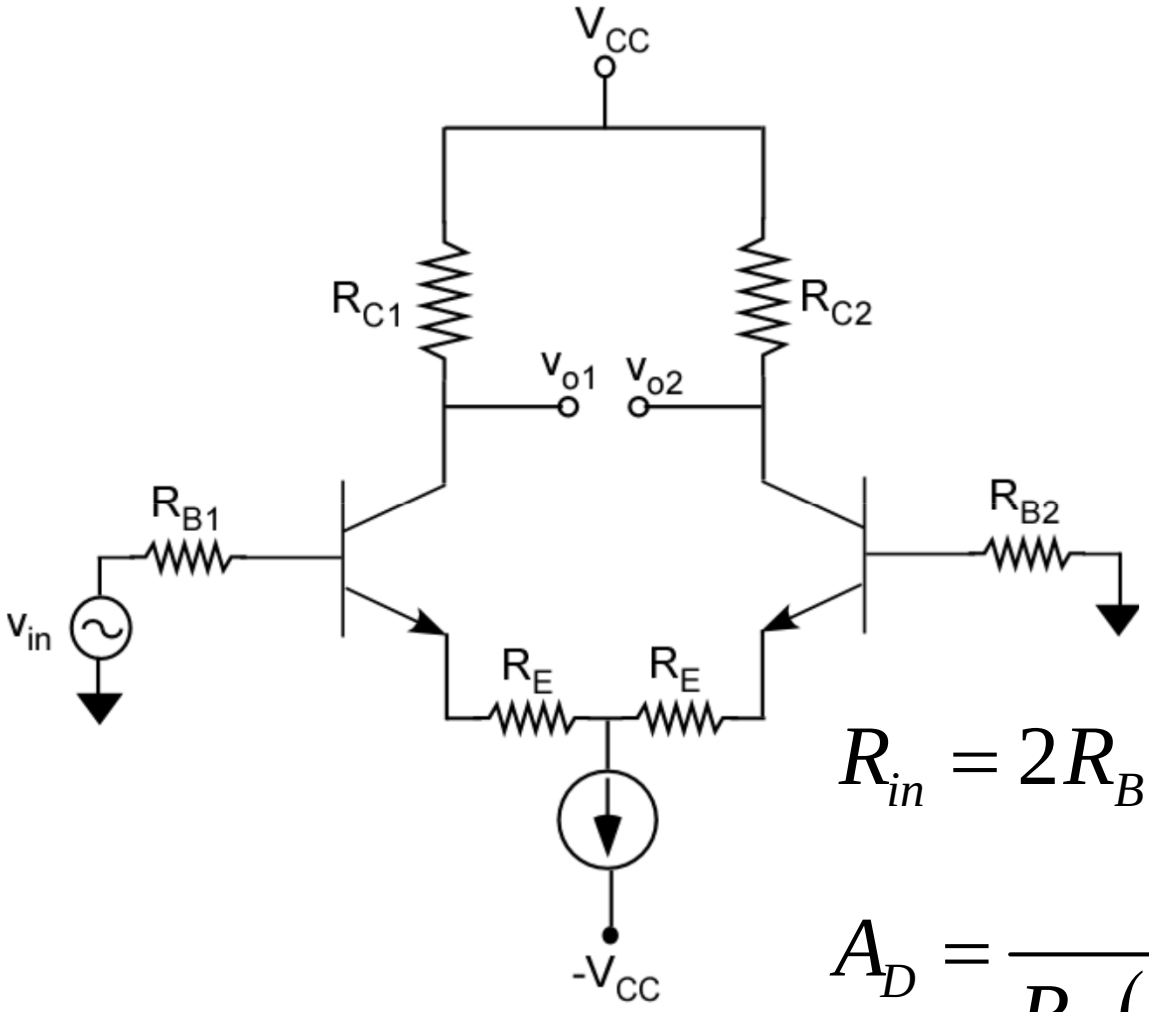
$$v_{o2} = g_m v_{\pi 2} R_C^{'} = g_m R_C^{'} \frac{v_{in} r_\pi}{r_\pi} = \frac{g_m R_C^{'}}{2} v_{in}$$

Single-ended gain of first stage: $A_{S1} = -g_m R_C^{'}$

Double-ended differential gain (with $v_{out}=v_{o2}-v_{o1}$):

$$A_D = \frac{g_m R_C^{'}}{2} - \frac{\left(-g_m R_C^{'}\right)}{2} = g_m R_C^{'} = \frac{\beta R_C^{'}}{r_\pi}$$

BJT Differential Pair – General



$$R_{B1} = R_{B2} = R_B$$

$$R_{C1} = R_{C2} = R_C$$

$$R_{in} = 2R_B + 2R_E\left(\beta + 1\right) + 2r_\pi$$

$$A_D = \frac{\beta R_C^{'}}{R_E\left(\beta + 1\right) + r_\pi + R_B}$$

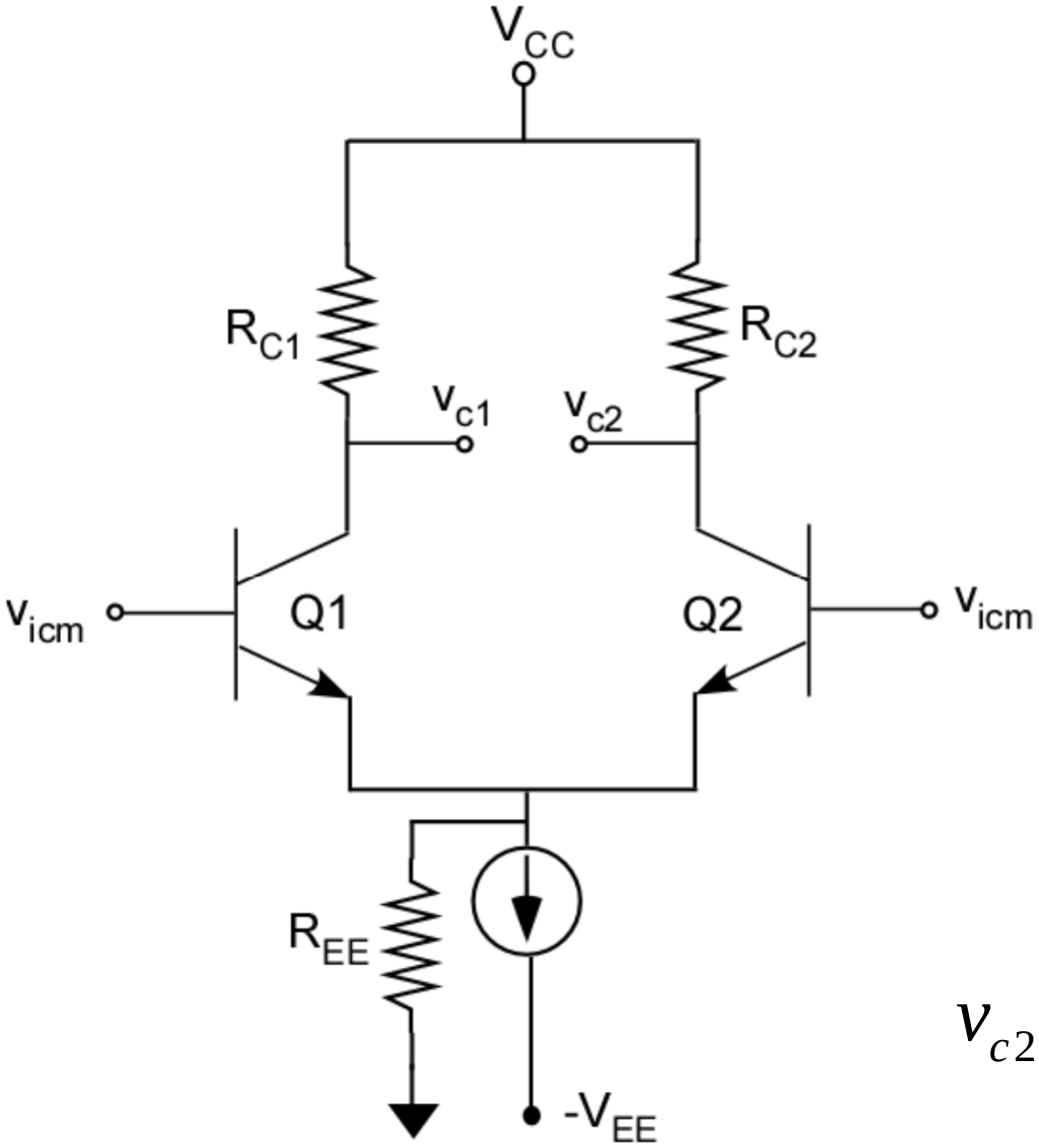
Differential Amplifiers - Observations

- **Observations**
  - The differential pair attenuates the input signal of each stage by a factor of one-half cutting the gain of each stage by one-half
  - The double-ended output causes the two single-ended gains to be additive
  - Thus, the voltage gain of a perfectly matched differential stage is equal to that of a single stage

Remarks on Differential Amplifiers

1. In many applications, the differential amplifier is not fed in a complementary fashion
2. Rather, the input signal may be applied to one of the input terminals while the other terminal is grounded
3. In this case, the signal voltage at the emitters will not be zero and thus the resistor R_{EE} will have an effect on the operation
4. However, if R_{EE} is large ($R_{EE} >> r_e$) as is usually the case, v_{id} will still divide equally between the 2 junctions
5. The operation of the differential amplifier will still be almost identical to that of the symmetrical feed and the CE equivalence can still be employed

Common Mode



$$R_{C2} = R_C + \Delta R_C$$

$$R_{C1} = R_C$$

Can show that

$$v_{c1} = -v_{icm} \frac{\alpha R_C}{2R_{EE} + r_e}$$

$$v_{c2} = -v_{icm} \frac{\alpha \left(R_C + \Delta R_C \right)}{2R_{EE} + r_e}$$

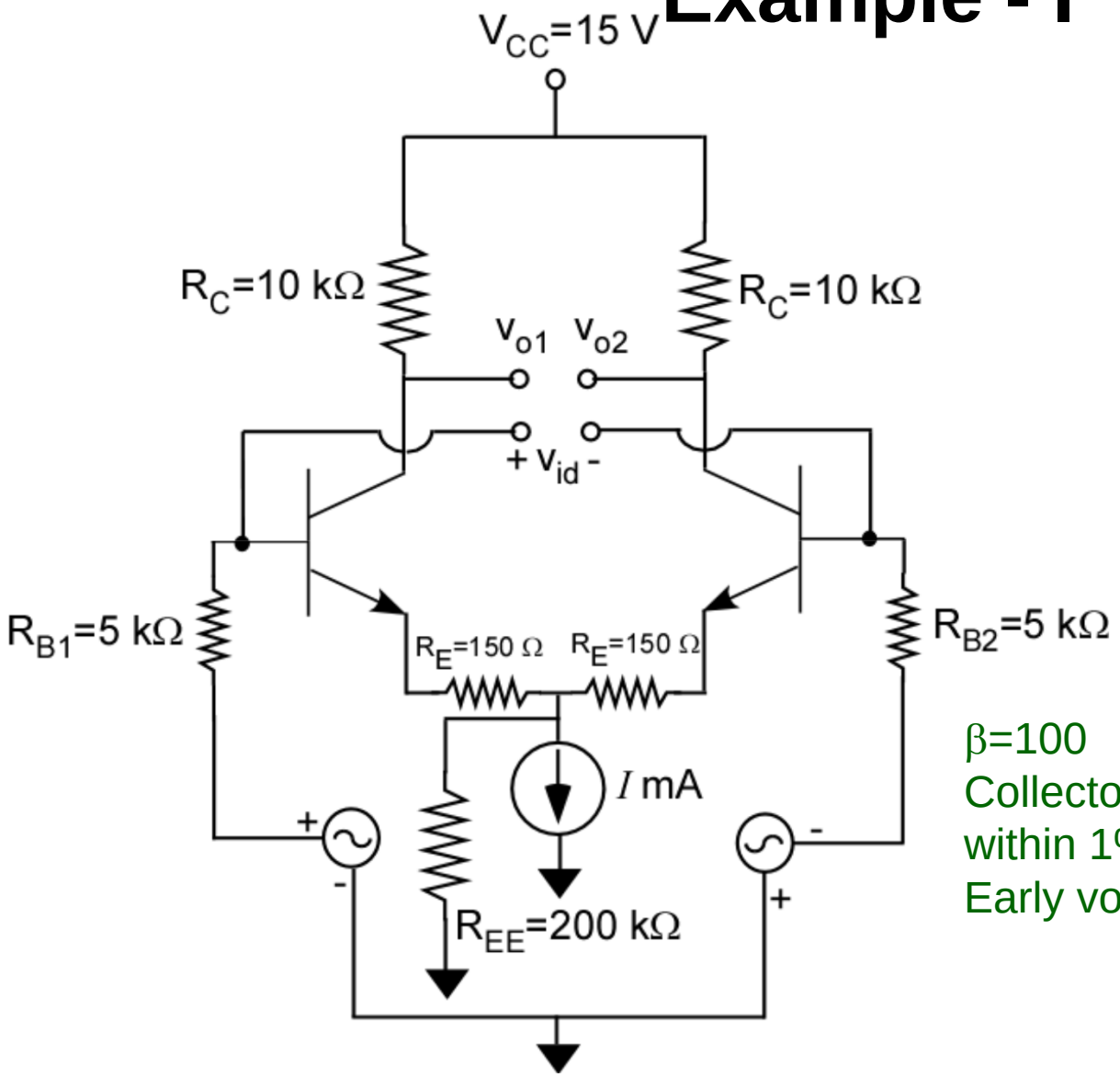
BJT Diff Pair - Common Mode

$$v_o = v_{c1} - v_{c2} = v_{icm} \frac{\alpha \Delta R_C}{2R_{EE} + r_e}$$

$$A_{cm} = \frac{\alpha \Delta R_C}{2R_{EE} + r_e} \simeq \frac{\alpha \Delta R_C}{2R_{EE}}$$

$$A_{cm} = \frac{\alpha R_C}{2R_{EE}} \cdot \frac{\Delta R_C}{R_C}$$

Example - I



β=100
Collector resistance accurate within 1%
Early voltage = 100V

Example – I (cont')

Emitter current in both transistors is: 0.5 mA

$$r_e = \frac{V_T}{I_E} = \frac{25\,mV}{0.5\,mA} = 50\,\Omega$$

$$R_{id} = 2(\beta+1)(r_e + R_E) = 2\times 101\times(50+150) \simeq 40\,k\Omega$$

$$\frac{v_{id}}{v_{sig}} = \frac{R_{id}}{R_{sig}+R_{id}} = \frac{40}{5+5+40} = 0.8$$

$$\frac{v_o}{v_{id}} = \frac{\text{Total resistance in the collectors}}{\text{Total resistance in the emitters}}$$

Example - I (cont')

$$\frac{v_o}{v_{id}} = \frac{2R_C}{2\left(r_e + R_E\right)} = \frac{2\times 10}{2\left(50+150\right)\times 10^{-3}} = 50$$

Overall differential gain:

$$A_d = \frac{v_o}{v_{sig}} = \frac{v_{id}}{v_{sig}} \cdot \frac{v_o}{v_{id}} = 0.8\times 50 = 40$$

$$\underbrace{A_{cm}}_{\text{common-mode gain}} = \frac{R_C}{2R_{EE}} \frac{\Delta R_C}{R_C}$$

Where ΔR_C is the worst case variation in collector resistance

Example – I (cont')

$$A_{cm} = \frac{10}{2 \times 200} \times 0.02 = 5 \times 10^{-4}$$

Common-Mode Rejection ratio CMRR

$$CMRR = 20 \log \frac{|A_d|}{|A_{cm}|}$$

$$CMRR = 20 \log \frac{40}{5 \times 10^{-4}} = 98\ dB$$

Example – I (cont')

Input common-mode resistance: R_{icm}

$$r_o = \frac{V_A}{I/2} = \frac{100}{0.5} = 200\ k\Omega$$

$$R_{icm} = (\beta + 1)\left(R_{EE} \,||\, \frac{r_o}{2} \right) = 101(200\ k\Omega \,||\, 100 k\Omega) = 6.7\ M\Omega$$

Example - II

In the circuit shown, the dc bias current is 4 mA. If α = 0.993, $R_{B1} = R_{B2} = R_{B3}$ = 1,000 Ω, R_E = 30 Ω, R_C = 1.6 kΩ, V_{CC} = 10 V, and $V_{BE(on)}$ = 0.7 V,

(a) Calculate the dc collector currents

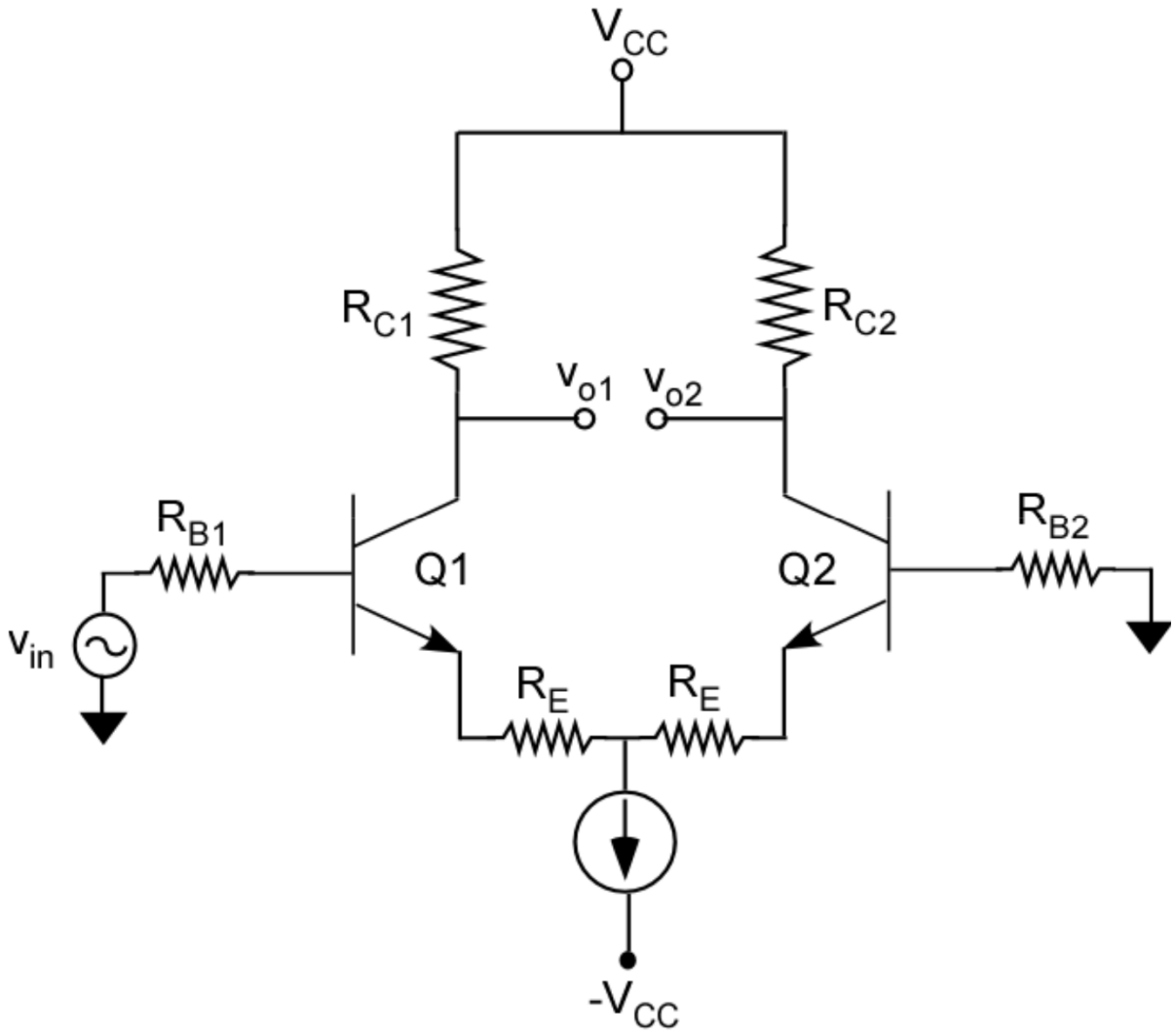
(b) Calculate the dc or quiescent collector voltages

(c) Calculate the maximum peak value of vout before serious distortion results

(d) Calculate the incremental differential voltage gain of the circuit

(e) If the base resistor of Q2 is changed to R_{B2}= 400 Ω, calculate the dc collector current through each device

Example - II



Example - II

(a) Assuming perfect match between Q1 and Q2, DC bias current will split equally $I_{E1} = I_{E2} = 2\text{mA}$. $I_C = \alpha I_E = 1.986$ mA

(b) The quiescent collector voltages will equal

$$V_{CC} - I_C R_C = 10 - 1.986 \times 1.6 = 6.82\,V$$

(c) Maximum collector voltage is 10 V (at cutoff) minimum is 0 V (at saturation).Therefore, positive peak voltage is 10-6.82 = 3.18 V, and negative peak is 6.82 V ➔p-p voltage = 6.36 V

Example - II

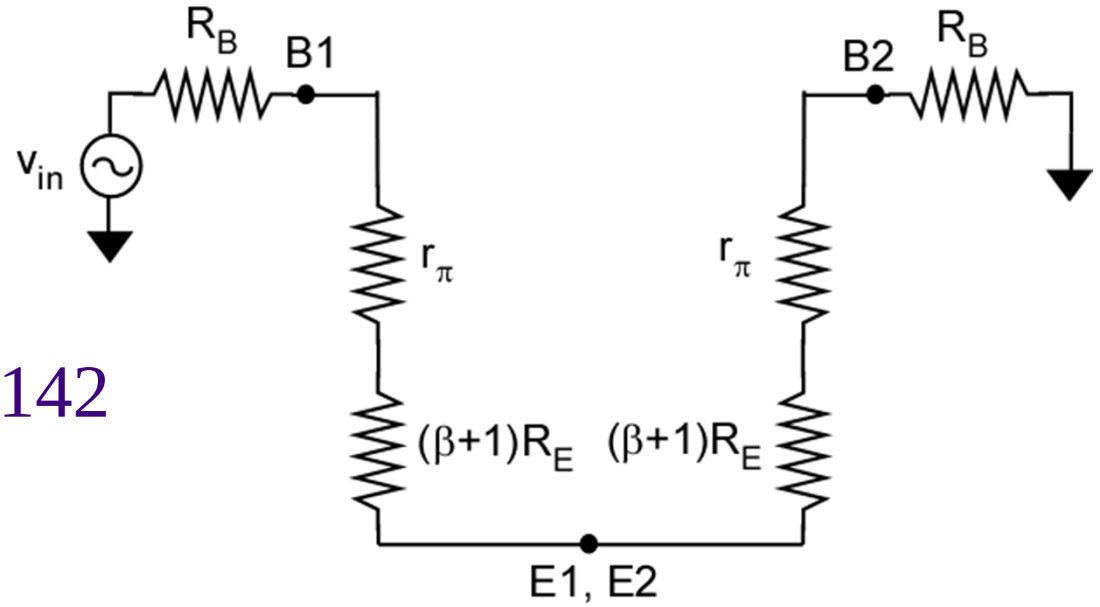
(d) The incremental differential voltage gain of the circuit is defined as:

Calculate r_e and β

$$A_D = \frac{v_{out}}{v_{in}} = \frac{v_{o2} - v_{o1}}{v_{in}}$$

$$r_e = \frac{26}{I_E} = \frac{26}{2} = 13\,\Omega$$

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.993}{0.007} = 142$$



Example - II

Applying the gain equation and assuming r_{out} >> 1.6 kΩ gives

$$A_D = \frac{142 \times 1600}{143 \times (13+30) + 1000} = 31.8\, V/V$$

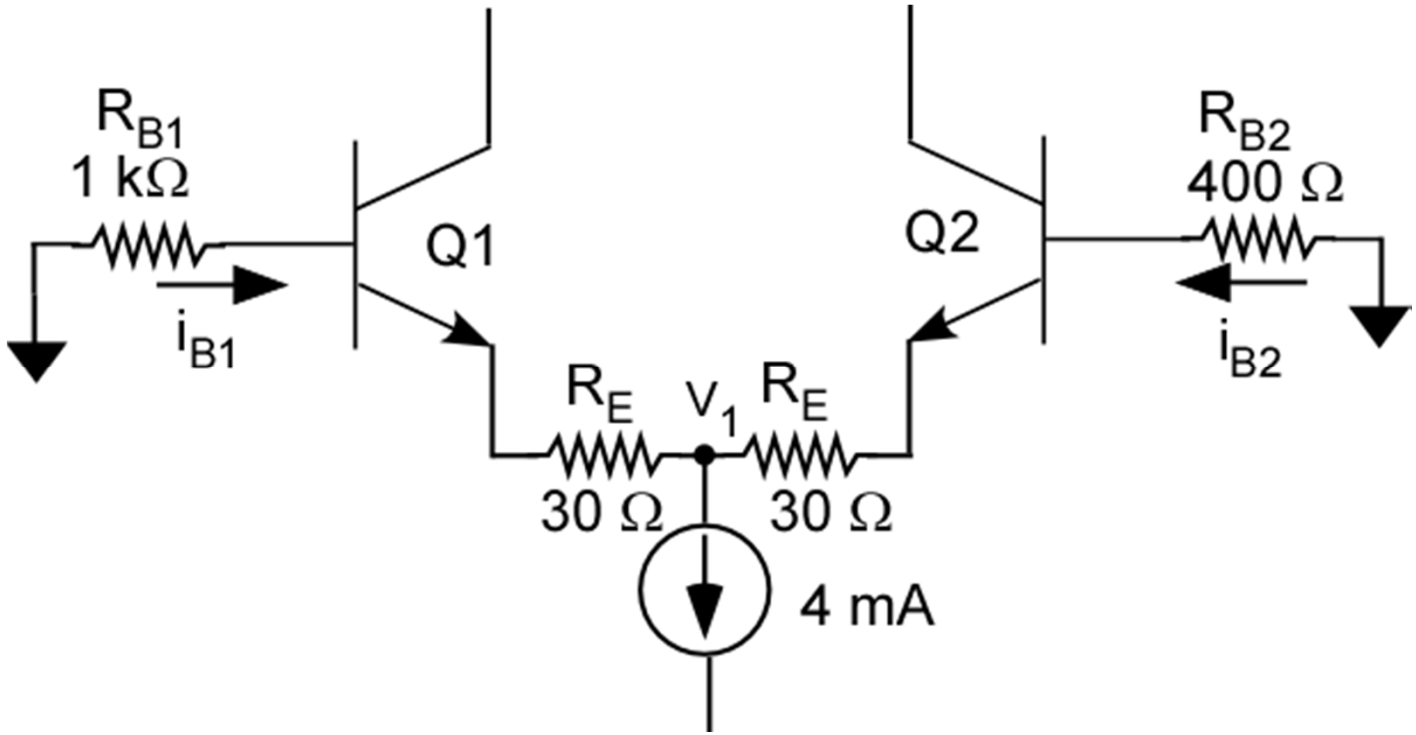
(e) The voltage at the node above the dc current source can be found from

$$V_1 = -\left[I_{B1} R_{B1} + V_{BE(on)} + (\beta + 1) I_{B1} R_E \right]$$

$$V_2 = -\left[I_{B2} R_{B2} + V_{BE(on)} + (\beta + 1) I_{B2} R_E \right]$$

Example - II

Effects of non-balance



Example - II

$$(\beta+1)I_{B1}+(\beta+1)I_{B2}=4\,mA$$

$$I_{B1}=13.1\,\mu A \qquad I_{B2}=14.8\,\mu A$$

The corresponding emitter and collector currents are

$$I_{E1}=1.88\,mA \qquad I_{E2}=2.12\,mA$$

$$I_{C1}=1.86\,mA \qquad I_{C2}=2.10\,mA$$

The two quiescent collector voltages are no longer equal, resulting in a nonzero quiescent output voltage

$$V_{CQ2}=10-1.6\times 2.1=6.64\,V$$

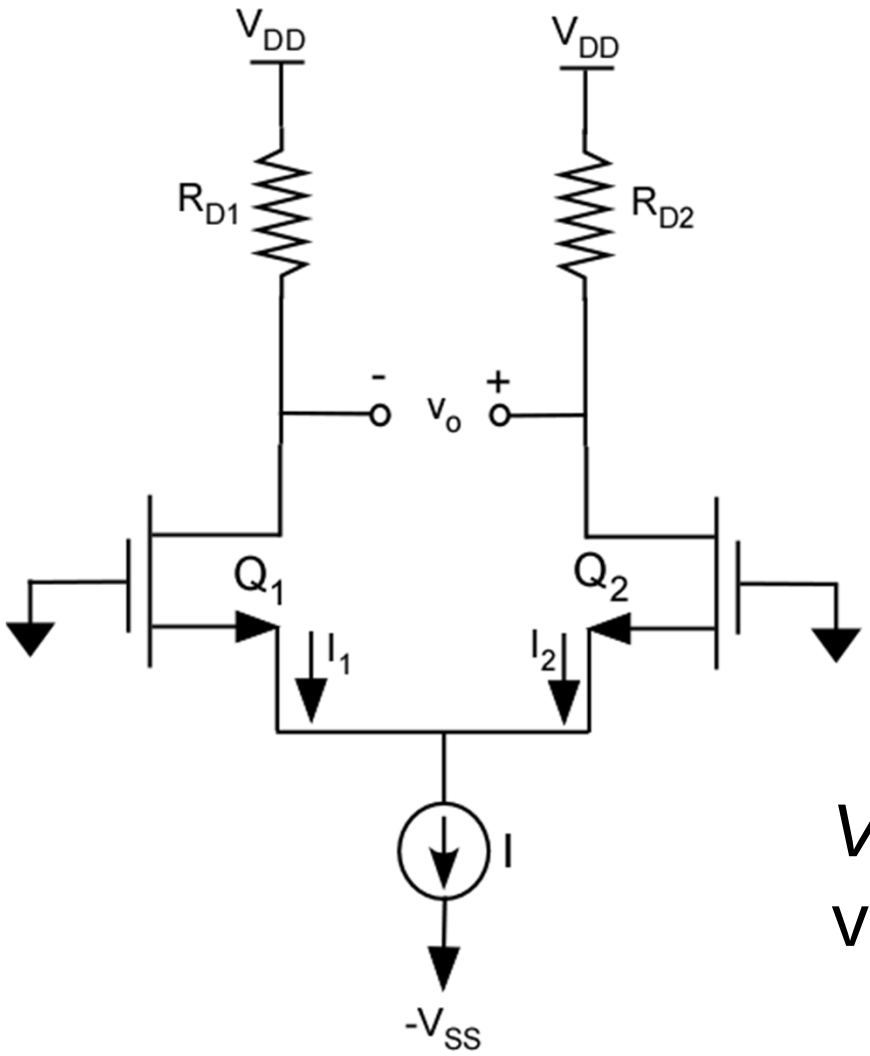
$$V_{CQ1}=10-1.6\times 1.86=7.02\,V$$

Example - II

$$V_{outQ} = V_{CQ2} - V_{CQ1} = 6.64 - 7.02 = -0.38\,V$$

Nonzero quiescent voltage ➔serious consequences when this stage is followed by additional gain stages, creating an output offset voltage when the inputs are shorted together

Nonideal Characteristics



Input offset voltage of MOS differential pair

Mismatch can result in a dc output voltage V_o (output dc offset voltage)

$V_{os}=V_o/A_d$ is input offset voltage

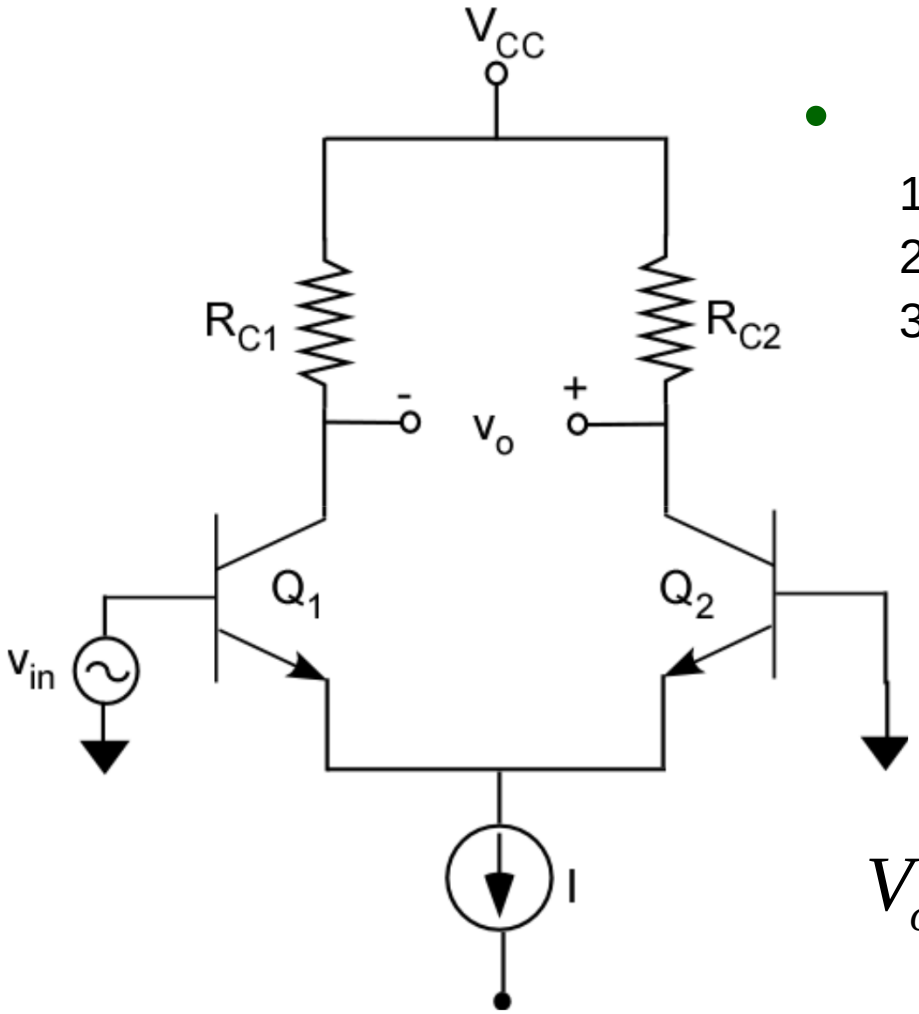
Nonideal Characteristics

If V_{os} is applied (differentially) at the input, a zero voltage difference should result at the output

- **Factors contributing to dc offset voltage**
  1. Mismatch in load resistance
  2. Mismatch in *W/L*
  3. Mismatch in V_T

$$V_{os} = \sqrt{\left(\frac{V_{ov}}{2} \cdot \frac{\Delta R_D}{2}\right)^2 + \left(\frac{V_{ov}}{2} \cdot \frac{\Delta(W/L)}{W/L}\right)^2 + (\Delta V_T)^2}$$

Input Offset Voltage for BJT Diff Pair



- **Offset results from**
  1. Mismatch in RC's
  2. Mismatch in β
  3. Mismatch in junction area

$$V_{os} = V_T \sqrt{\left(\frac{\Delta R_C}{R_C}\right)^2 + \left(\frac{\Delta I_S}{I_S}\right)^2}$$

Offset Current for BJT Diff Amp

In a perfectly symmetric differential pair, the 2 input terminals carry equal dc current to support bias

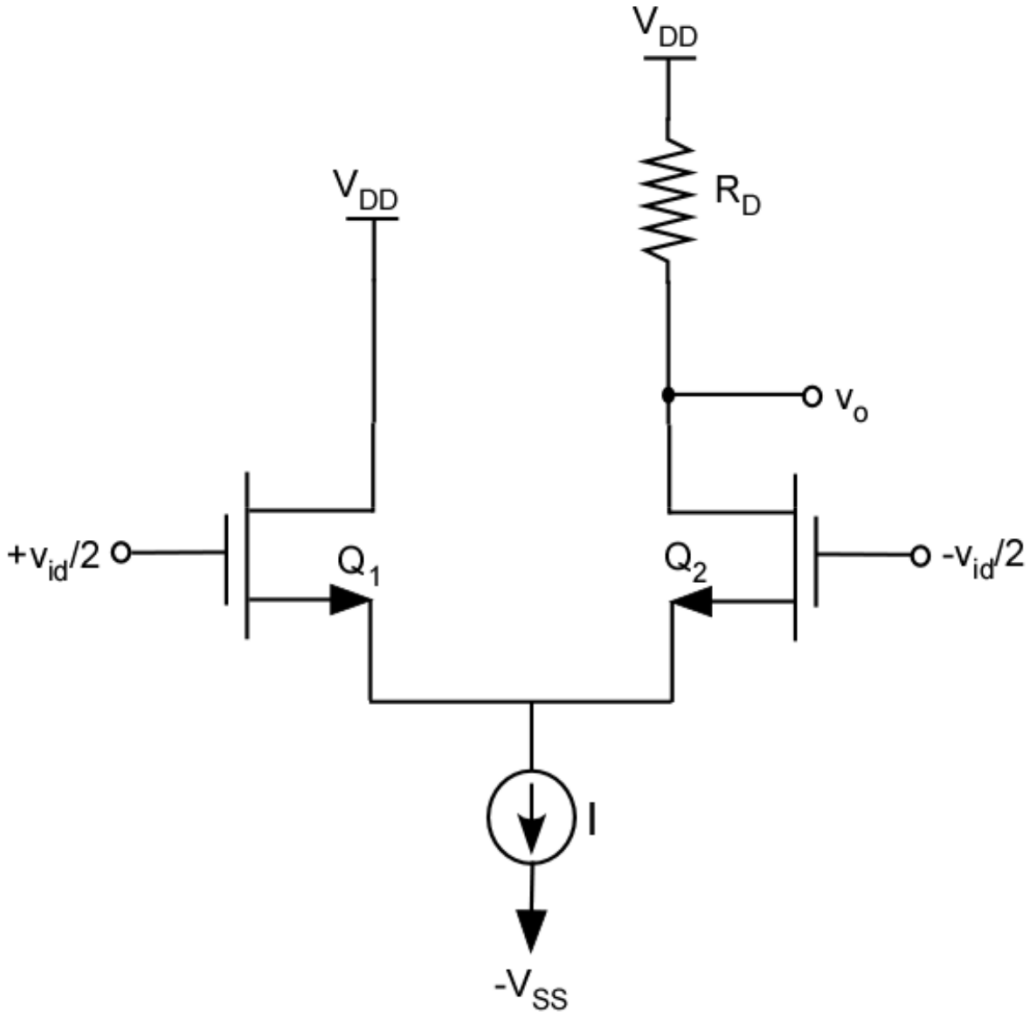
$$I_{B1} = I_{B2} = \frac{I/2}{\beta + 1}$$

Mismatches (primarily from β) make the 2 input dc currents unequal

$$I_{os} = \left| I_{B1} - I_{B2} \right|$$

$$I_{os} = I_B \left(\frac{\Delta\beta}{\beta} \right)$$

Differential-to-Single-Ended Conversion

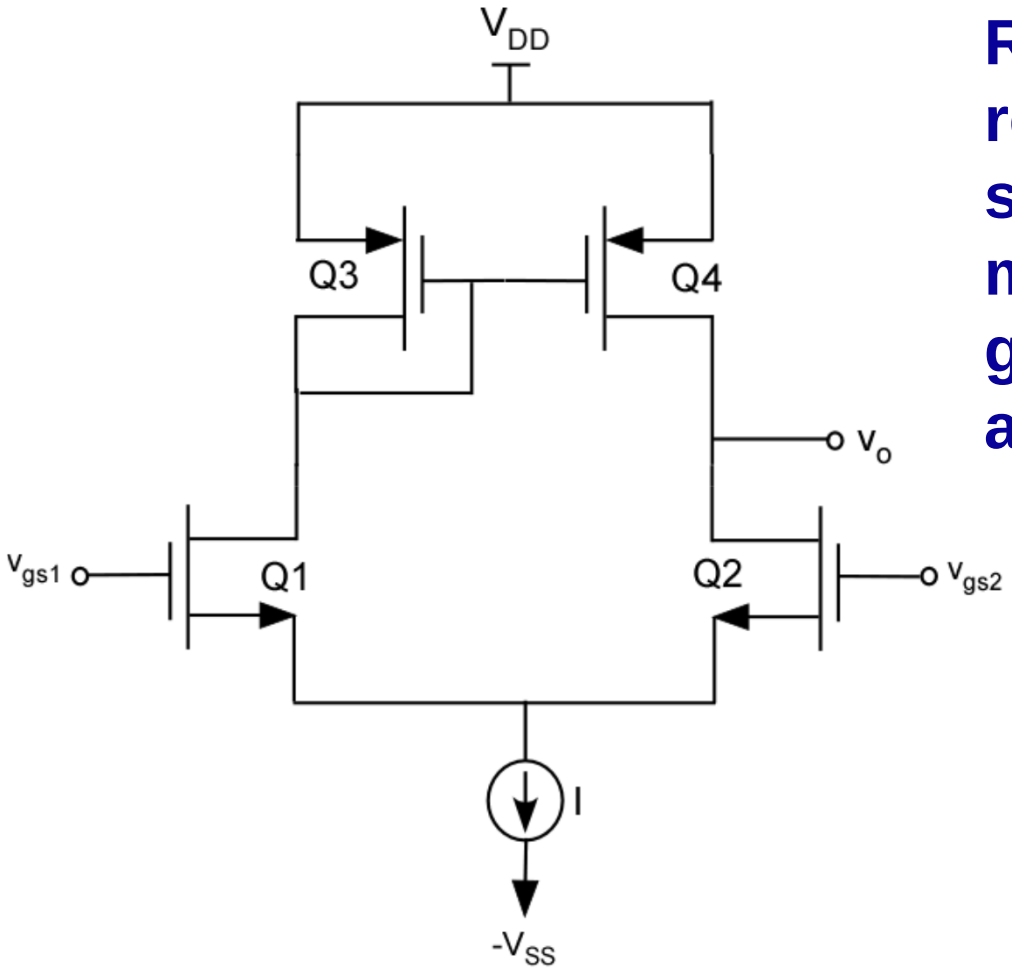


- Beyond first stage, signal can be converted from differential to single-ended
- Simply ignore the drain current in Q_1 and eliminate its drain resistor

Differential-to-Single-Ended Conversion

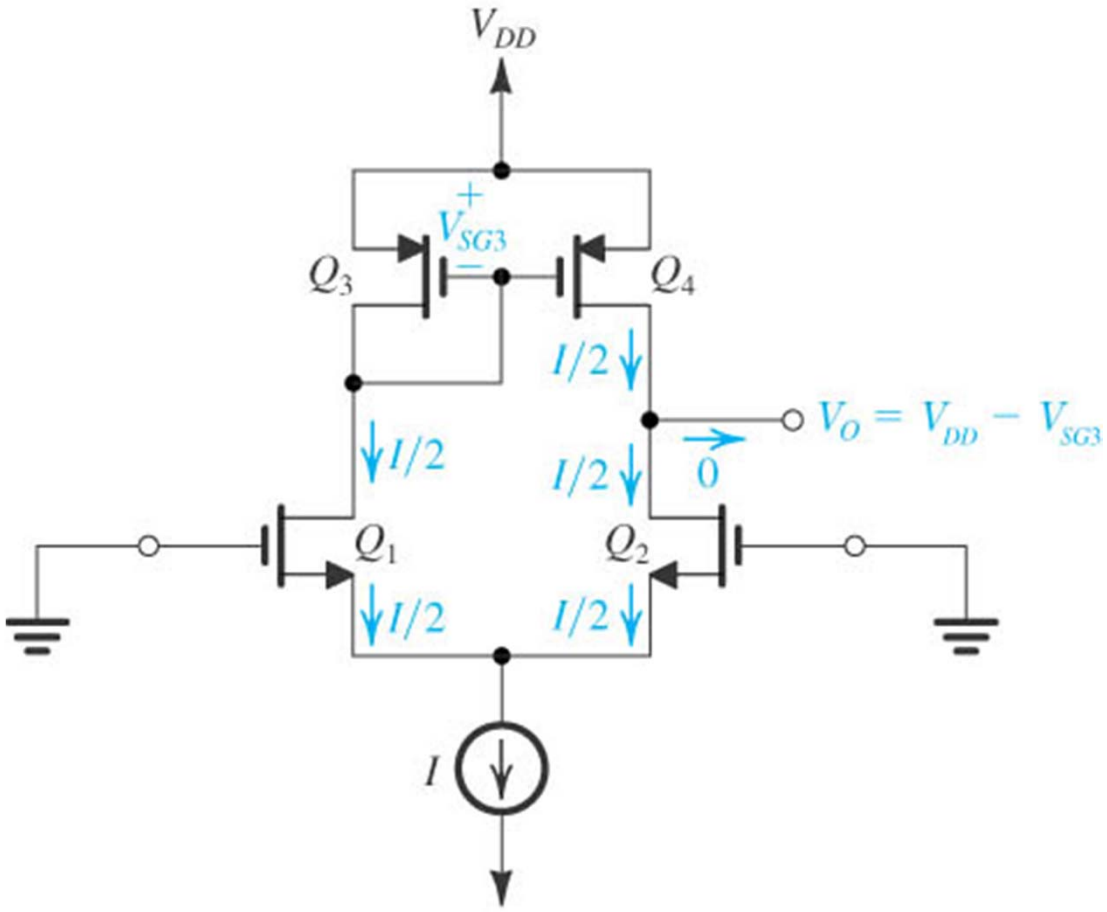
- **Limitations**
  - Factor of 2 (6 dB) is lost in the gain if drain current of Q_1 is not used
  - Much better approach consists of using drain current of Q_1
  - Active load approach allows to perform conversion without loss of gain by making use of drain current in Q_1

MOS Differential Amp with Active Load



Replacing drain resistances with current sources, results in much higher voltage gain and savings in chip area in diff amp

MOS Differential Amp - Equilibrium



MOS Differential Amp with Active Load

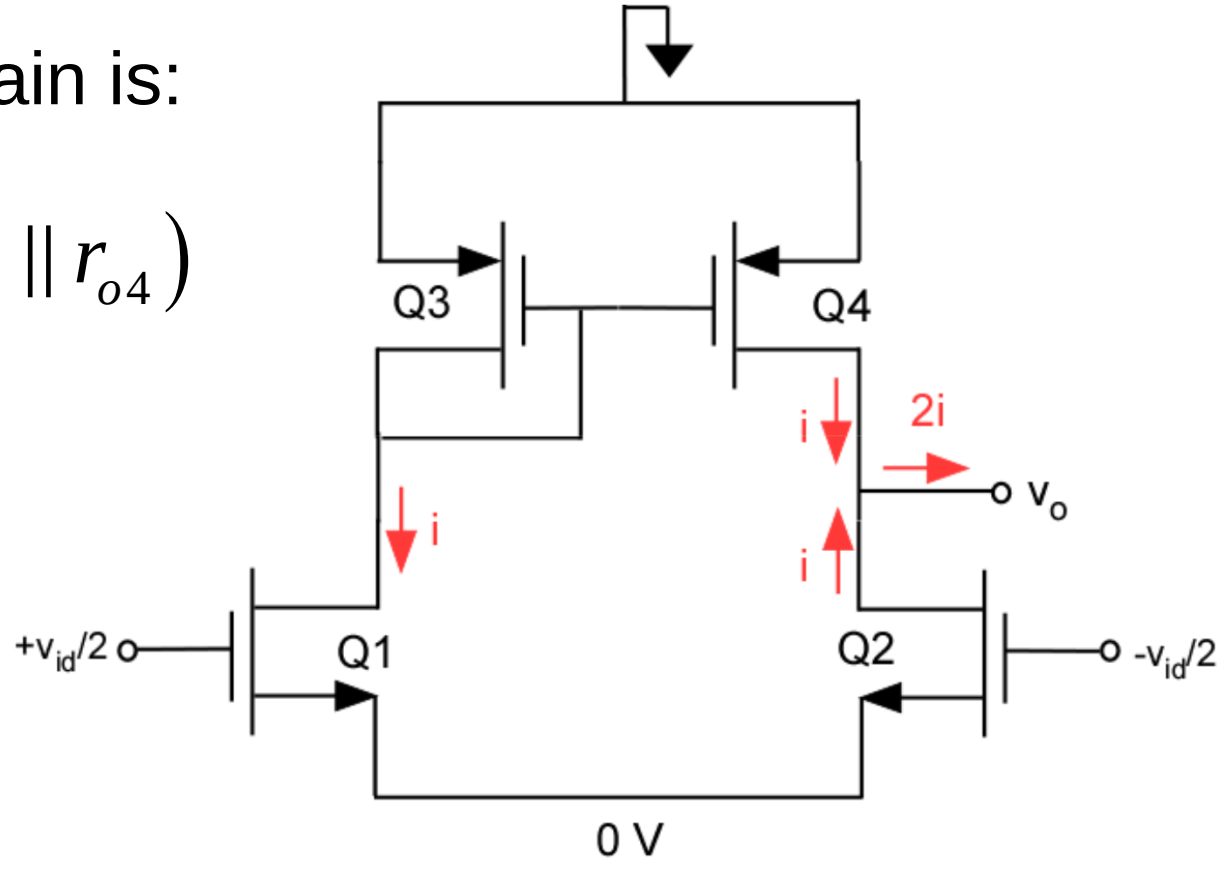
Current mirror action makes it possible to convert the signal to single-ended form without loss of gain.

The differential gain is:

$$A_d \equiv \frac{v_o}{v_{id}} = g_m \left(r_{o2} \,\|\, r_{o4} \right)$$

$$If \;\; r_{o2} = r_{o4} = r_o$$

$$A_d = \frac{1}{2} g_m r_o$$



MOS Differential Amp with Active Load

The active-loaded MOS differential amplifier has a low common-mode gain ➔ high CMRR

The common-mode gain is:

$$A_{cm} \equiv \frac{v_o}{v_{icm}} = -\frac{1}{2R_{SS}} \frac{r_{o4}}{1+g_{m3}r_{o3}}$$

R_{SS} is internal impedance of current source

$$Usually,\ g_{m3}r_{o3} \gg 1 \ and \ r_{o3} = r_{o4}$$

$$A_{cm} = -\frac{1}{2g_{m3}R_{SS}}$$

MOS Differential Amp with Active Load

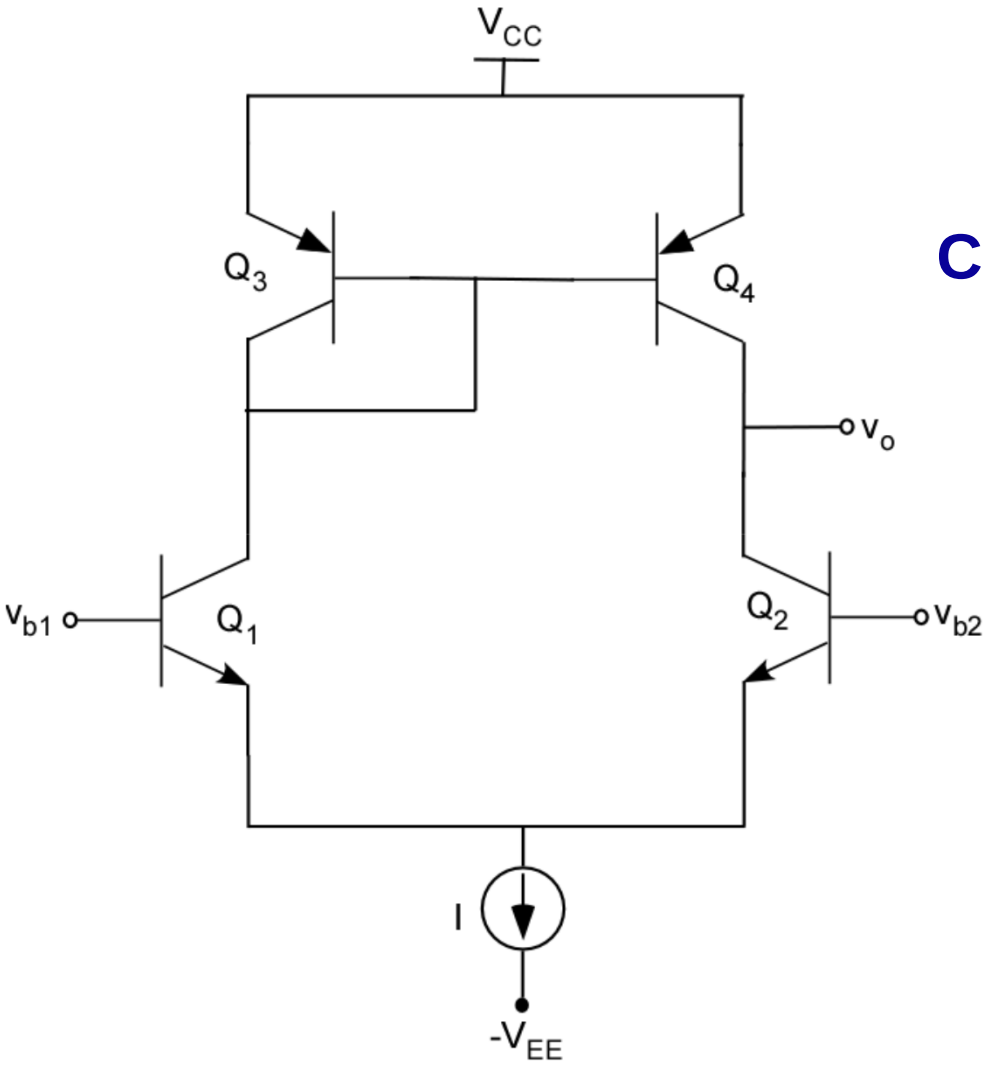
Since R_{SS} is large, A_{cm} will be small

$$CMRR \equiv \frac{|A_d|}{|A_{cm}|} = \left[g_m \left(r_{o2} \,||\, r_{o4} \right) \right] \left[2 g_{m3} R_{SS} \right]$$

$$If \quad r_{o2} = r_{o4} = r_o \quad and \quad g_{m3} = g_m$$

$$CMRR = \left(g_m r_o \right) \left(g_m R_{SS} \right)$$

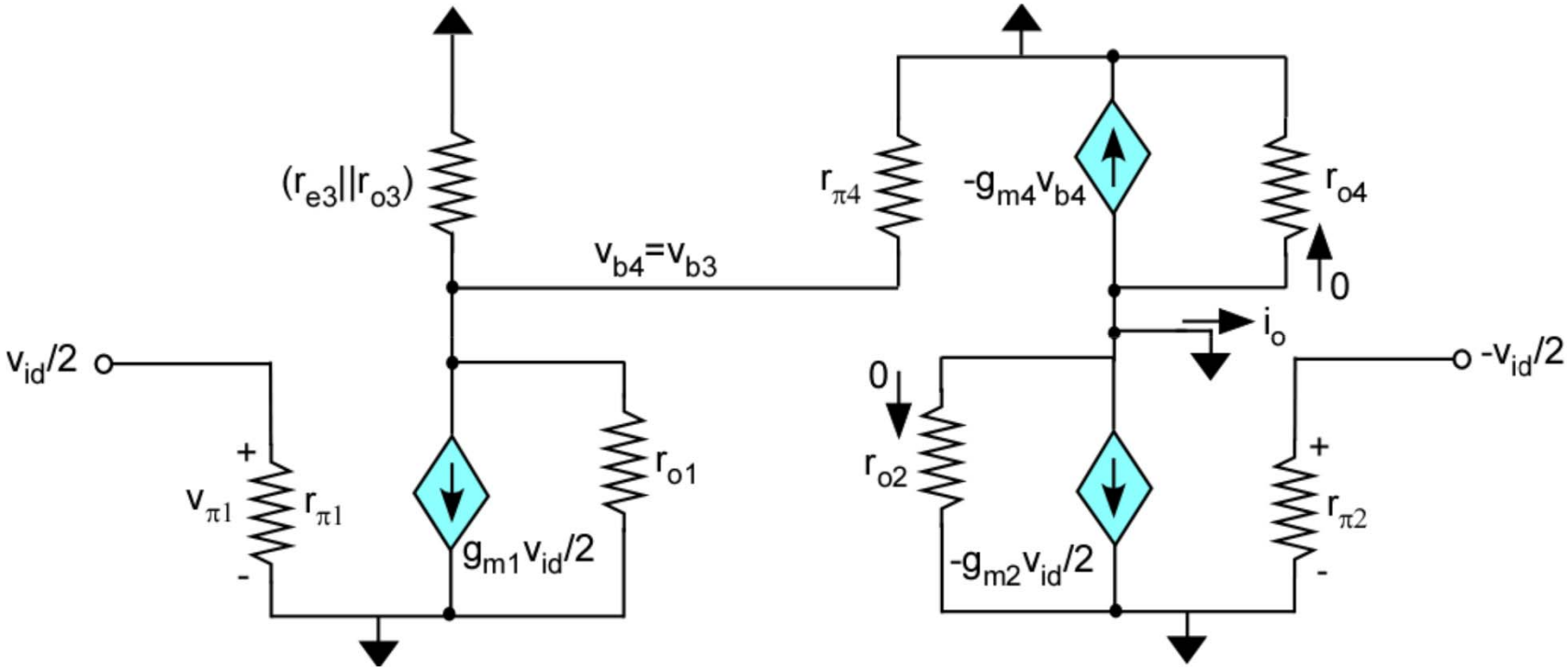
BJT Differential Amp with Active Load



Current mirror & active load

Differential stage

Active Loaded BJT Pair – Incremental Model



Virtual ground develops at common-emitter terminal

BJT Differential Amp with Active Load

Output resistance is parallel equivalent of the output resistance of the differential pair and the output resistance of the current mirror

The differential gain is:

$$A_d \equiv \frac{v_o}{v_{id}} = g_m \left(r_{o2} \,\|\, r_{o4} \right)$$

$$If \;\; r_{o2} = r_{o4} = r_o$$

$$A_d = \frac{1}{2} g_m r_o$$

The differential input impedance is:

$$R_{id} = 2r_\pi$$

BJT Differential Amp with Active Load

The active-loaded BJT differential amplifier has a low common-mode gain ➔ high CMRR

The common-mode gain is:

$$A_{cm} \equiv \frac{v_o}{v_{icm}} \simeq -\frac{r_{o4}}{\beta_3 R_{EE}}$$

R_{EE} is internal impedance of current source

$$It\ is\ assumed\ that,\ \ g_{m3} = g_{m4}$$

$$and\ r_{\pi 4} = r_{\pi 3}\ \ and\ r_{o3} \gg r_{\pi 3}, r_{\pi 4}$$

BJT Differential Amp with Active Load

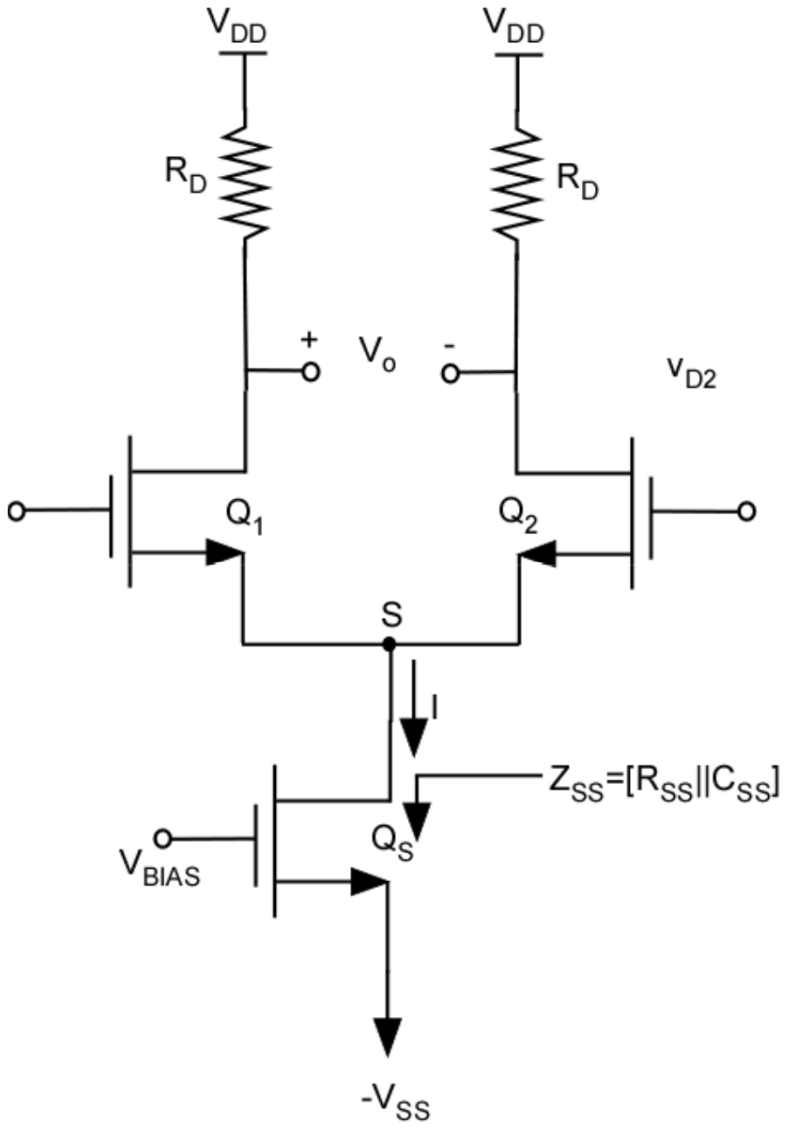
$$CMRR \equiv \frac{|A_d|}{|A_{cm}|} = \left[g_m \left(r_{o2} \,||\, r_{o4} \right) \right] \left(\frac{\beta_3 R_{EE}}{r_{o4}} \right)$$

$$If \quad r_{o2} = r_{o4} = r_o$$

$$CMRR = \frac{1}{2} \beta_3 g_m R_{EE}$$

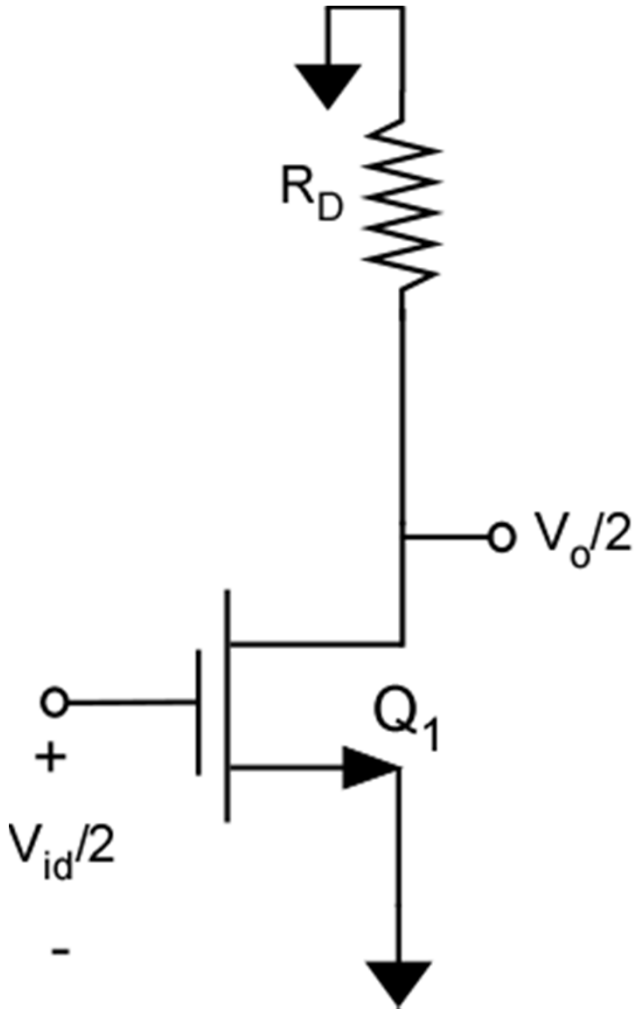
For large *CMRR*, bias current source should have large output resistance R_{EE}

Frequency Response of MOS Diff Amp



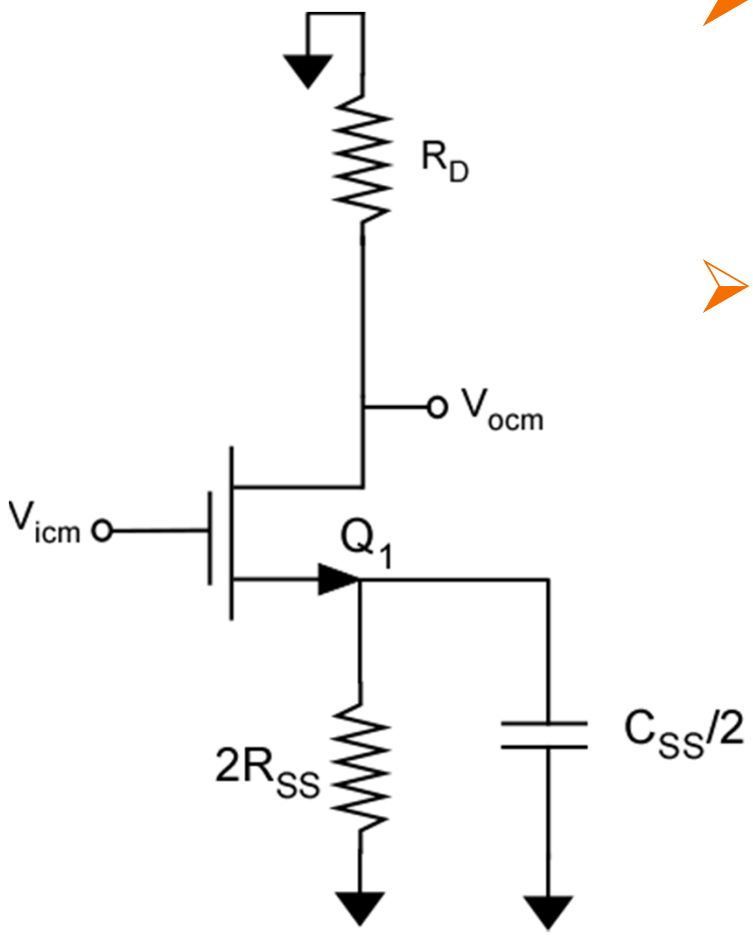
- **Resistively Loaded**
  1. Resistance R_{SS} is between node S and ground
  2. Capacitance C_{SS} is between node S and ground
  3. C_{SS} includes C_{db}, C_{gd}, and C_{sb}

Frequency Response – Differential Half



Gain function of differential half will be identical to that of common-source amplifier

Frequency Response – Common-Mode



- $C_{SS}/2$ will form dominant real-axis zero at much lower frequency
- Zero dominates frequency dependence of A_{cm}

Common-mode gain is found by analyzing the effect of a mismatch ΔR_D in R_D

Frequency Response – Common-Mode

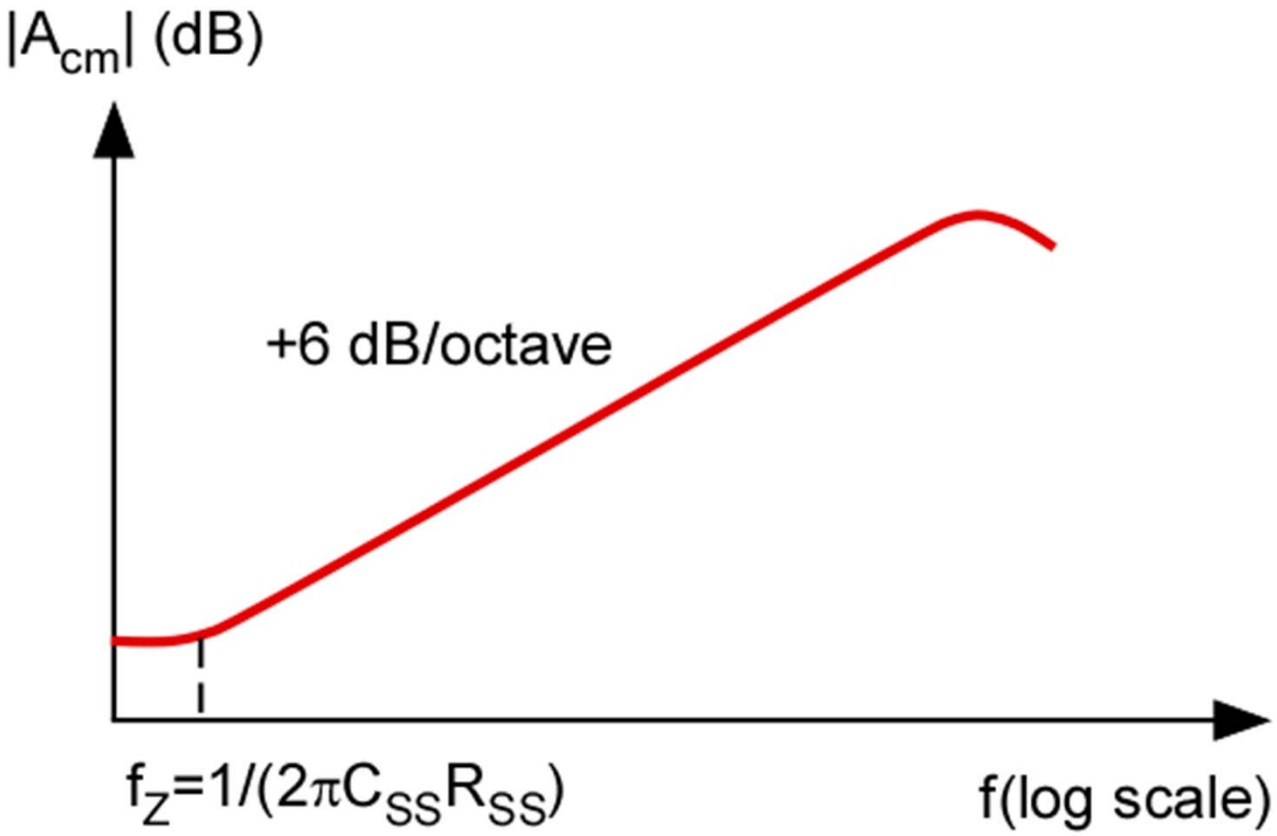
$$A_{cm}(s) = -\frac{R_D}{2R_{SS}}\left(\frac{\Delta R_D}{R_D}\right)\left(1 + sC_{SS}R_{SS}\right)$$

A_{cm} picks up a zero on the negative real axis of the complex s-plane. The frequency is ω_Z

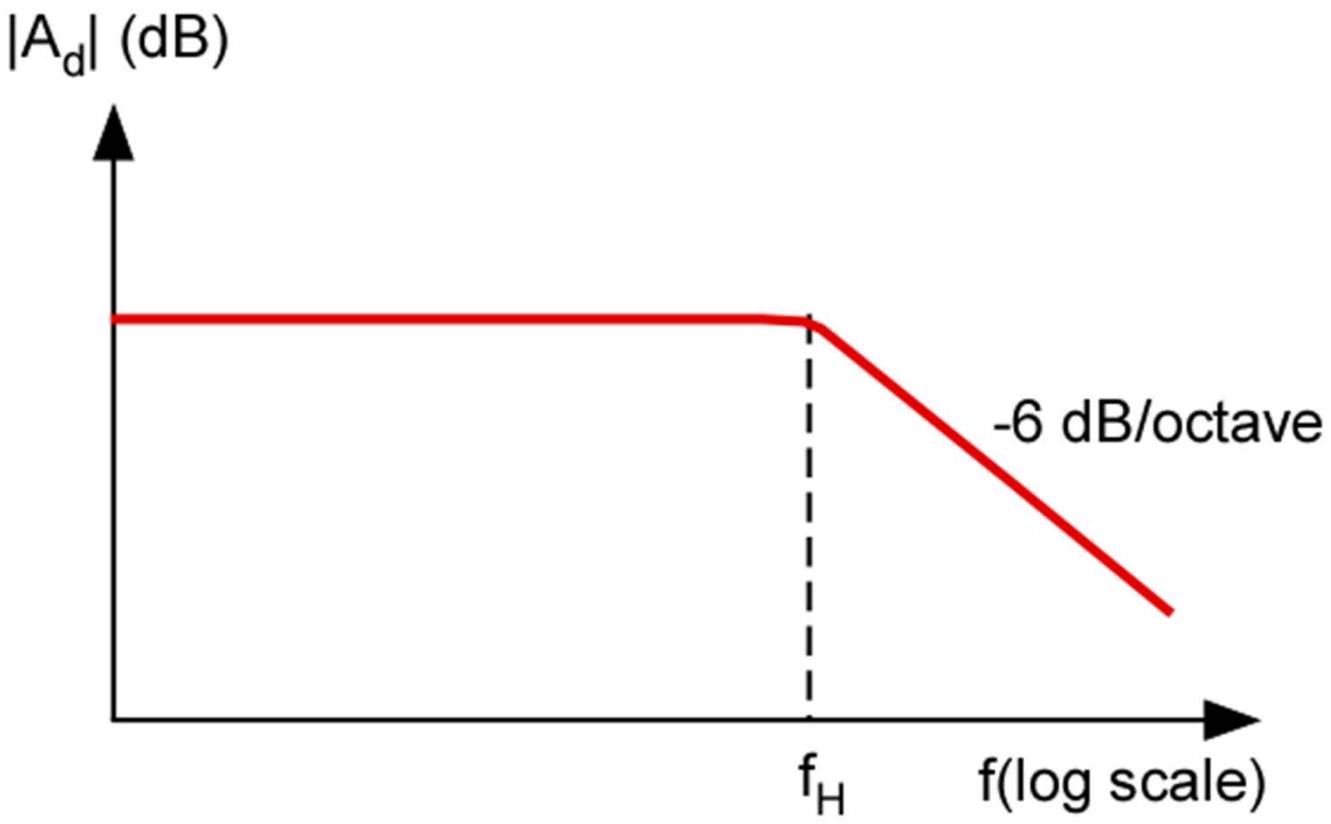
$$\omega_Z = \frac{1}{C_{SS}R_{SS}}$$

$$f_Z = \frac{1}{2\pi C_{SS}R_{SS}}$$

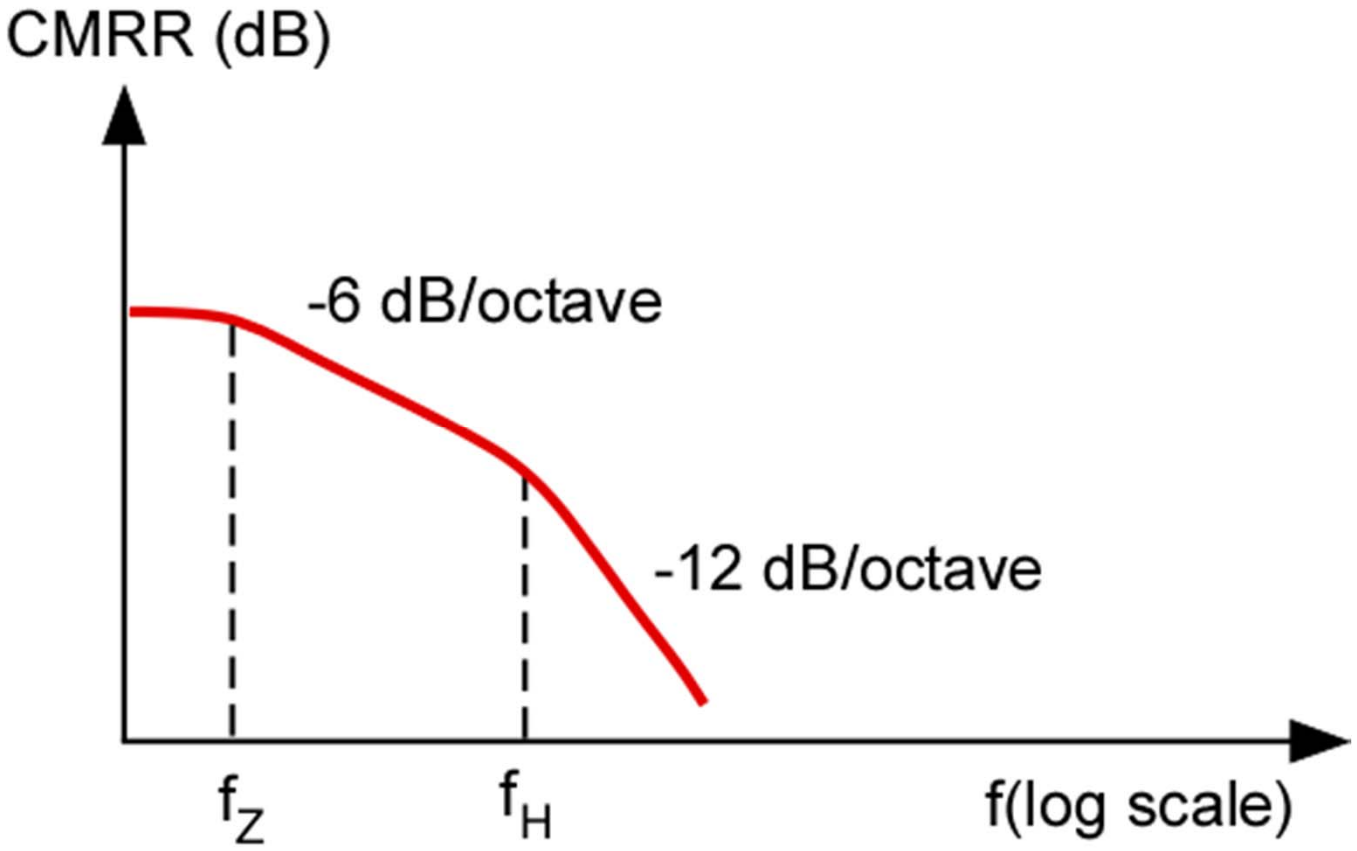
Frequency Response – Common-Mode Gain



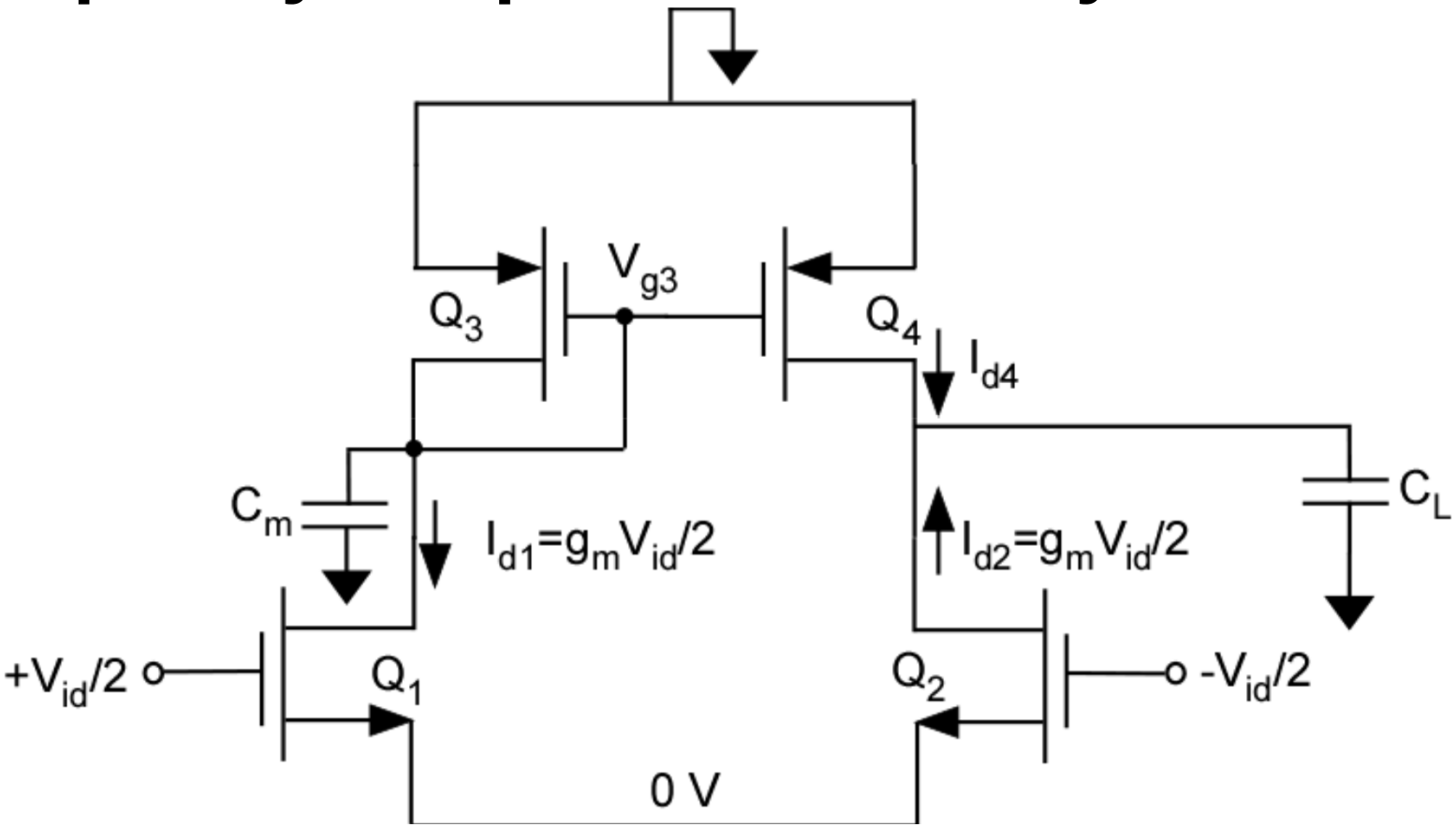
Frequency Response – Differential Gain



Frequency Response – CMRR



Frequency Response – Actively Loaded MOS



$$C_m = C_{gd1} + C_{db1} + C_{db3} + C_{gs3} + C_{gs4}$$ ➔Capacitance at input node

$$C_L = C_{gd2} + C_{db2} + C_{gd4} + C_{db4} + C_{load}$$ ➔Capacitance at output node

Frequency Response – Actively Loaded MOS

$$A_d(s) \equiv \frac{v_o}{v_{id}} = (g_m R_o)\left(\frac{1}{1+sC_L R_o}\right)\left(\frac{1+s\dfrac{C_m}{2g_{m3}}}{1+s\dfrac{C_m}{g_{m3}}}\right)$$

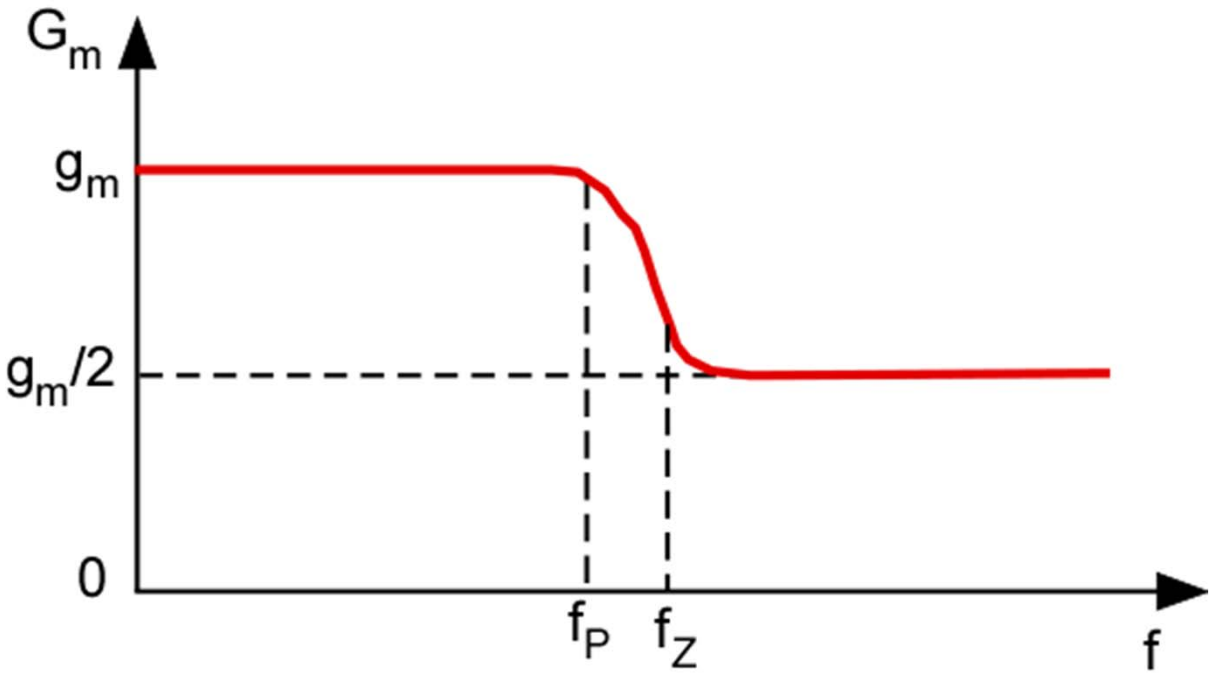
First pole: $f_{P1} = \dfrac{1}{2\pi C_L R_o}$

Second pole: $f_{P2} = \dfrac{g_{m3}}{2\pi C_m} \simeq \dfrac{g_{m3}}{2\pi(2C_{gs3})} \simeq f_T/2$

Zero at: $f_Z = \dfrac{2g_{m3}}{2\pi C_m} \simeq f_T$

Mirror pole and zero occur at very high frequencies

Actively Loaded MOS - Transconductance

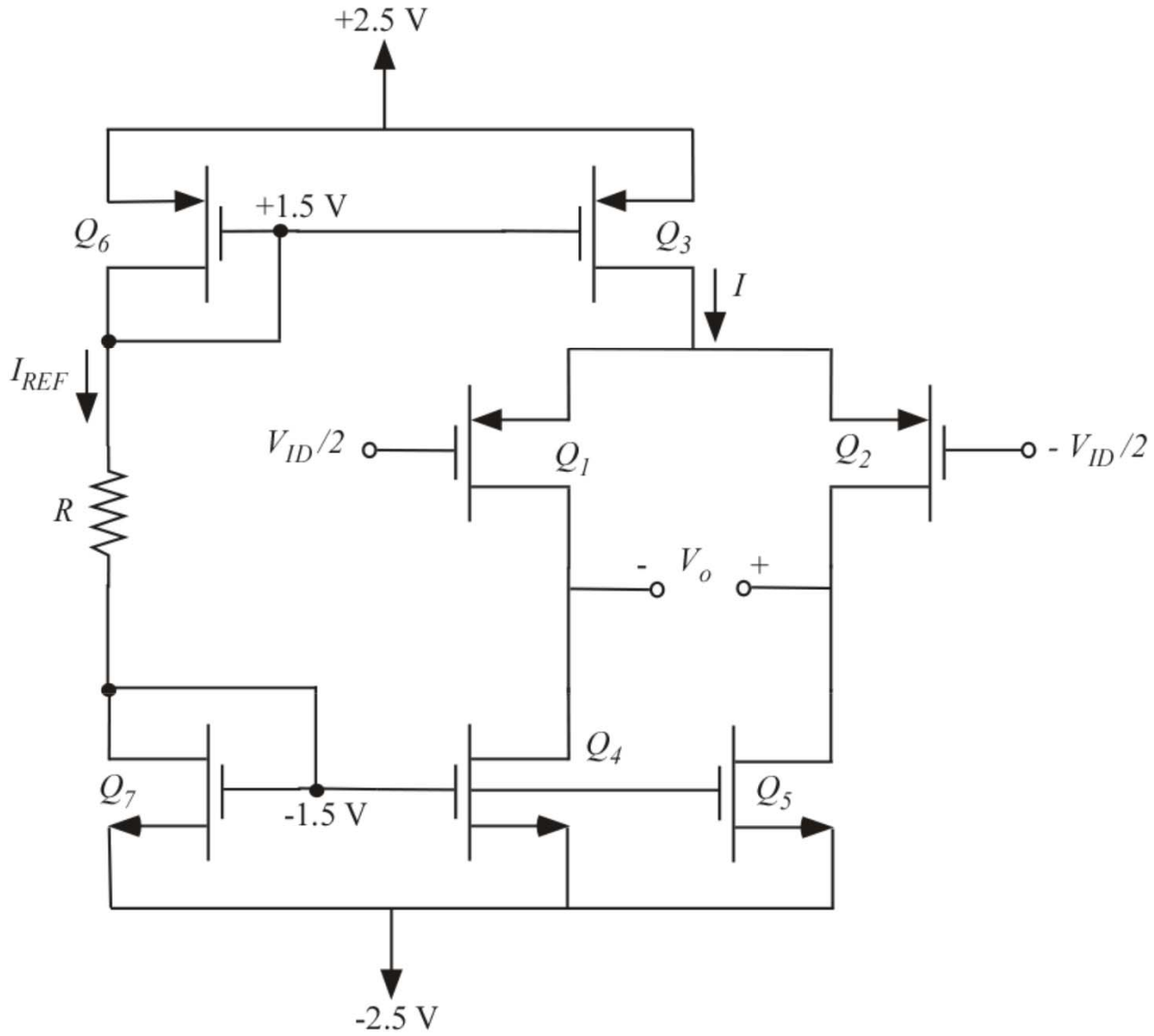


CMOS OP Amp Example

In the differential amplifier shown, Q_1 and Q_2 form the differential pair while the current source transistors Q_4 and Q_5 form the active loads for Q_1 and Q_2 respectively. The dc bias circuit that establishes an appropriate dc voltage at the drains of Q_1 and Q_2 is not shown. The following specifications are desired: differential gain A_d = 80V/V, I_{REF} = 100 μA, the dc voltage at the gates of Q_6 and Q_3 is +1.5V; the dc voltage at the gates of Q_7, Q_4 and Q_5 is –1.5V.

The technology available is specified as follows: $\mu_n C_{ox} = 3\mu_p C_{ox}$ = 90μA/V^2; $V_{tn} = |V_{tp}| = 0.7$V, $V_{An} = |V_{Ap}|$ = 20V. Specify the required value of R and the W/L ratios for all transistors. Also, specify I_D and V_{GS} at which each transistor is operating. For dc bias calculations, you may neglect channel-length modulation. Fill in the entries in the table provided to show your results.

CMOS OP Amp Example



CMOS OP Amp Example

$$I_{REF} = 100\mu A = \frac{1.5-(-1.5)}{R} \Rightarrow R = \frac{3V}{0.1mA} = 30k\Omega$$

Drain currents are determined by symmetry and inspection V_{GS} values are also determined by inspection for all transistors except Q_1 and Q_2. To determine V_{GS} for Q_1 and Q_2, we do the following: the equivalent load resistance will consist of r_{o1} in parallel with r_{o4} for Q_1 and r_{o2} in parallel with r_{o5} for Q_5. Since the r_o's are equal, this corresponds to $r_o/2$. We have:

$$g_m \frac{r_o}{2} = A_d \Rightarrow g_m = \frac{2A_d}{r_o} = \frac{2\times 80}{400k\Omega} = 0.4mA/V$$

CMOS OP Amp Example

$$g_m = \frac{2I_D}{V_{ov}} \Rightarrow V_{ov} = \frac{2I_D}{g_m} = \frac{2 \times 0.05}{0.4} = 0.25$$

Take polarity into account for PMOS

$$V_{GS1,2} = -0.25 - V_T = -0.95$$

To find W/L ratios, use

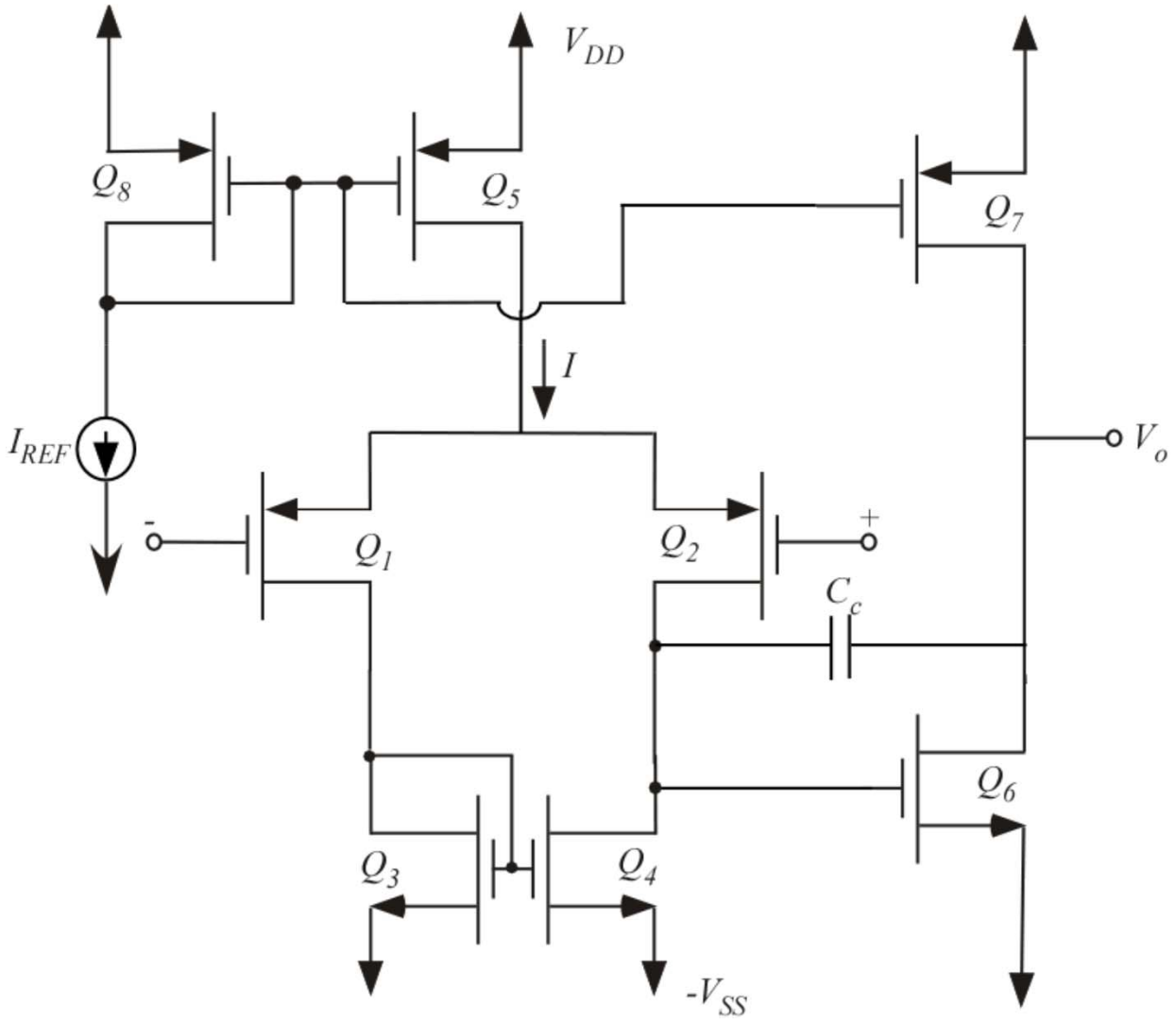
$$I_D = \mu C_{ox} \frac{W}{2L}(V_{GS} - V_T)^2 \Rightarrow \frac{W}{L} = \frac{2I_D}{\mu C_{ox}(V_{GS} - V_T)^2}$$

taking into account PMOS and NMOS devices separately

CMOS OP-AMP DESIGN TABLE

	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Units
μC_{ox}	30	30	30	90	90	30	90	$\mu A/V^2$
I_D	50	50	100	50	50	100	100	μA
V_{GS}	-.95	-.95	-1	+1	+1	-1	+1	V
W/L	57.3	57.3	74 1.	12.3	12.3	73.1	24.7	

2-Stage CMOS Op Amp



2-Stage CMOS Op Amp

Two-stage configuration with two power supplies which can range from +/- 2.5 V for 0.5 μm technology to +/- 0.9 V for 0.18 μm technology. I_{REF} is generated either externally or using on-chip CKT.

Current mirror formed by Q_5-Q_8 supplies differential pair Q_1-Q_2 with bias current. The W/L of Q_5 is selected to control I. The diff pair is actively loaded by current mirror Q_3-Q_4

2-Stage CMOS Op Amp

Second stage is Q6 which is a CS amplifier for which Q7 is the current source. A capacitor Cc is included for negative feedback to enhance the Miller effect through Q6 ➔ compensation. This op amp does not have a low output impedance and is thus not suited for driving a low-impedance load. The *W/L* ratios are given and listed below:

	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
W/L	20/0.8	20/0.8	5/0.8	5/0.8	40/0.8	10/0.8	40/0.8	40/0.8

$$Let\ I_{REF} = 90\ \mu A,\quad V_{tn} = 0.7\,V,\ V_{tp} = -0.8\,V$$

$$\mu_n C_{ox} = 160\ \mu A/V^2,\ \ \mu_p C_{ox} = 40\ \mu A/V^2$$

2-Stage CMOS Op Amp

$$|V_A| \; for \; all \; devices = 10\,V, \quad V_{DD} = V_{SS} = 2.5\,V$$

- **Voltage Gain**

First stage: $A_1 = -g_{m1}\left(r_{o2} \,||\, r_{o4}\right)$

Since Q_8 and Q_5 are matched, $I = I_{REF}$, Q_1, Q_2, Q_3 and Q_4 will have $I/2$ = 45 μA.

$I_{Q7} = I_{REF}$ = 90 μA = I_{Q6}

Let V_{GS} - V_T = V_{ov} (overdrive voltage)

2-Stage CMOS Op Amp

$$From\ I_D = \frac{1}{2}\left(\mu C_{ox}\right)\left(W/L\right)V_{ov}^2$$

We find V_{ov} for each transistor.

Transconductance is: $g_m = \dfrac{2I_D}{|V_{ov}|}$

$$r_o = \frac{|V_A|}{I_D}$$

2-Stage CMOS Op Amp – Voltage Gain

Gain for first stage: $A_1 = -g_{m1}\left(r_{o2} \,||\, r_{o4}\right)$

$$A_1 = -0.3\left(222 \,||\, 222\right) = -33.3\,V/V$$

Gain for second stage: $A_2 = -g_{m6}\left(r_{o6} \,||\, r_{o7}\right)$

$$A_2 = -0.6\left(111 \,||\, 111\right) = -33.3\,V/V$$

Overall dc open loop gain is (-33.3)(-33.3) = 1109 V/V

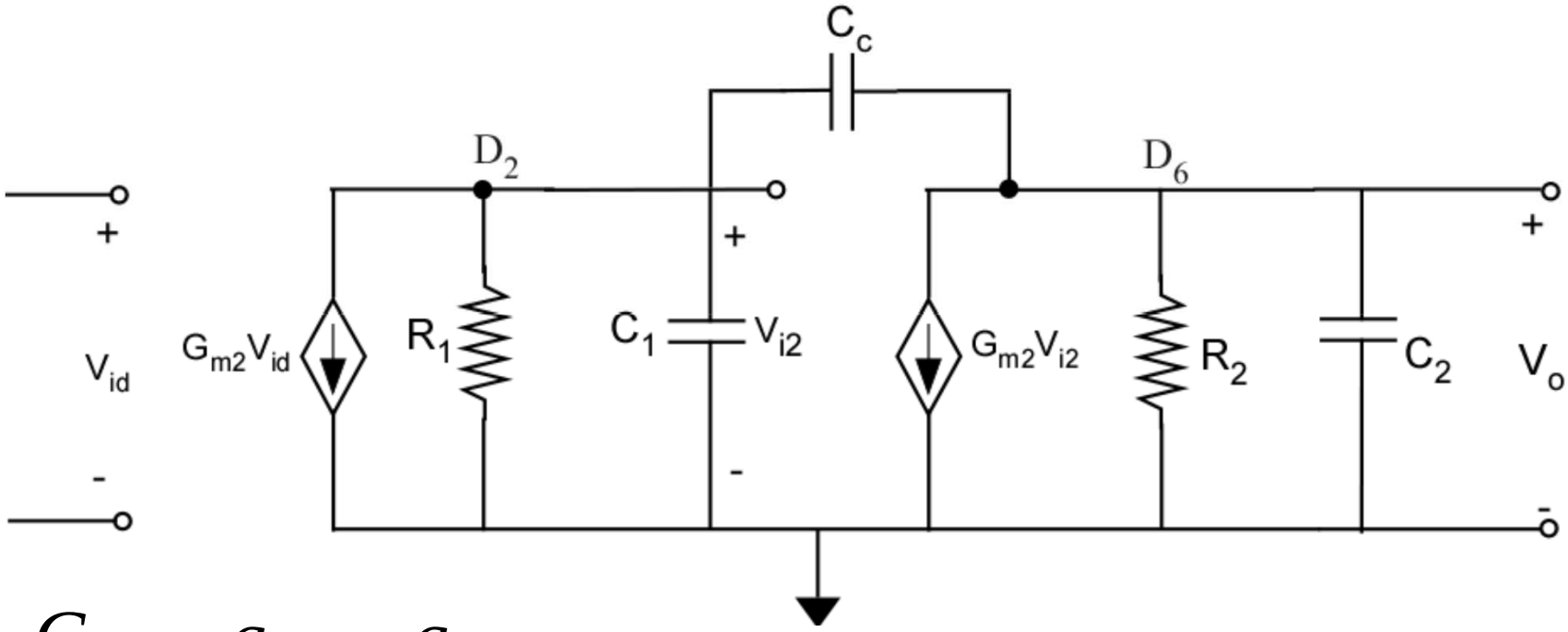
20 log1109 = 61 dB

2-Stage Op Amp Design Table

	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
W/L	20/0.8	20/0.8	5/0.8	5/0.8	40/0.8	10/0.8	40/0.8	40/0.8
$I_D(\mu A)$	45	45	45	45	90	90	90	90
$\lvert V_{ov}\rvert$ (v)	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3
$\lvert V_{GS}\rvert$ (v)	1.1	1.1	1.0	1.0	1.1	1.0	1.1	1.1
g_m(mA/V)	0.3	0.3	0.3	0.4	0.6	0.6	0.6	0.6
$r_o(k\Omega)$	222	222	222	222	111	111	111	111

2-Stage Op Amp – Frequency Response

Incremental Circuit



$$G_{m1} = g_{m1} = g_{m2}$$

$$R_1 = r_{o2} \parallel r_{o4}, \quad C_1 = C_{gd4} + C_{db4} + C_{gd2} + C_{db2} + C_{gs6}$$

2-Stage Op Amp – Frequency Response

$$G_{m2} = g_{m6}$$

$$R_2 = r_{o6} \| r_{o7}, \; C_2 = C_{db6} + C_{db7} + C_{gd7} + C_L$$

C_L is the load capacitance (usually large) $\Rightarrow C_2 \gg C_1$

$$\frac{V_o}{V_{id}} = \frac{G_{m1}\left(G_{m2} - sC_C\right)R_1R_2}{1 + sA + s^2B}$$

2-Stage Op Amp – Frequency Response

$$A = C_1 R_1 + C_2 R_2 + C_C \left(G_{m2} R_1 R_2 + R_1 + R_2 \right)$$

$$B = \left[C_1 C_2 + C_C \left(C_1 + C_2 \right) \right] R_1 R_2$$

Transmission zero at $s = s_Z$ with

$$\omega_Z = \frac{G_{m2}}{C_C}$$

Two poles that are the root of the denominator

$$\omega_{p1} \cong \frac{1}{R_1 C_C G_{m2} R_2} \qquad \omega_{p2} \cong \frac{G_{m2}}{C_2}$$