Texas A&M University

Computer and Electrical Engineering Department

Analog & Mixed Signal Center

ECEN 607: *Advanced Analog Circuit Design*

Homework 5

By

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Problem 1: Derive differential gain and PSRR expressions for the basic OTA

In this problem, the differential gain is obtained by analyzing the circuit showed in fig 1 as a single inverter with an active load. For the PSRR expressions the circuit is divided by two cuts showed in fig 1 as C1 for Vdd and C2 for Vss and analyzed as explained in [1].

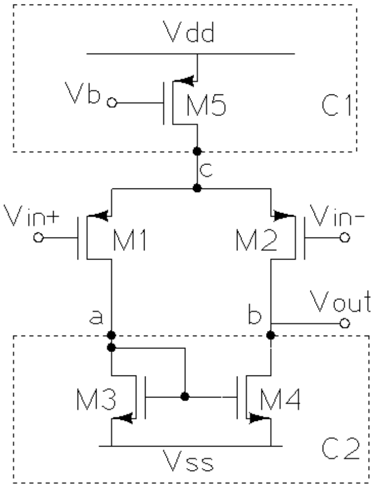

Figure 1 Simple OTA schematic

For the A_{Vdiff}, the analysis is the following:

$$Io = -gm2 \cdot Vin$$

$$Vo = Io \cdot Zout = -gm2/(go2 + go4) \cdot Vin$$

$$\boxed{A_{Vdiff} = \frac{Vo}{Vin} = \frac{-gm2}{(go2 + go4)}}$$

For the PSRR-, the C2 cut is used and the current passing through the points **a** and **b** is used for analysis as follows:

$$gmp{-}{\rightarrow}\ Io = i_{M2} - i_{M4} = (go2 + go4 + sCpa + sCpb)Vss$$

$$\boxed{PSRR{-}= \frac{GM}{gmp-} = \frac{gm1}{go2 + go4 + sCpa + sCpb}}$$

Where sCp is the total parasitic capacitances in node a and parasitic capacitances in node b. The current flowing from Vss to Vout goes directly through go4 and other path is through M3 as a current buffer and M1 then goes through the source of M2 and finally reach Vout.

For the PSRR+, the C1 cut is used and the point c is used for the analysis as follows:

$$gmp+\rightarrow Io = i_{M2} - i_{M4} = \frac{Vdd}{\left((go5 + sCpc)\left(\frac{gm2 - gm1}{gm2 + gm1}\right)\right)}$$

$$\boxed{PSRR+= \frac{GM}{gmp+} = \frac{gm1}{\left((go5 + sCpc)\left(\frac{gm2 - gm1}{gm2 + gm1}\right)\right)}}$$

Where the current flowing from Vdd gets divided by the current divider seen at the sources of M1 and M2. Then one half of the current goes directly to Vout and the other half goes through the current buffer of M1, then by the current mirror this currents gets reflected and added to Vout.

Problem 2: Derive differential gain and PSRR expressions for the current feedback and voltage feedback Amplifiers

For the second problem there are two circuits to be analyzed so for the first one, it has a voltage amplifier as a gain boosting for the current mirror acting as an active load to boost the output impedance to increase the output gain. The configuration is showed is fig 2.

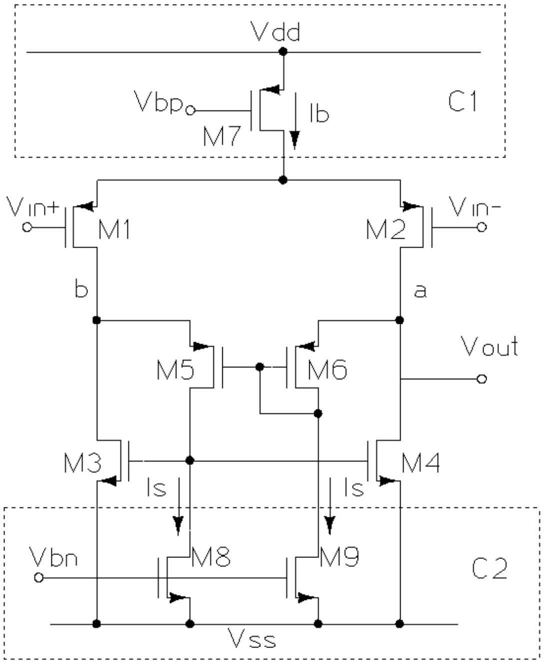

Figure 2 Transconductance with Current Amplifier

The circuit in fig 2 has two feedback loops with one common node; it has a negative loop that decreases the impedance in node b by the gain of the current amplifier and a positive loop that increases the output impedance at node a by the gain of the current amplifier. In order to prove this founding the voltage gain is obtained, the following diagram showed in fig 3 is used.

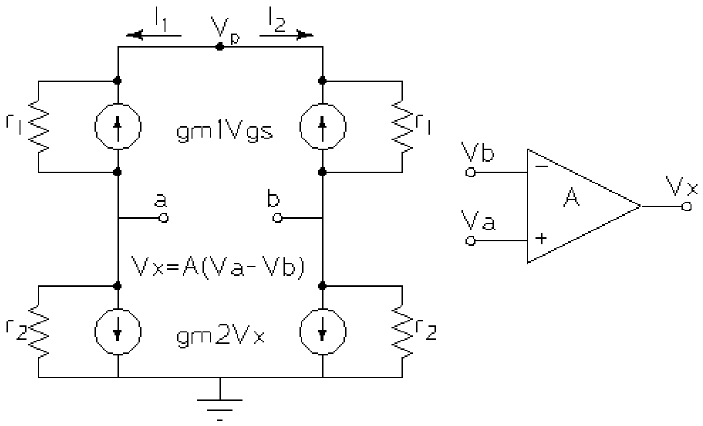

Figure 3 Equivalent model for circuit with feedback loops

Then using fig 3, the differential gain is obtained:

$$I_1 = -gm1(Vi - Vp) + \frac{(Vp - Va)}{r1} = gm2Vx + \frac{Va}{r2}$$

$$I_2 = -gm1(-Vi - Vp) + \frac{(Vp - Vo)}{r2} = gm2Vx + \frac{Vo}{r2}$$

Having by KCL, I_1+I_2=0 then

$$Vp = \frac{Va + Vo}{2(1 + gm1r1)}$$

$$Vx = -\frac{Va + Vo}{2gm2r2}$$

Knowing that Vx=A(Va-Vb) and plugging this in the previous equations:

$$Vp = \frac{gm2r2Vo}{(1 + gm1r1)(gm2r2 + \frac{1}{2A})} \quad \leftrightarrow \quad Vx = -\frac{Vo}{gm2r2 + \frac{1}{2A}}$$

Then plugging these results in I_2 equation we obtain:

$$gm1Vi = gm2Vx + \frac{Vo}{r2} - gm1Vp - \frac{Vp}{r1} + \frac{Vo}{r1} = \left[\frac{gm2}{(gm2r2 + \frac{1}{2A})}\left(1 - \frac{r2}{r1}\right) + \frac{1}{r1} + \frac{1}{r2}\right]Vo$$

Therefore the differential gain is given by

$$\boxed{A_{Vdiff} = \frac{gm1r1r2(Agm2r2 + 1)}{(r1 + r2)} \approx \frac{gm1Agm2r2}{(go1 + go2)}}$$

From this equation we can see the boosting factor of Agm2r2 that gives the increase in gain. In order to obtain the PSRR expressions for this circuit the cuts C1 and C2 are used for PSRR+ and PSRR- respectively. For the PSRR+, we are going to have the same expression as in problem 1 because the current flowing from Vdd to the output node goes through the same paths. So the expression is give by

$$gmp{+}\rightarrow Io = i_{M2} - i_{M4} = \frac{Vdd}{\left((go7 + sCp7)\left(\frac{gm2 - gm1}{gm2 + gm1}\right)\right)}$$

$$\boxed{PSRR+=\frac{GM}{gmp+}=\frac{gm1}{\left((go7+sCp7)\left(\frac{gm2-gm1}{gm2+gm1}\right)\right)}}$$

For the PSRR-, the current flowing from Vss is directly injected by M4 and assuming perfect matching between M5 and M6 we don’t have a current contribution though them because at the end these currents get canceled between each other at the output node. Another contributor for this current is through M3 that flows to M1 then through M2 as a current buffer and finally reachs the output node.

As an approximation to explain the behavior of the circuit, the output impedance should be very large due the positive feedback loop that increase that impedance acting as an open circuit for the current flowing from Vss, also the negative feedback loop is making the impedance at node b very small acting as a short circuit and allowing the current from Vss to flow directly through the output so the gmp is going to be close to 1 an is given by:

$$gmp-\longrightarrow Io=i_{M2}-i_{M4}=(gob+goa+sCpa+sCpb)Vss$$

$$\boxed{PSRR-=\frac{GM}{gmp-}=\frac{gm1}{gob+goa+sCpa+sCpb}\approx\frac{gm1}{gob+sCpb}\approx Av}$$

Where the admittance in node a is really small due the positive feedback loop and the admittance in node b is very large due the negative feedback and is going to be more dominant at high frequencies. The PSRR- is going to be almost equal to the voltage gain of the circuit giving a good PSRR- response due the fact that this gain is going to be very high.

For the second circuit showed in fig 4, the analysis is similar to the previous OTA. First we need to obtain the voltage gain. This circuit has two feedback loops one positive loop that will increase the output impedance proportionally to the gain of the voltage amplifier and another loop that will decrease the impedance at the drain of M1 due the negative feedback.

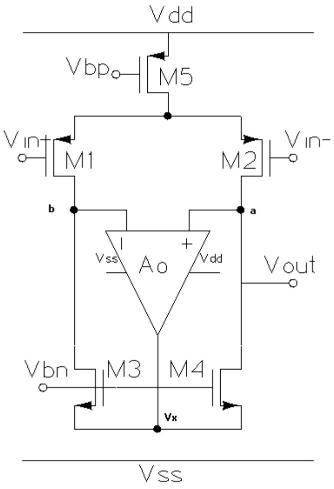

Figure 4 Transconductance with voltage amplifier

First the voltage gain is obtained as follows, assuming the voltage at node b equals to Ac ground:

$$Vx = Ao \cdot V_{test}$$

$$I_{test} = \frac{V_{test} - Vx}{Za} + gm4 \cdot Vx = V_{test}\left[\left(\frac{1 - Ao}{Za}\right) + gm4 \cdot Ao\right]$$

$$\boxed{Av = gm1 \cdot Zout = \frac{gm1}{(1 - Ao)goa + gm4Ao} \approx \frac{gm1}{Ao(goa - gm4) + go1}}$$

Where goa =go2+go4+sCpa and Cpa is the parasitic capacitances at node a.

For the PSRR expressions the same analysis as in the previous amplifier is used. For the PSRR+ the path from Vdd to the output node is through M5 and the current gets divided by the impedances at the sources of M1 and M2, then it travels to the output node as:

$$gmp+ \rightarrow Io = i_{M2} - i_{M4} = \frac{Vdd}{\left((go5 + sCp5)\left(\frac{gm2 - gm1}{gm2 + gm1}\right)\right)}$$

$$\boxed{PSRR+= \frac{GM}{gmp+} = \frac{gm1}{\left((go5 + sCp5)\left(\frac{gm2 - gm1}{gm2 + gm1}\right)\right)}}$$

For the current flowing from Vss to the output node there is a special consideration because this circuit isn't connect directly to Vss due the Active load sources are floating and connected to the output of the voltage amplifier in feedback. So the current from Vss comes through the voltage amplifier and M3 and M4, where the bias transistor is connected to Vss and it reflects the current from Vss to the output nodes. So basically the gain from Vss to the output node is close to one.

$$gmp- \rightarrow Io = i_{M2} - i_{M4} = (gob + goa + sCpa + sCpb)Vss$$

$$\boxed{PSRR-= \frac{GM}{gmp-} = \frac{gm1}{gob + goa + sCpa + sCpb} \approx \frac{gm1}{gob + sCpb} \approx Av}$$

Where the admittance in node a is really small due the positive feedback loop and the admittance in node b is very large due the negative feedback and is going to be more dominant at high frequencies. The PSRR- is going to be almost equal to the voltage gain of the circuit giving a good PSRR- response due the fact that this gain is going to be very high. This behavior is similar to the one observed in the previous amplifier.

Problem 3: Design two amplifiers with feedback loops to increase gain

The objective of this problem is to design a single stage amplifier with different feedback loop implementations that meets all the requirements listed in table 1.

Parameter	Value
A_{vo}(DC)	> 60dB
GBW	>10MHz
Phase Margin	>50°
Slew Rate	>1.7V/µs
Settling Time	<100ns
C_L	30-50pF

Table 1 Amplifier Requirements

The two implementations are using AMI 0.6µm Technology. The design procedure was the same as the one in problem 1 in Homework 2 and only special considerations for each circuit was taken.

In order for the first circuit to be stable the current I_1 must be less than the current flowing through the branches of M3 and M4 in fig 2. So for this case it was chosen to be 1/10th of the current. Also in order to get the indicated bandwidth the following equation was use:

$$gm1 = 2\pi \cdot GBW \cdot C_L = 2\pi(10x10^6)(50x10^{-12}) = 3.14\ mA/V$$

As can be seen in the above equation a huge transconductance is needed in gm1 in order to get the bandwidth that makes impossible to achieve this with the current consumption specification, so the current consumption was increased in order to get the GBW specification. The results for this implementation are showed in table 2 and the plots are below.

Parameter	Specification	Simulation
A_{vo}(DC)	> 60dB	60dB
GBW	>10MHz	13MHz
Phase Margin	>50°	90°
Slew Rate +	>1.7V/µs	6.7V/µs
Slew Rate -	>1.7V/µs	6.2V/µs
Settling Time	<100ns	73ns
PSRR+@DC	-	-80 dB
PSRR-@DC	-	-62dB
CMRR	-	80dB

Table 2 OTA with current amplifier results

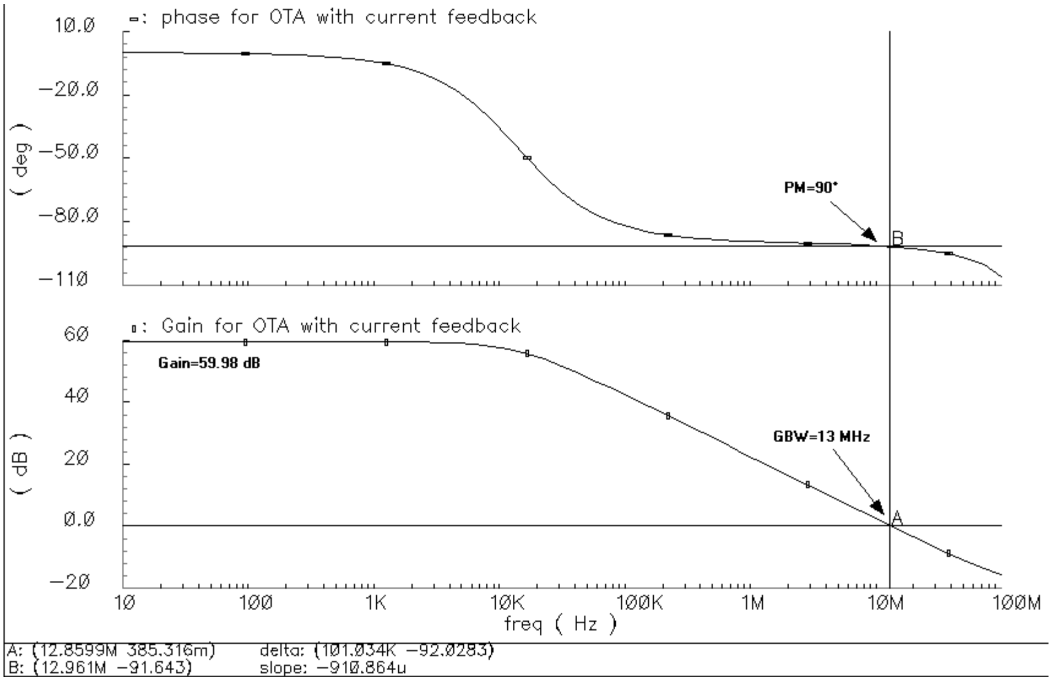

Figure 5 Ac analysis for the OTA with current amplifier

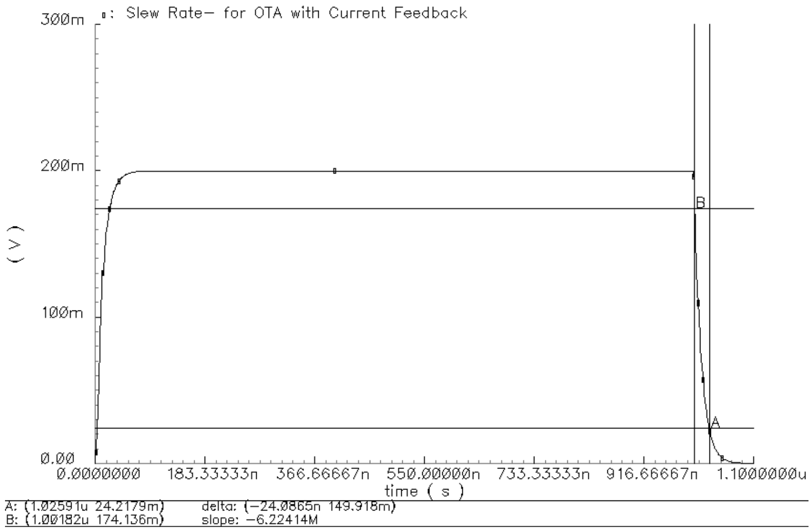

Figure 6 Slew Rate - for OTA with current amplifier

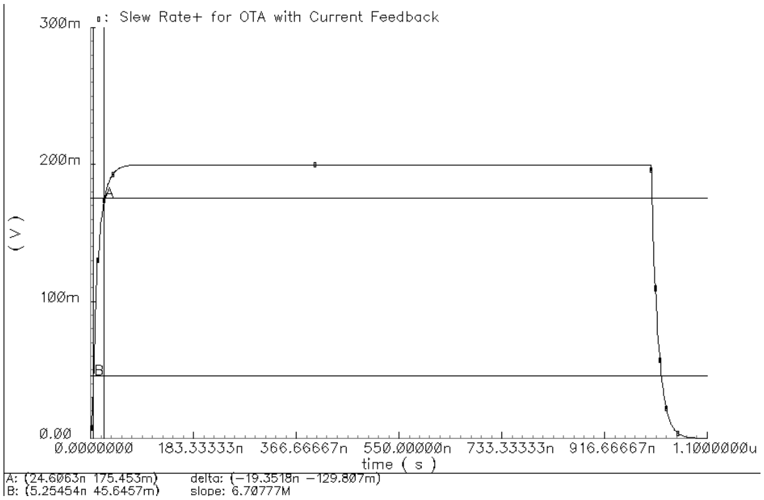

Figure 7 Slew Rate + for OTA with current amplifier

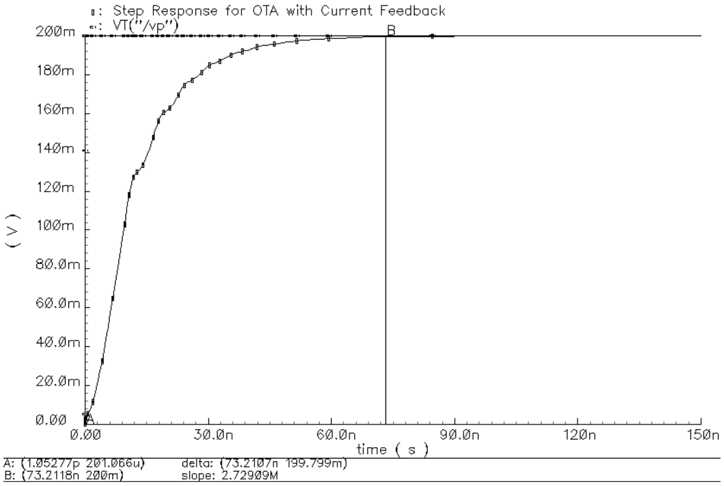

Figure 8 Settling Time for OTA with current amplifier

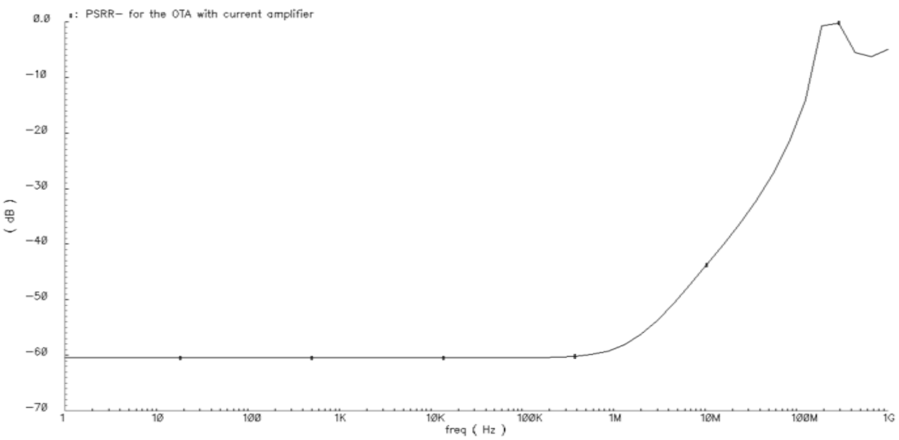

Figure 9 PSRR- for the OTA with current amplifier

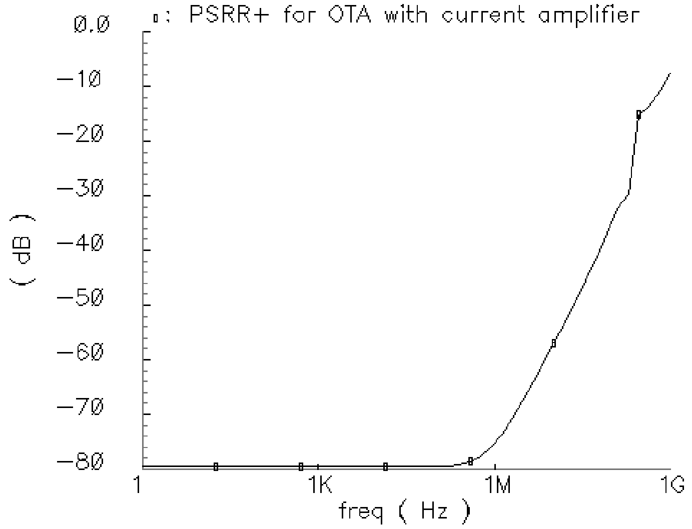

Figure 10 PSRR+ for the OTA with current amplifier

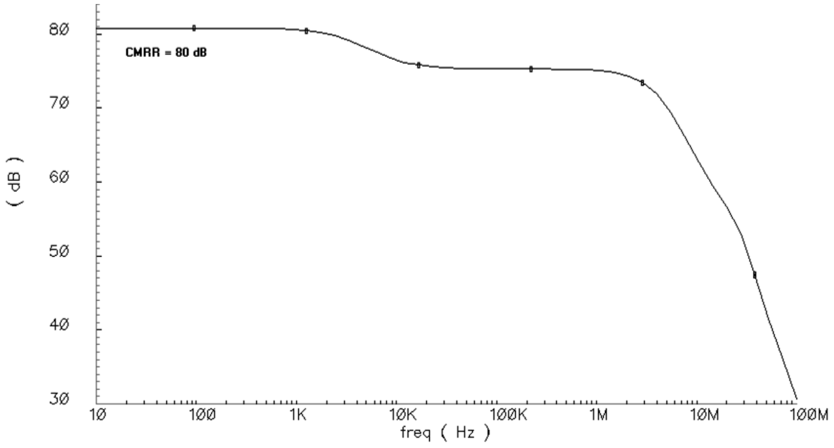

Figure 11 CMRR for the OTA with current amplifier

For the second OTA the same consideration as in the first OTA was assumed. Also we maintain the same current consumption in order to compare the results between both implementation in a fair way and with this make sure that only the feedback amplifier is being modified. The results for the second OTA with voltage amplifier in the active load are showed below in table 3.

Parameter	Specification	Simulation
A_{vo}(DC)	> 60dB	77.5dB
GBW	>10MHz	13.53MHz
Phase Margin	>50°	90°
Slew Rate +	>1.7V/µs	6.18V/µs
Slew Rate -	>1.7V/µs	7.12V/µs
Settling Time	<100ns	84ns
PSRR+@DC	-	-80 dB
PSRR-@DC	-	-90 dB
CMRR	-	95dB

Table 3 Results for OTA with voltage amplifier

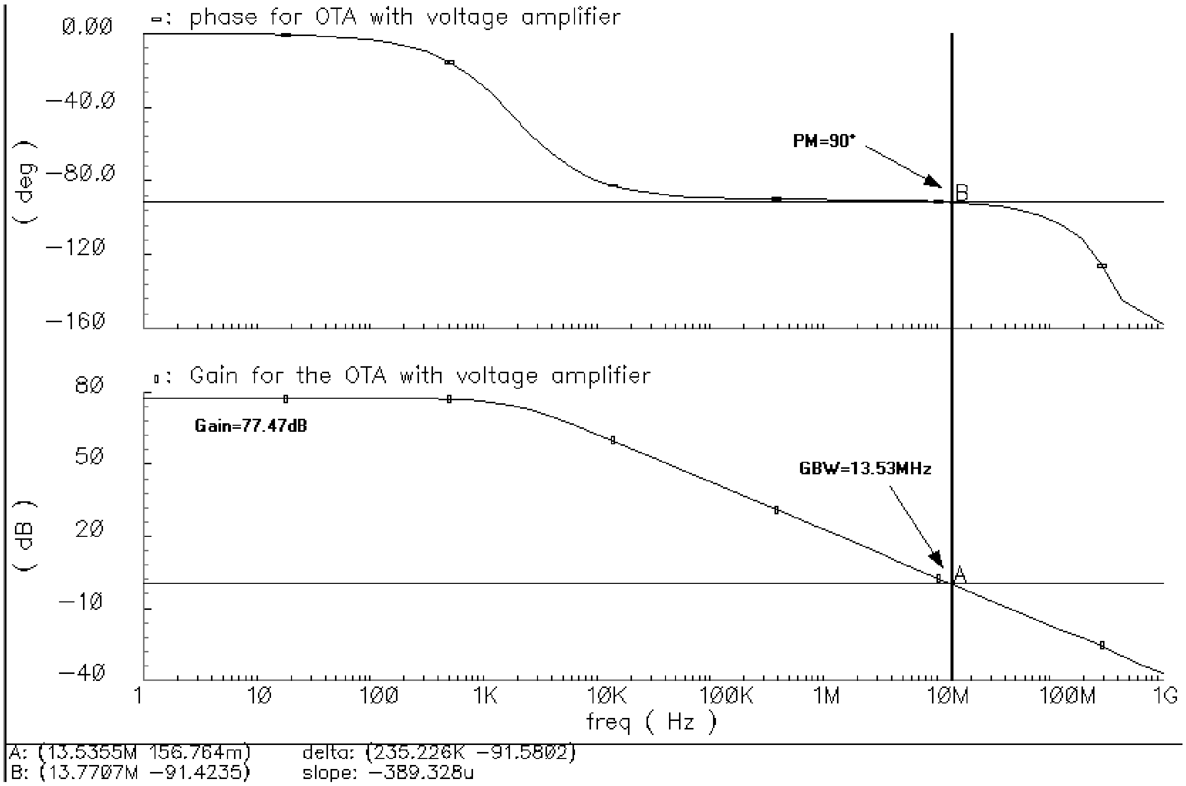

Figure 12 AC analysis for the OTA with voltage amplifier

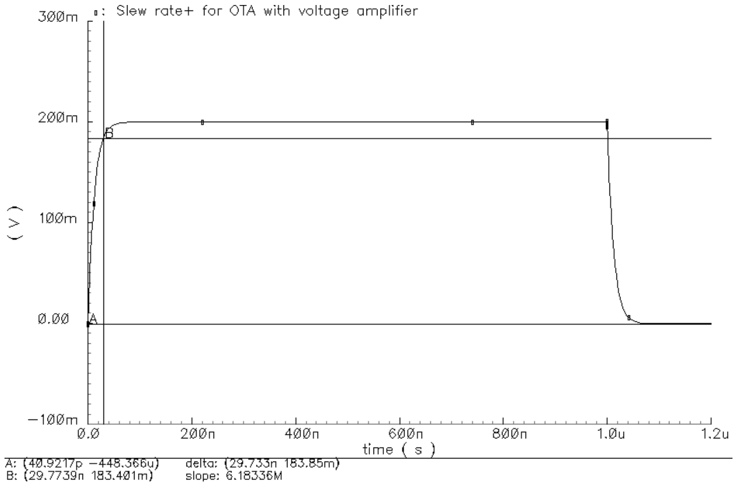

Figure 13 Slew Rate + for OTA with voltage amplifier

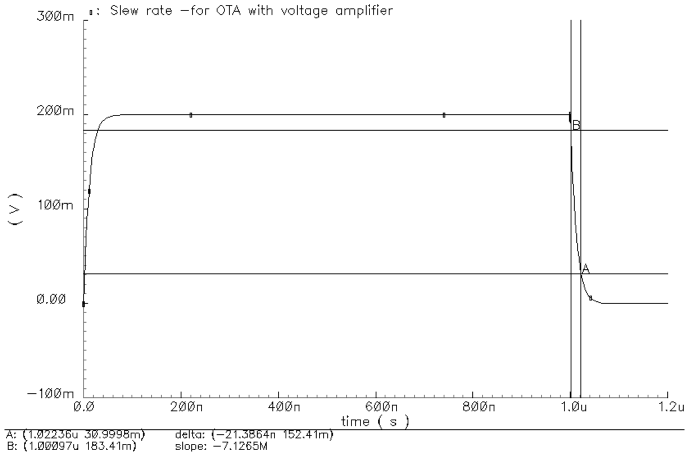

Figure 14 Slew Rate - for OTA with voltage amplifier

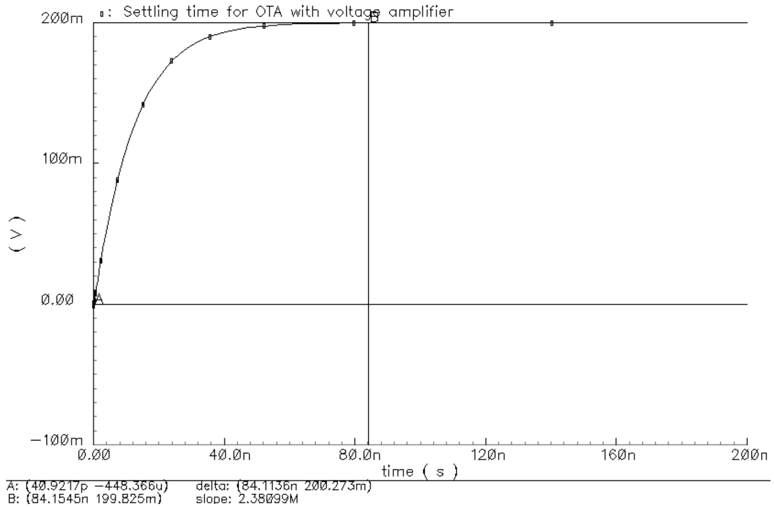

Figure 15 Settling time for OTA with voltage amplifier

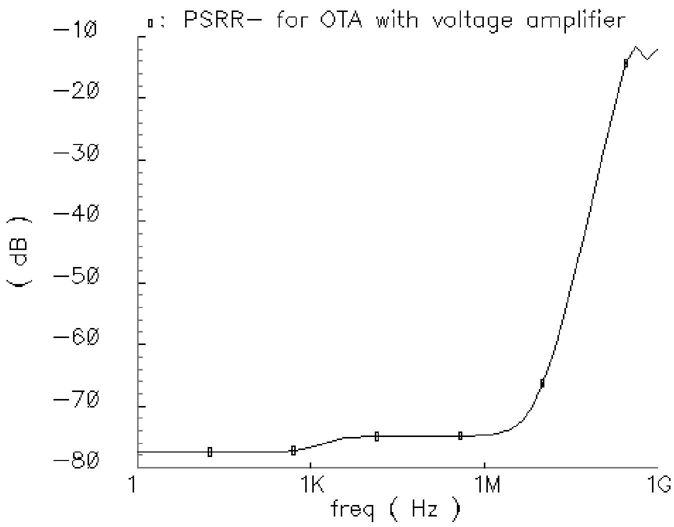

Figure 16 PSRR- for OTA with voltage amplifier

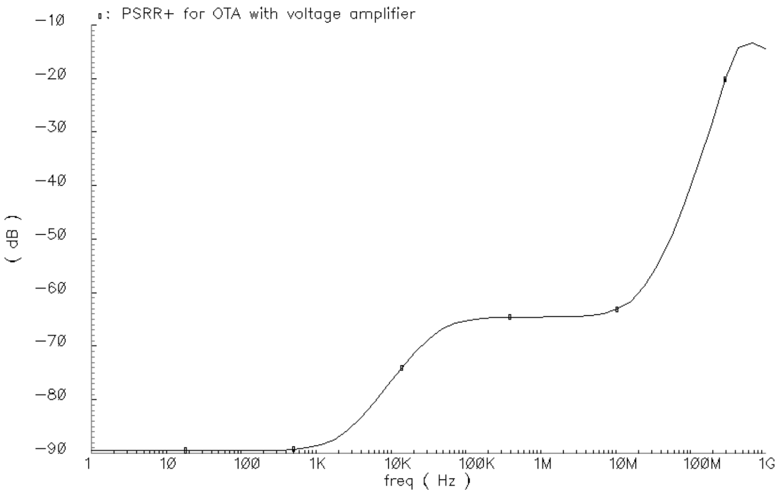

Figure 17 PSRR+ for OTA with voltage amplifier

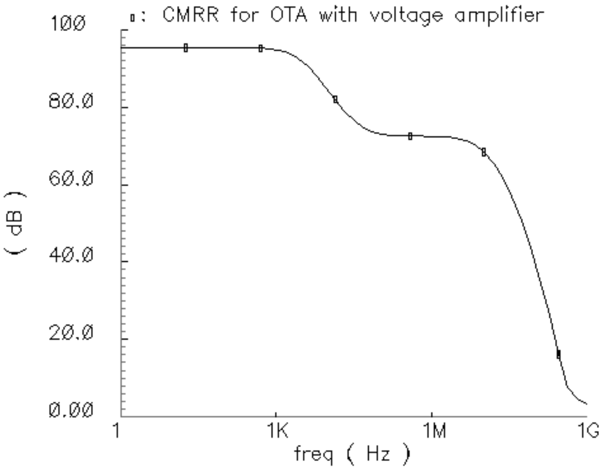

Figure 18 CMRR for OTA with voltage amplifier

In order to compare the results of both implementation and look their improvements a simple OTA without gain boosting was designed with the same bias current and results for the AC analysis are shown in the figure below.

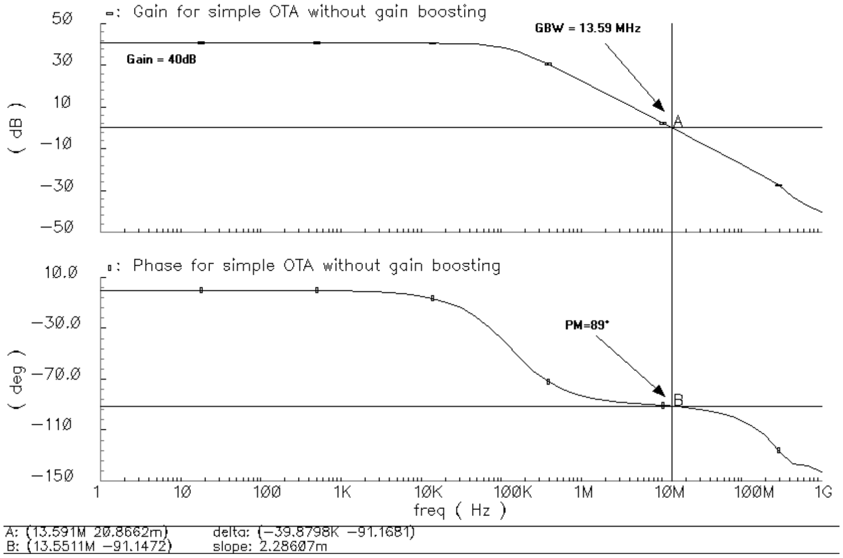

Figure 19 Gain for the simple OTA without Gain boosting

The final results to compare the implementations are show in table 4.

Parameter	Specification	Voltage Amp	Current Amp	Simple OTA
A_{vo}(DC)	> 60dB	77.5dB	60dB	40dB
GBW	>10MHz	13.53MHz	13MHz	13.59MHz
Phase Margin	>50°	90°	90°	89°
Slew Rate +	>1.7V/μs	6.18V/μs	6.7V/μs	-
Slew Rate -	>1.7V/μs	7.12V/μs	6.2V/μs	-
Settling Time	<100ns	84ns	73ns	-
PSRR+@DC	-	-80 dB	-80 dB	-
PSRR-@DC	-	-90 dB	-62dB	-
CMRR	-	95dB	80dB	-

Table 4 Final results for all the OTA for comparison

In conclusion we can see that the gain boosting effect increases the gain significantly compared with the simple OTA. Also the differences between the voltage and current amplifiers implementation in the gain boosting are more noticeable in the transient response than in the AC responses were they remain almost the same. The current amplifier is faster. The voltage amplifier implementation has better PSRR- due the fact that its nodes aren't connected directly to Vss so the PSRR- is directly affected by the PSRR performance of the amplifier by itself. For both amplifiers there is a constraint in how much gain can they have due stability issues. The gain from Vss to the output results in one as can be seen in the PSRR- plot where it is proportional to the gain of the circuit, so if we increase the gain the PSRR response improves. This happens in both cases with the amplifiers in feedback at the active loads. They correspond with the plots.

Problem 4: Derive the effective capacitance of the following circuit

For this problem the ideal models for the opamp and current amplifier will be used as shown in fig X. The effective capacitance in the feedback loop will be amplified by the gain of the current amplifier times the gain of the voltage amplifier so this configuration is creating a super capacitor.

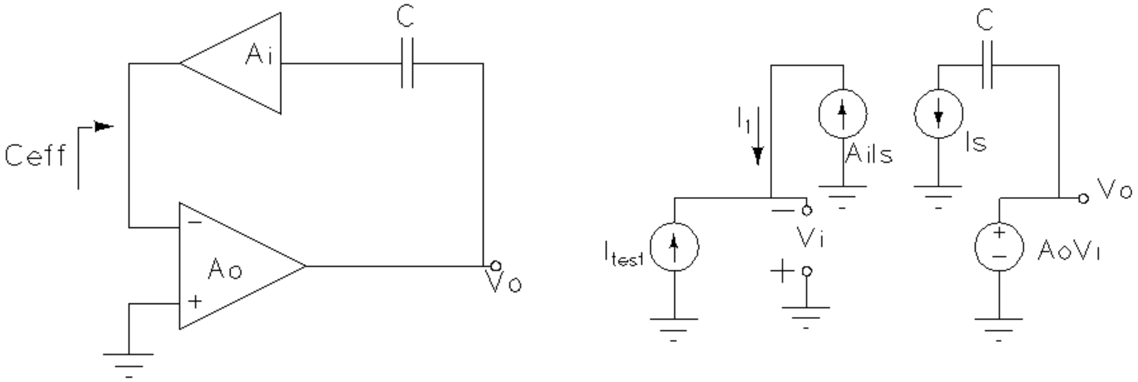

Figure 20 Capacitor in feedback with current amplifier and equivalent ideal model

In order to get the expression of the effective capacitance the fig X is used. Here we can see that:

$$Vo = Ao \cdot Vi = -Ao \cdot V_{test}$$

$$I_1 = Ai \cdot Is = -Ai \cdot Ao \cdot V_{test} \cdot sC$$

$$I_{test} = -I_1 = Ai \cdot Ao \cdot V_{test} \cdot sC$$

$$\boxed{Ceff = Ai \cdot Ao \cdot C}$$

References

[1] M. S. J. Steyaert and W. M. C.Sansen, “Power Supply Rejection Ratio in Operational Transconductance Amplfiers”, IEEETrans. On Circuits and Systems, Vol. 37, No. 9, pp 1077-1084, September 1990.

[2] Vadim, Ivanov, “Operational amplifier speed and accuracy improvement”, Kluwer academic publisher, 2004