

Untitled

Hi, All

I provide the spice model for Prob.2 of HW#8 here for you as a reference.

```
.model nmos nmos kp=60u vt0=0.7 lambda=0.03 ld=0 gamma=0.4 tox=20nm
cgs0=300pf cgd0=300pf cbd=80ff cbs=80ff
.model nmos4 nmos kp=60u vt0=0.7 lambda=0.03 ld=0 gamma=0.4 tox=20nm
cgs0=300pf cgd0=300pf cbd=12.6ff cbs=12.6ff
.model pmos pmos kp=30u vt0=-0.7 lambda=0.03 ld=0 gamma=0.4 tox=20nm
cgs0=300pf cgd0=300pf cbd=80ff cbs=80ff
.model pmos2 pmos kp=30u vt0=-0.7 lambda=0.03 ld=0 gamma=0.4 tox=20nm
cgs0=300pf cgd0=300pf cbd=2.06ff cbs=2.06ff
```

In the circuit, M4 use the model "nmos4" and all the other nmos use model "nmos". M2 use the model "pmos2" and all the other pmos use model "pmos". I already calculated the cap size and included in the spice model, so you do not need to include the device size in you spice netlist.

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