EE140 HW#5. solution

1.

a) Transistor M_{1s}, M_{2s} and R_s form the start up circuit for the reference circuit (M_1, M_2, M_3, M_4, M_5, M_6 and R_{ref}). Initially, gate of M_{1s} voltage is higher than gate voltage of M_5, so there is current flow through M_{2s} and it inject into the referen circuit. During the normal operation, gate voltage is less than gate voltage of M_5 so that M_{2s} is cut off. The start up circuit does not affect the normal operation of the reference circuit.

$I_{M_{2s}} \approx 0$.

b) KVL of the loop (M_5, M_6 and R_{ref}):

$$V_{GS5} = V_{GS6} + I_{DS6} R_{ref}$$

$\therefore V_{t5} + V_{dsat5} = V_{t6} + V_{dsat6} + I_{DS6} \cdot R_{ref}$

Since we ignore body effect: $V_{t5} = V_{t6} = V_{t0}$

$\therefore V_{dsat5} = V_{dsat6} + I_{DS6} \cdot R_{ref}$

$(\frac{W}{L})_6 = 4(\frac{W}{L})_5 \Rightarrow V_{dsat6} = \frac{1}{2} V_{dsat5}$

$\therefore V_{dsat5} = 2 V_{dsat6} = 2 I_{DS6} \cdot R_{ref}$

M_1, M_2, M_3, M_4 form wilso current mirror.

$\therefore I_{DS5} = I_{DS6} \Rightarrow V_{dsat5} = 2 I_{DS5} \cdot R_{ref}$

$\therefore g_{m5} = \frac{2 I_{DS5}}{V_{dsat5}} = \frac{1}{R_{ref}}$

(Notes: g_{m5} only depends on the reference resistor, this circuit called constant-g_m reference circuit)

C) $A_{dm} = g_{m8,9} \cdot R_D$ ($g_{m8} = g_{m9} = g_{m8,9}$)

Since $(\frac{W}{L})_7 = \frac{1}{2}(\frac{W}{L})_{8,9}$ $I_{DS7} = 2I_{DS8} = 2 I_{DS9}$

$\therefore g_{m7} = g_{m8} = g_{m9} = g_{m8,9}$

$g_{m7} = g_{m5}$ (since $I_{DS7} = I_{DS5}$ and $\left(\frac{W}{L}\right)_7 = \left(\frac{W}{L}\right)_5$)

$\therefore A_{dm} = g_{m8,9} \cdot R_D$

$= g_{m7} \cdot R_D = g_{m5} \cdot R_D = \frac{R_D}{R_{ref}} = 10$

2. (B)

Transistor M1, M2 and M3 form a Wilson current mirror. if we ignore C_{gd}

$\therefore i_{ds4} = i_{sd3}$ (since $(\frac{W}{L})_1 = (\frac{W}{L})_2 = (\frac{W}{L})_3$)

That means all the small signal current flow through M4 will mirror to the i_{ds3}.

Consider M4 as a common source with degeneration configuration.

The $\frac{V_o}{V_i} = \frac{V_{gs}}{V_i} \cdot \frac{V_o}{V_{gs}}$

V_{gs} is small signal gate voltage of MS.

$\frac{V_o}{V_{gs}}$ is a source follower configuration and

$\frac{V_o}{V_{gs}} = 1$.

$\therefore \frac{V_o}{V_i} = \frac{V_{gs}}{V_i} = \underbrace{\frac{g_{m4}}{1 + g_{m4} \cdot R}}_{\text{Gm of first stage}} \cdot \underbrace{r_{o3} \cdot (2 + g_{m3} \cdot r_{o2}}_{\text{Rout of first stage}}$

SPICE deck for Prob.1

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* Hw5 Prob.1

.include 'model.m'

Vdd vdd 0 dc 1.2
Rref 5 0    1k
Rs   vdd 6  380
Rl1 vdd vo+ 10k
Rl2 vdd vo- 10k
Vi+ vi+ 0 dc 0.9
Vi- vi- 0 dc 0.9

M1 1 1 vdd vdd   PMOS W=4u L=0.13u
M2 2 1 vdd vdd   PMOS W=4u L=0.13u
M3 4 3 1  1      PMOS W=4u L=0.13u
M4 3 3 2 2       PMOS W=4u L=0.13u
M5 4 4 0   0     NMOS W=4u L=0.13u
M6 3 4 5   5     NMOS W=16u L=0.13u
M2s 6 6 0  0     NMOS W=5u L=0.13u
M1s vdd 6 4 4    NMOS W=0.13u L=1u
M7 d7 4 0 0      NMOS W=4u L=0.13u
M8 vo+ vi- d7 d7 NMOS W=8u L=0.13u
M9 vo- vi+ d7 d7 NMOS W=8u L=0.13u

.op
.tf V(vo+,vo-) vi+
.end
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Output Result

gm5= 1.0034m

**** small-signal transfer characteristics

v(vo+,vo-)/vi+ **= 10.0817**
input resistance at vi+ = 1.000e+20
output resistance at v(vo+,vo-) = 19.4769k