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Homework #6
Due 10/08/03

EECS 140
Fall 2003

```
.model nmos
+    nmos level=1 tox=2.6n vt0=0.3 gamma=0.2 phi=0.6 u0=250 ld=0.025u
+    capop=0 acm=3 ldif=0 hdif=0.2u cj=8e-4 cjsw=8e-12 cjgate=8e-11
+    lambda=0.2
.model pmos
+    pmos level=1 tox=2.6n vt0=-0.3 gamma=0.2 phi=0.6 u0=100 ld=0.025u
+    capop=0 acm=3 ldif=0 hdif=0.2u cj=8e-4 cjsw=8e-12 cjgate=8e-11
+    lambda=0.15
```

When using the above models, remember to us W/Leff in your calculations, where Leff=L-2*Ld and Ld=0.025um. You can calculate k' directly from the SPICE model parameters u0 and tox.

1. A circuit as shown in Fig.1 has Vcc=15V, R = 5KΩ, $V_{CE(sat)}$ =0.2V, and V_{BE}=0.7V.
   (a) Sketch load lines in the I_{c1}- V_{CE1} plane for R_L = 2KΩ and R_L = 10KΩ.
   (b) Calculate the maximum average sinusoidal output power that can be delivered to R_L (both values) before clipping occurs in (a) above. Sketch corresponding waveforms for I_{c1}, V_{ce1}, and P_{c1}.
   (c) Calculate the circuit efficiency for each value of R_L in (b). (Neglect power dissipated in Q3 and R)
   (d) Select R_L for maximum efficiency in this circuit and calculate the corresponding average output power with sinusoidal signals.

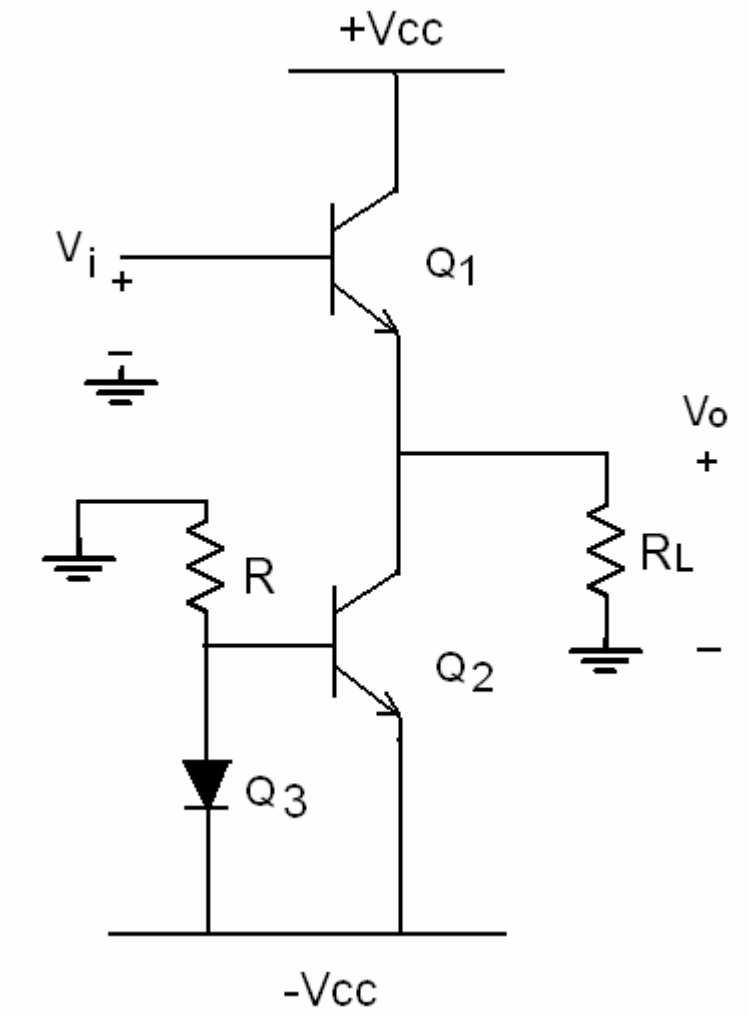

Fig. 1

2. Design a CMOS output stage based on the circuit of Fig.2 to deliver ±0.6V before clipping at V_o with R_L = 1KΩ and VDD = 1.2V. Use I_B = 10uA and 100uA idling current in M_{1a} and M_{1b}. Set $(W/L)_{4a} = (W/L)_{4b}$ = 0.5u/0.13u, $(W/L)_3$ = 0.2u/0.13u. Total chip area is to be minimized. Specify W/L for M_{1a}, M_{1b}, M_{2a}, M_{2b}. Use SPICE to verify your design by plotting the V_o vs V_i characteristic. Minimum L is 0.13u.

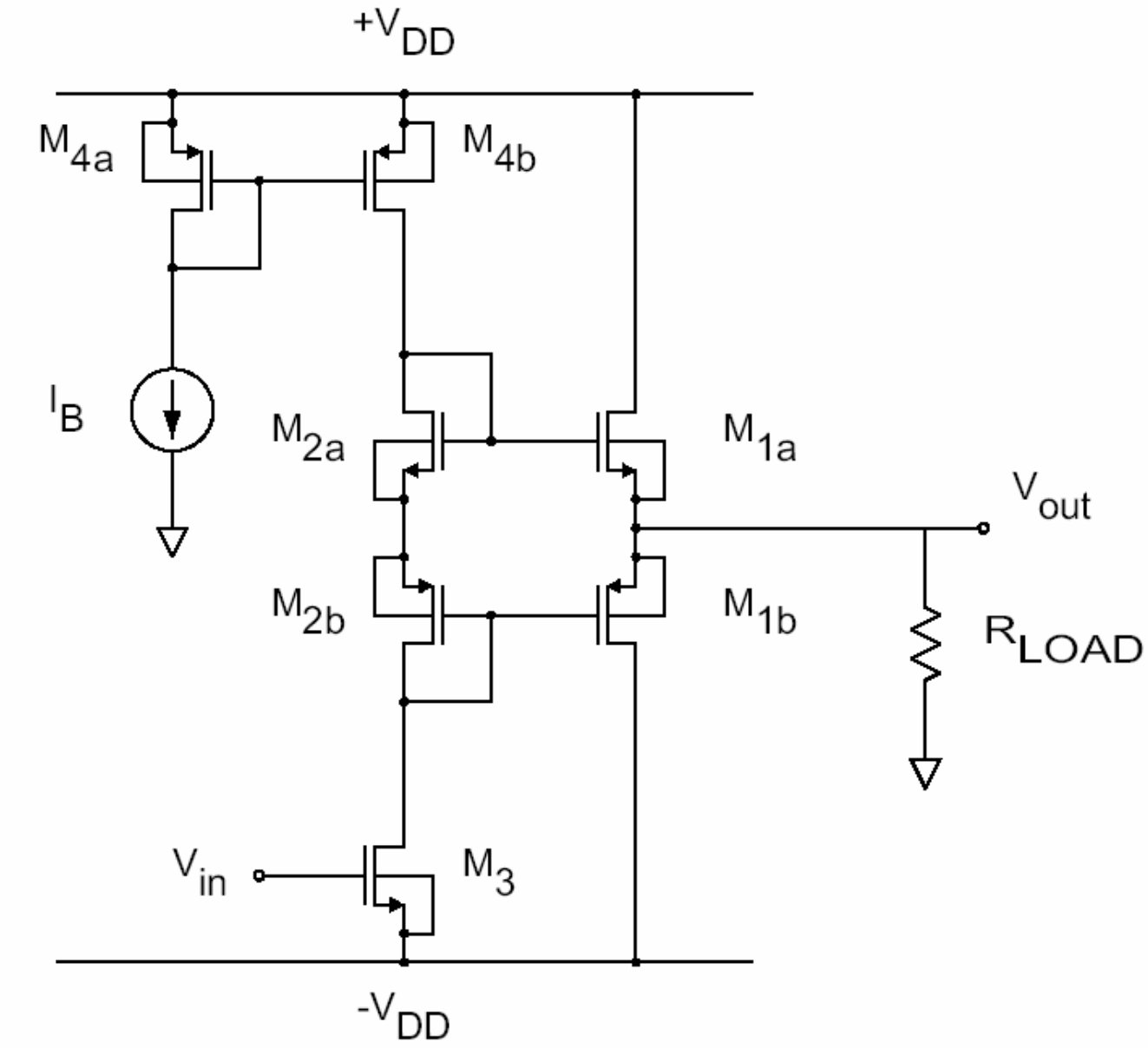

Fig. 2