UNIVERSITY OF CALIFORNIA AT BERKELEY
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Mike Chen	**(Due 3/30/04)**	**Spring 2004**

1) Compare the following current sources in figure 1, Kn'=200 μA/V^2, Kp'=100 μA/V^2, $(W/L)_1$=1, $(W/L)_2$=1, Vdd=1.2V, |Vtn|=|Vtp|=0.3V,
   a) Design R1, such that Iout is 1 μA, assuming γ=λ=0.
   b) Calculate the power supply sensitivity: ΔIout/ΔVdd, assuming γ=0, λn=0.05, λp=0.025.

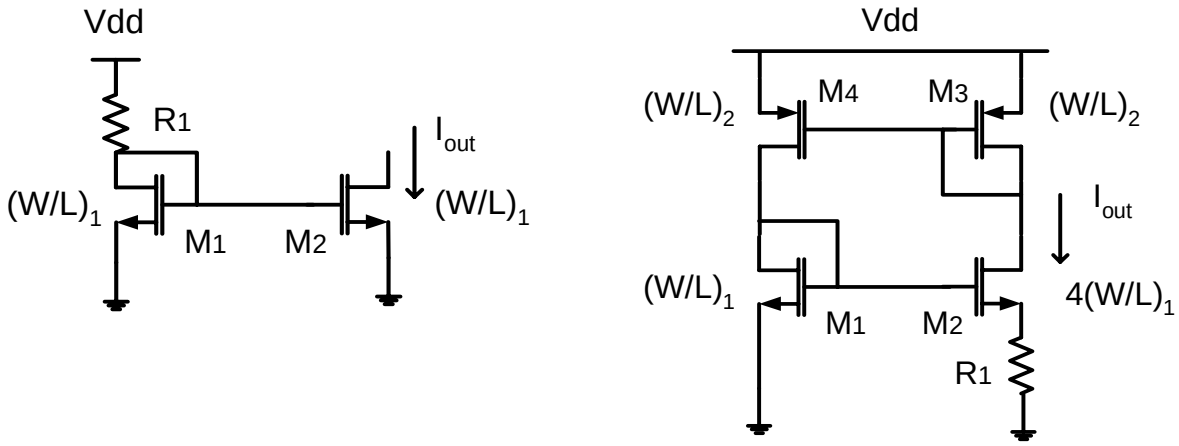

Figure 1

2) Given the output stage shown in figure 2, assuming L=0.13μm, Vsb=0 for all transistors, and Vdd=1.2V. Complete the following design:
   a) Choose (W/L), and Rref such that output swings from -0.8V to 0.8V with highest possible efficiency. You are free to choose the bias point of Vin. [$(W/L)_3=(W/L)_2$, all transistors operate in saturation region within the output swing range]
   b) Verify output swing range: Plot Vout vs. Vin for -1.2V < Vin < 1.2V in SPICE.
   c) Calculate efficiency of your design and verify with SPICE. [Hint: Input a sine wave such that output sine wave achieves amplitude of 0.8V.]

Device model:
.model nch nmos LEVEL=1 TOX=25 VTO=0.3 KP=100.0e-6 LAMBDA=0
+GAMMA=0.01 PHI=0.6

Spice Hint:
The following SPICE scripts will help you to measure efficiency.

```
.meas tran p_load avg p(RL)    *power to the load
.meas tran p_sup avg power     *power dissipated in supply
.meas tran eff param='100*p_load/p_sup'  *calculate efficiency
```

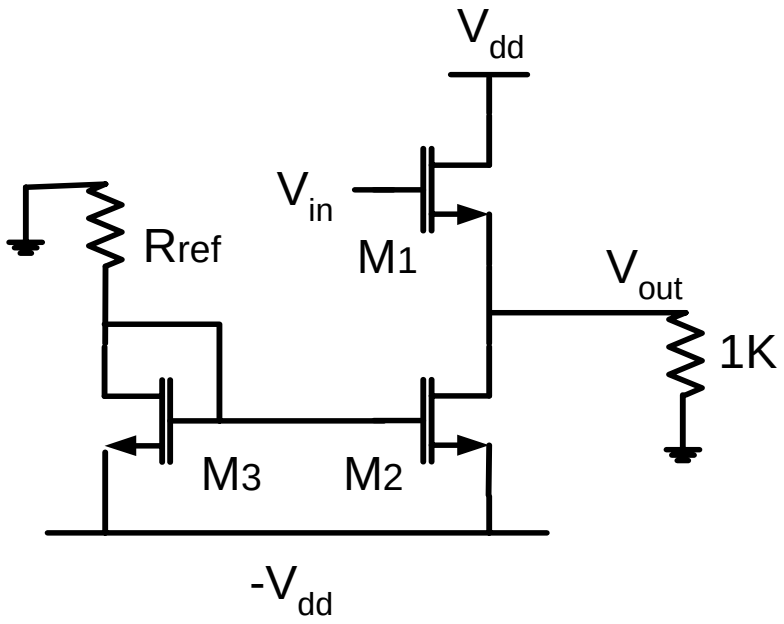

Figure 2

3) Redo the modified midterm problems, as posted on the website. Make approximations to be within 1%!