# University of California at Berkeley
# College of Engineering - Department of EECS

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## Homework #6

Due: Friday, April 4th, 5 pm 240 Cory

### Problem 1: Complex Logic

Figure 1 shows the block diagram of a digital circuit with two standard inverters and two complex logic gates. The details of the two complex logic gates are shown in Figure 2.

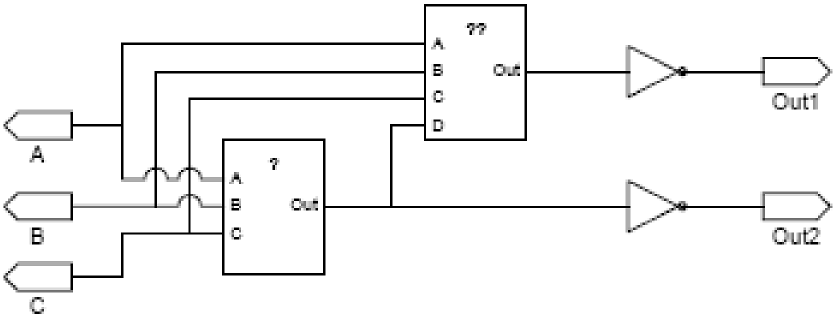


Figure 1: Block diagram of unknown logic circuit

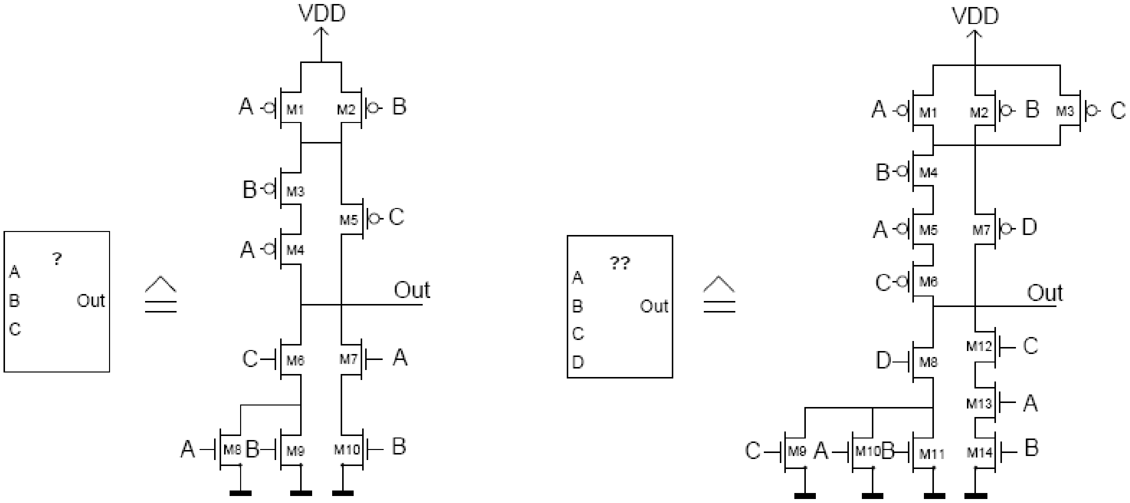


Figure 2: Transistor level schematic of logic gates in circuit of Figure 1.

1) Express Out1 and Out2 in terms of the input signals A, B and C.
   What functionality does the circuit implement?

?: $\text{Out} = \overline{AB+C(A+B)} = \overline{AB + AC + BC} = \overline{\text{carry}}$

??: $\text{Out} = \overline{ABC+D(A+B+C)} = \overline{\text{sum}}$

➔ Out1 = sum
➔ Out2 = carry

The circuit in Figure 1 implements a full adder

2) Size all the transistors in Figure 2, such that the gates "?" and "??" have a worst case pull-up and pull-down performance approximately equal to a unit sized inverter. When doing so try to minimize the maximum input capacitance seen at any input. Assume long channel devices, use integer ratios when scaling the devices and neglect body effect.

?:

| Device | Size |
|---|---|
| M1 | 3 |
| M2 | 3 |
| M3 | 6 |
| M4 | 6 |
| M5 | 6 |
| M6 | 2 |
| M7 | 2 |
| M8 | 2 |
| M9 | 2 |
| M10 | 2 |

??:

| Device | Size |
|---|---|
| M1 | 3 |
| M2 | 3 |
| M3 | 3 |
| M4 | 8 |
| M5 | 8 |
| M6 | 8 |
| M7 | 6 |
| M8 | 2 |
| M9 | 2 |
| M10 | 2 |
| M11 | 2 |
| M12 | 3 |
| M13 | 3 |
| M10 | 3 |

Note: The pull-up resistance for ?? when A, B and C are all low is only 17.5/18 times the equivalent pull-up resistance of an inverter. All other equivalent resistances are equivalent to the one of a standard inverter.

3) Calculate the logical effort of all the inputs of gates "?" and "??"

?: $LE_A = LE_B = 13/3$
$LE_C = 8/3$

??: $LE_A = LE_B = LE_C = 16/3$
$LE_D = 8/3$

4) Which input propagates fasted to the Out2? Considering your answer to 1), could there be any reason for giving that particular input priority?

Input C propagates fasted to Out2 since it is closest to the output in gate ?. Since Out2 is the carry output of the full-adder, it would make sense to optimize the propagation delay from the carry input to the carry output for most adder structures. Therefore C should be used as the carry input of the full-adder cell.

## Problem 2: Static CMOS vs. Pass-Transistor Logic

In this problem you are asked to compare static CMOS vs. Pass-Transistor Logic (PTL) based on a XNOR gate. A XNOR (Figure 3 shows the symbol) provides a high output signal whenever the two input signals are logically equal.

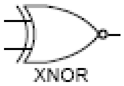
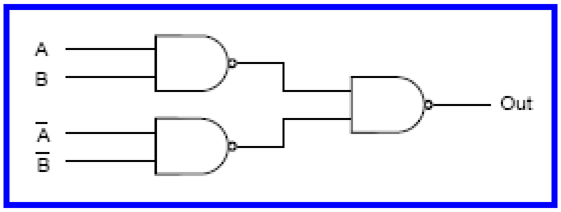


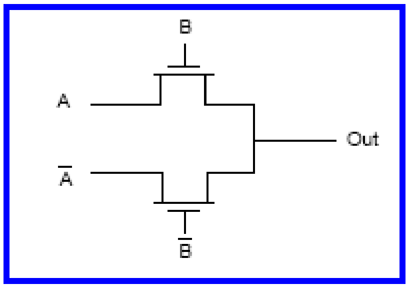
Figure 3: Symbol of XNOR

1) Design a 2-input XNOR in static CMOS. To simplify matters you can assume that you have both input polarities available (A & A`, B and B`). How many transistors do you need to build the XNOR?



12 transistors are needed to build the XNOR in complementary CMOS assuming both input polarities are available

2) Now design the same circuit in NMOS only PTL (no CMOS inverter at the output). Again, assume that both input polarities are available. How many transistors do you need now?



Here only 2 transistors are needed

3) Next you use the gates you just designed to build the circuit shown in Figure 4. You implement the same circuit one time using the CMOS XNOR gate and the second time using your PTL XNOR gate. You can assume that somehow magically you have the inverted output values of your single gates available as well (i.e. if Output = low = $V_{OL}$ then Output` = high = $V_{OH}$ and vice versa). Further assume $V_{DD} = 1.2$ V, $V_{Tn} = V_{Tp} = 0.3$ V and neglect body effect.

   a. Complete the timing diagram in Figure 5

   b. By purely looking at the voltage levels, which implementation would you prefer and why?

      Complementary CMOS is the preferred logic style here, since the logic HI level does not degenerate towards the output as it does for the PTL gates due to the $V_T$ drop per stage. In this particular PTL implementation the logic high level at the output is only VDD/2 at can therefore not even be used to drive a CMOS inverter directly anymore.

   c. Compare the two implementations with respect to their performance (elaborate).

      CMOS is also preferable in this implementation when it comes to speed since there is always only one equivalent resistor between VDD or GND to charge the capacitance at any node. The gates act as buffers. In the PTL implementation without CMOS inverters at the PTL output, the resistances add and the associated time constant therefore increases.

   d. Propose a solution utilizing NMOS and PMOS that helps to overcome some of the problems of the less favorable logic style. What are the pros and cons of your solution?

      One possibility would be to connect an inverter to the output of the PTL gate. This would restore the logic high levels at the output and speed up chains of gates (since it provides some buffering). A drawback of this solution is that increased static currents can flow in the inverter when the output of the gate is high, since $|V_{GS}|$ of the PMOS is not 0.

      Another possibility would be to use an inverter plus a small PMOS as a keeper. That would switch off the PMOS in the inverter harder and therefore reduce the static power consumption in the inverter. A minor drawback of this technique, on top of the increased transistor count, is that it is now harder to switch the output to zero, since the keeper transistor is “fighting” against the NMOS trying to pull down.

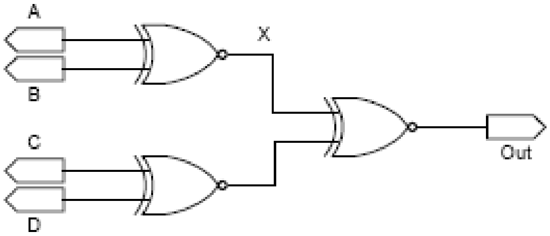


Figure 4: Cascade of XNORs

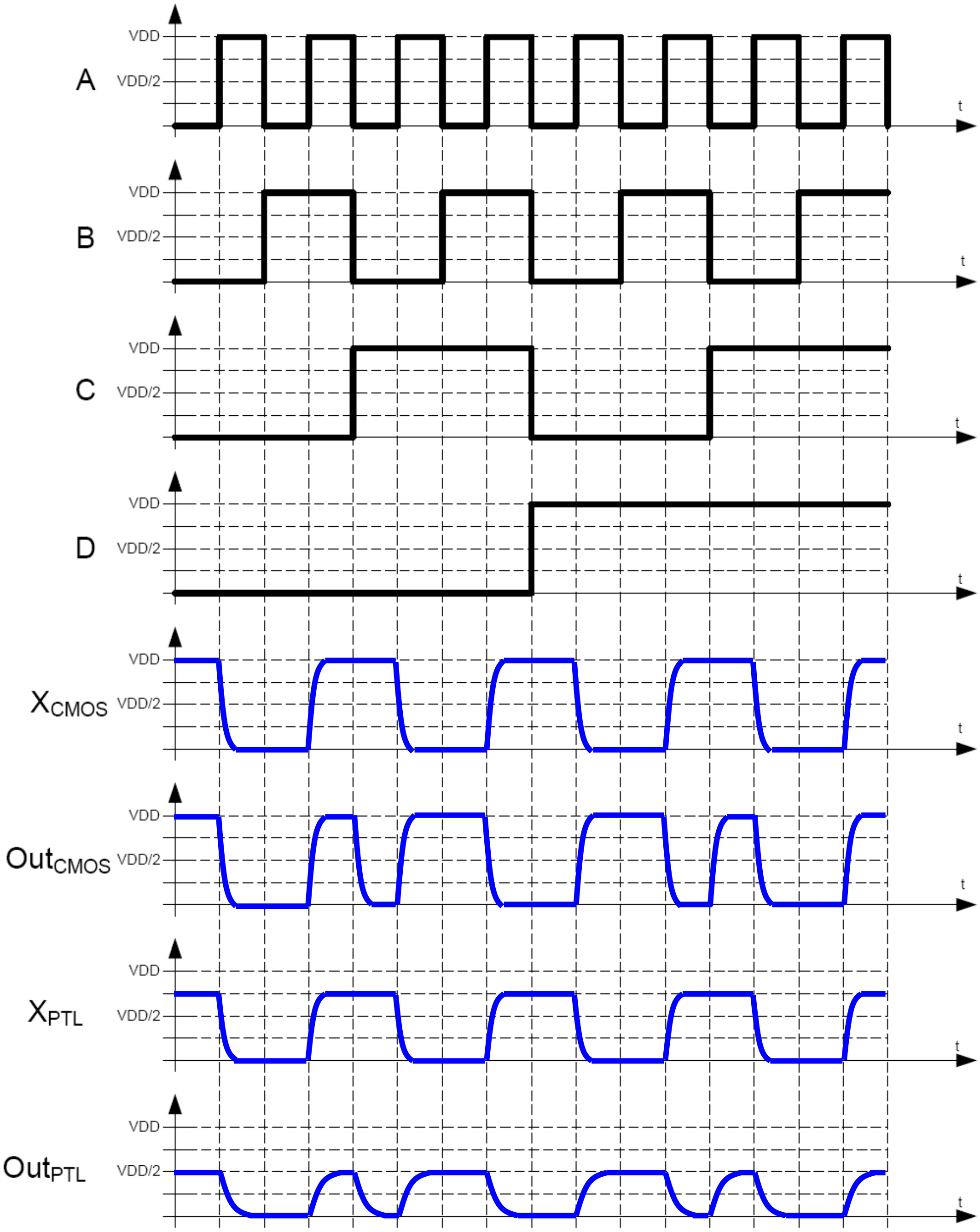
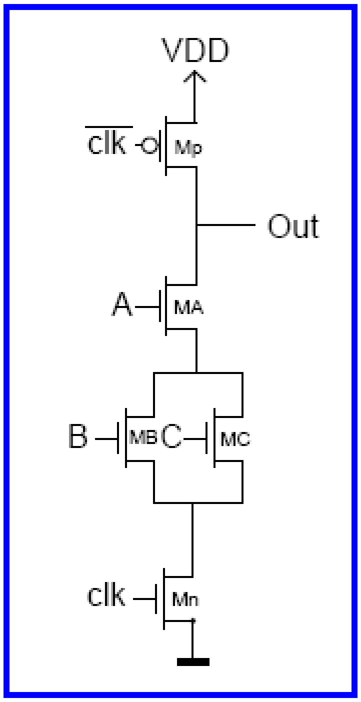


Figure 5. Timing diagram for circuit in Figure 4.

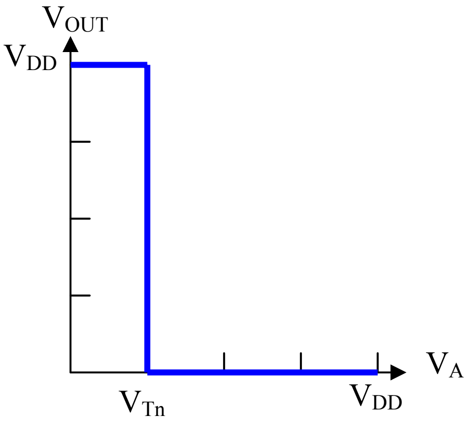
## Problem 3: Dynamic Logic

a) Implement the logic function given below with a single dynamic logic gate and optimize it with the fact that the input A is part of the critical path in mind.

$$\text{Out} = \overline{A(B+C)}$$



b) Draw the VTC (i.e. $V_{out}$ vs. $V_A$) for the case when B and C are high all the time and A transitions from low to high during the evaluation cycle. Assume $V_{DD}$ = 1.2 V and $V_{Tn}$ = 0.3 V



c) Size the input transistors (the ones that are not connected to the clk-signal; the “clk-transistors” can be considered to be ideal shorts during the evaluation cycle for this problem) such that the gate has the same pull down strength as a minimum inverter. Calculate the logical effort for your gate for a high-to-low transition at the output. Does your result make sense?

$M_A = M_B = M_C = 2$
$LE_A = LE_B = LE_C = 2/3$

A logical effort smaller then 1 is possible for dynamic gates, since they are usually optimized for one particular transition (H → L at the output in this case)

d) Assume an equivalent $C_L = 30$ fF and $C_S = C_D = 2$ fF (for the used transistor size, i.e. you don't need to multiply it by your scaling factor from c). Calculate the output voltage at the end of the evaluation cycle assuming B and C are low all the time and A transitions from low to high during the evaluation cycle. Assume that $f_{clk}$ is slow enough such that all the transients settle within the evaluation period.

Assuming the output voltage drops by less than $V_{Tn}$:

$\Delta V_{out} = -(V_{DD} - V_{Tn}) * 3C_S / C_L = 0.18$ V
→ Our assumption was correct!
→ $V_{out}' = 1.02$ V

e) In order to combat the effect of charge sharing you can add a circuit shown in Figure 6 (often referred to as inverter + level restoring transistor or keeper) to the output of your dynamic gate.

- Why do you think the size of the inverter is 4/1 instead of the usual 2/1? Does that make sense or is it a mistake?

  The inverter is sized 4/1 to have a higher switching threshold ($V_M$) which makes the output flip sooner when a high-to-low transition occurs (the only possible transition for a dynamic NMOS gate) and therefore increases the speed of the gate slightly.

- What is the maximum $W_K/L_K$ of the keeper transistor that still guarantees full functionality of your gate?
  ($V_{DD} = 1.2$ V, $V_{Tn} = V_{Tp} = 0.3$ V, $k_n' = 180$ uA/V$^2$, $k_p' = 90$ uA/V$^2$, $\lambda_n = \lambda_p = 0.5$, $V_{satn} = 0.3$ V, $V_{satp} = 0.6$ V, min. W/L = 0.12/0.1 um)

  In order to make sure the output of the gate can be pulled to logic low, the NMOS have to be able to pull the output voltage below the threshold voltage of the NMOS device (to make sure the inverter flips). A less conservative approach would require the output voltage to be only pulled below the switching threshold of the 4/1 inverter (which is approx. 0.65 V). Both solutions are ok. All the transistors in the pull-down network can be replaced with a minimum sized NMOS, since we are interested in the worst case, and the currents between the equivalent NMOS and the pull-up PMOS ($M_K$) can be equated. Using the equations for the region of operation the transistors are in and plugging in the corresponding voltages allows to solve for $W_K$ / $L_K$.

Case A: Vout <= $V_{Tn}$

NMOS: Linear Region / Velocity Saturation
PMOS: Velocity Saturation

$$\boxed{\begin{aligned}&k_n'\frac{W_n}{L_n}\left[(V_{DD}-V_{Tn})\times V_{Tn}-\frac{V_{Tn}^2}{2}\right]\times(1+\lambda\times V_{Tn})\\&=k_p'\frac{W_p}{L_p}\left[(V_{DD}-V_{Tp})\times V_{satp}-\frac{V_{satp}^2}{2}\right]\times(1+\lambda\times(V_{DD}-V_{Tn}))\end{aligned}}$$

$\underline{W_p/L_p = 1.19}$

Case B: Vout <= $V_{Minverter} = 0.65$ V

NMOS: Velocity Saturation
PMOS: Linear Region

$$\boxed{\begin{aligned}&k_n'\frac{W_n}{L_n}\left[(V_{DD}-V_{Tn})\times V_{satn}-\frac{V_{satn}^2}{2}\right]\times(1+\lambda\times V_{Minverter})\\&=k_p'\frac{W_p}{L_p}\left[(V_{DD}-V_{Tp})\times(V_{DD}-V_{Minverter})-\frac{(V_{DD}-V_{Minverter})^2}{2}\right]\times(1+\lambda\times(V_{DD}-V_{Minverter}))\end{aligned}}$$

$\underline{W_p/L_p = 1.63}$