Running Cadence

Once the Cadence environment has been setup you can start working with Cadence. You can run cadence from your directory by typing

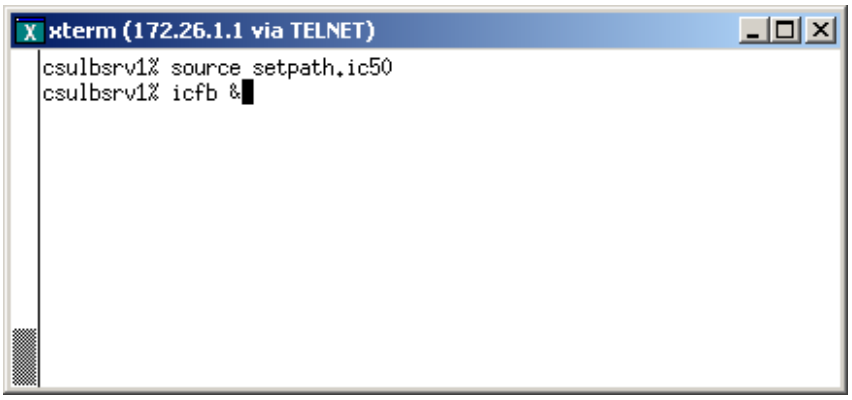


Figure 1.

Main window (Common Interface Window), CIW opens and from the pull down menus you can start your design.

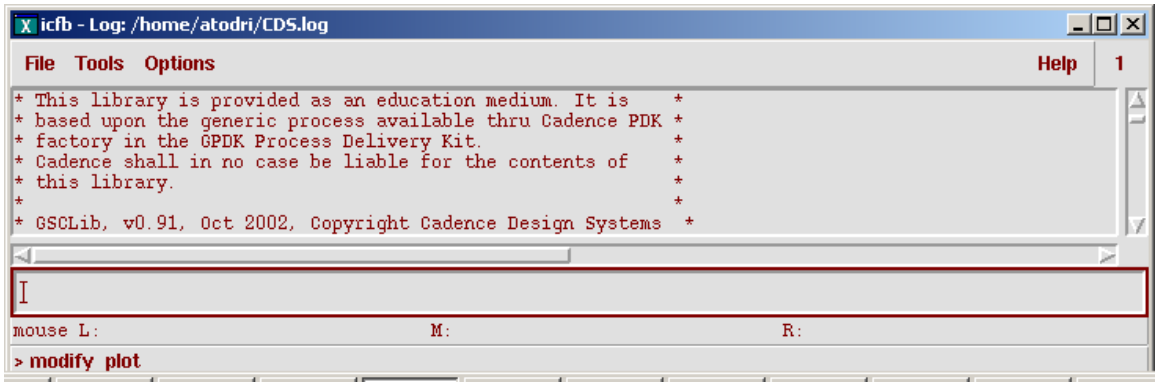


Figure 2.

To create your own library, select from File-> New -> Library, the pop-up window shows up as shown in the Figure 3.

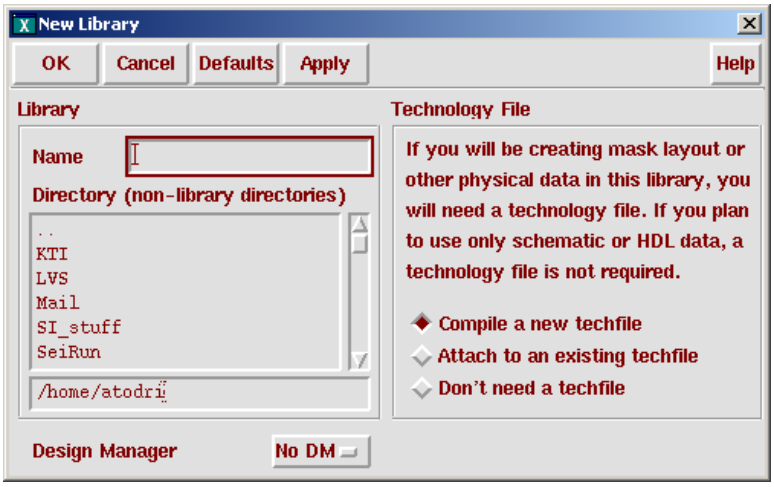


Figure 3.

In the Name section write the name of library. You need add a technology file to your new library. You can attached or compile a tech file to the library. In this case you will attach an existing tech. file. You can attach the technology file from the "gpdk" library as shown in the Figure 4.

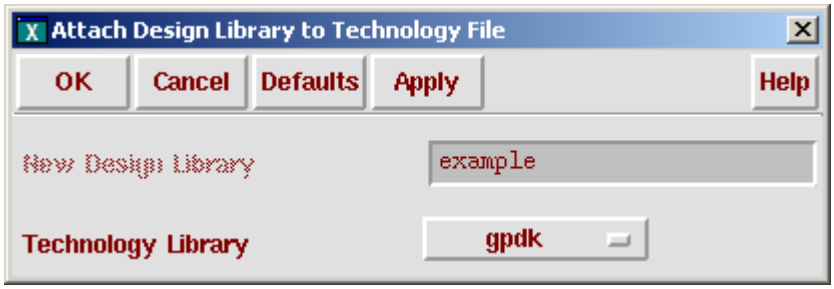


Figure 4.

After creating the working library, you can start creating various views to simulate your design.

I-V Characteristics of Diode

First we start by creating the new cell view for the diode. From File-> New -> Cellview

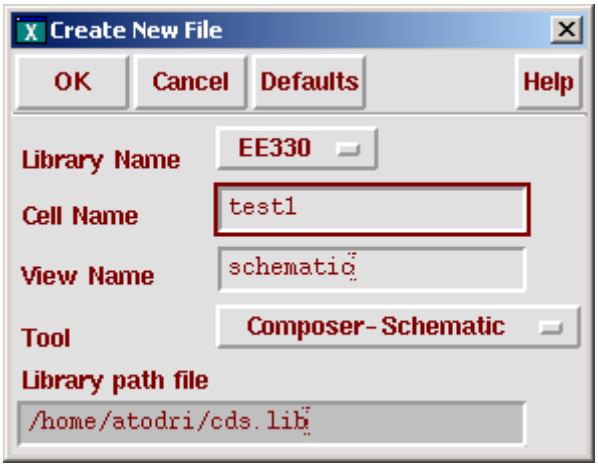


Figure 5.

This creates the schematic view as shown in the Figure 5. You will be using a voltage supply, resistor, and a diode to create the schematic view as shown in the Figure 6.

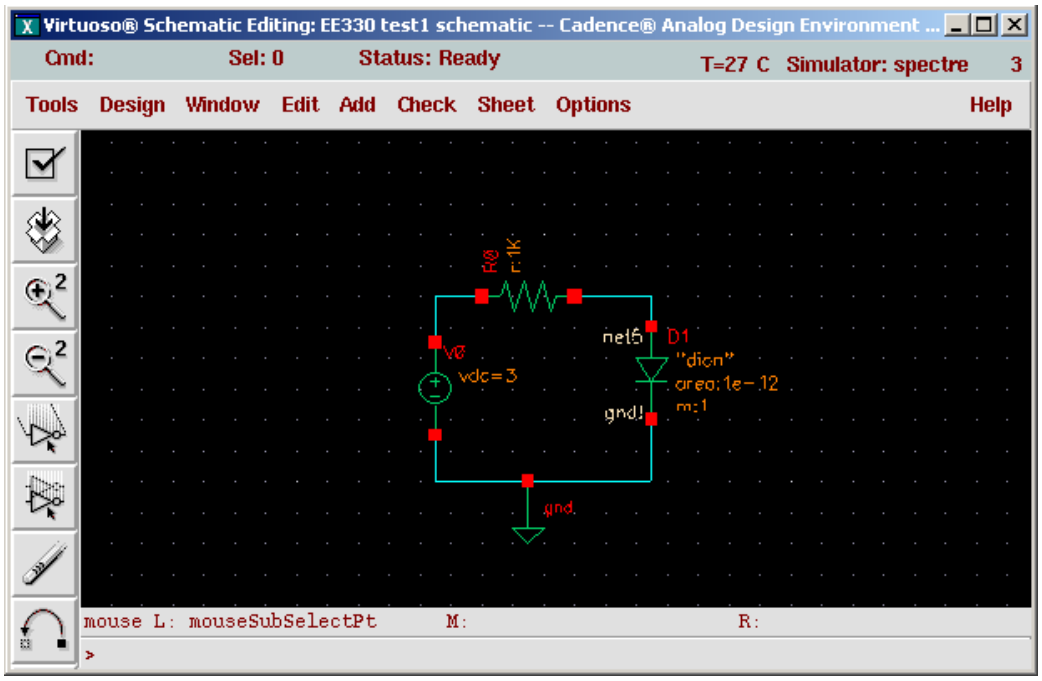


Figure 6.

To add any of the components in the schematic:

From Add-> Instance ->

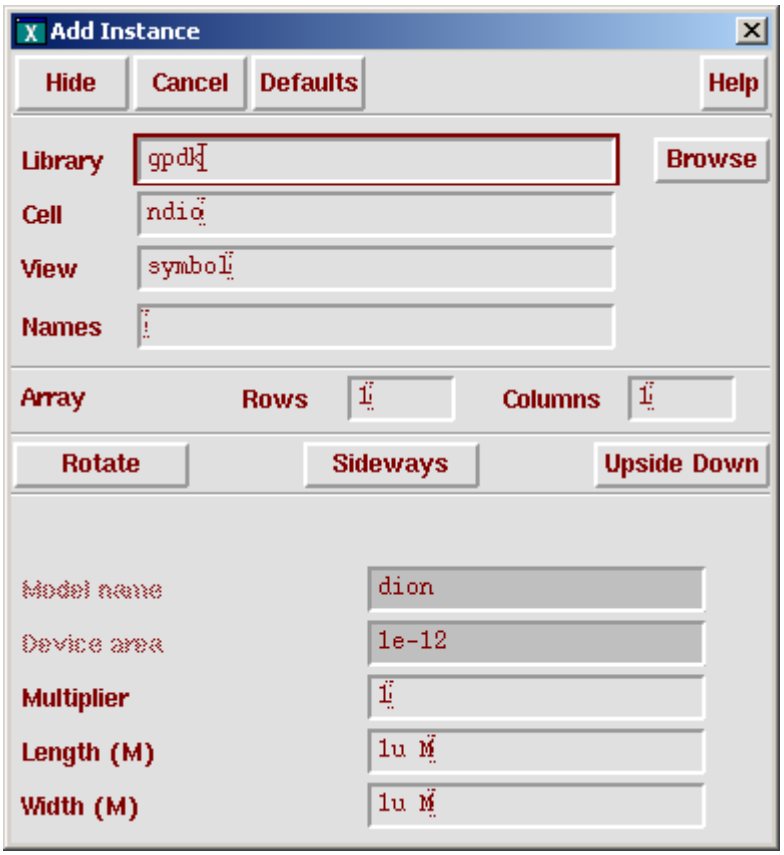


Figure 7.

Select the diode, voltage supply, resistance and ground as shown in the Figures 7, 8, 9 and 10.

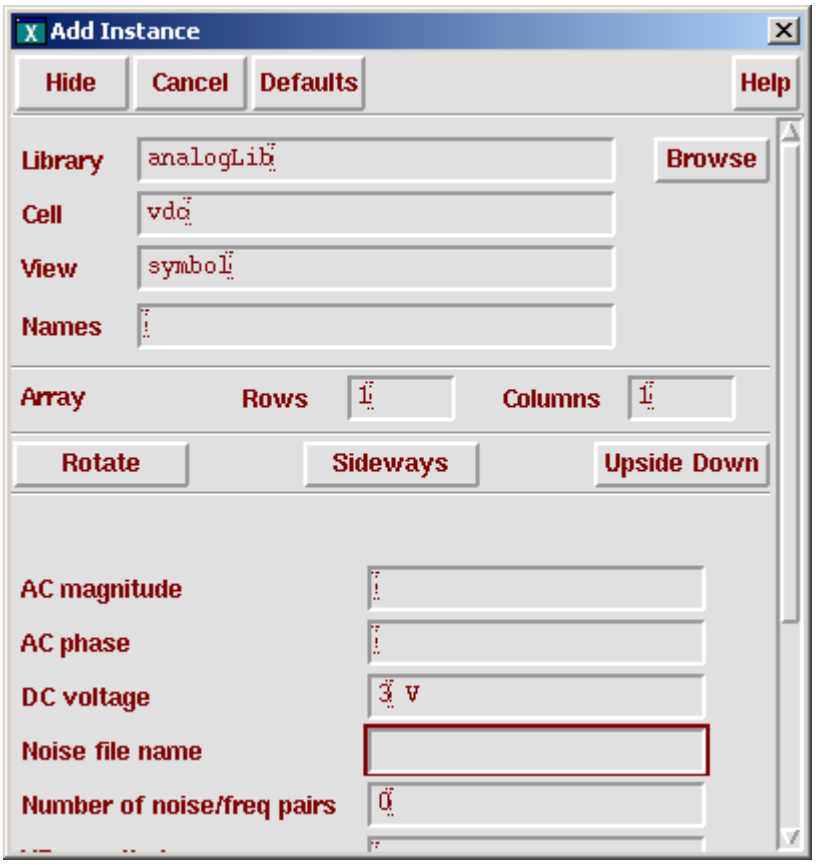

Add Instance
Hide
Cancel
Defaults
Help
Library
analogLib
Browse
Cell
vdc
View
symbol
Names
Array
Rows
1
Columns
1
Rotate
Sideways
Upside Down
AC magnitude
AC phase
DC voltage
3 V
Noise file name
Number of noise/freq pairs
0

Figure 8.

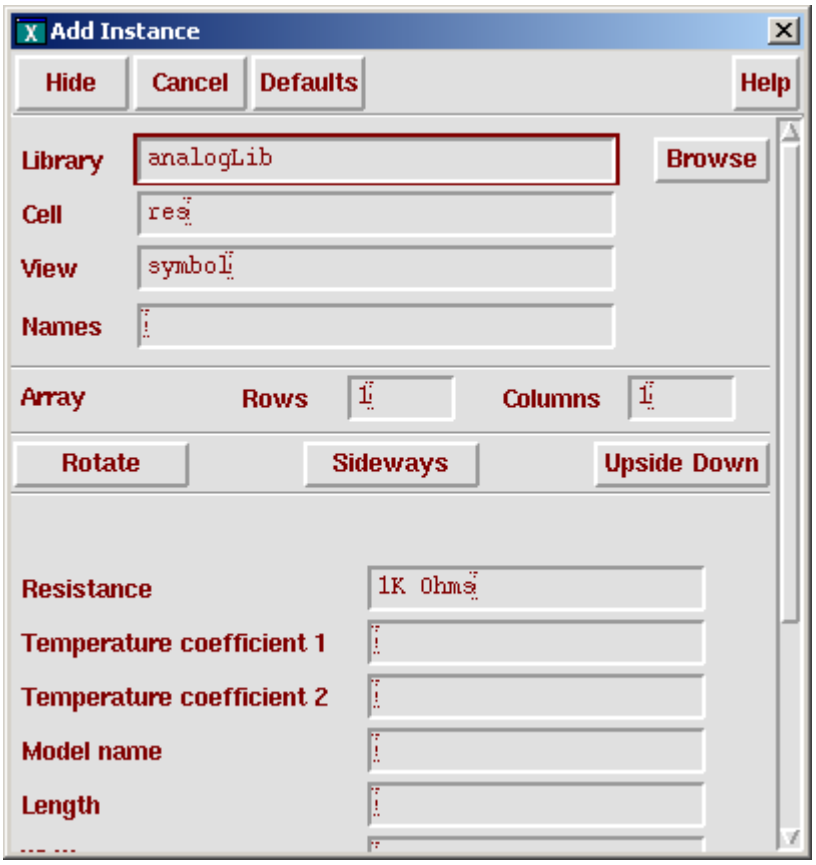


Figure 9.

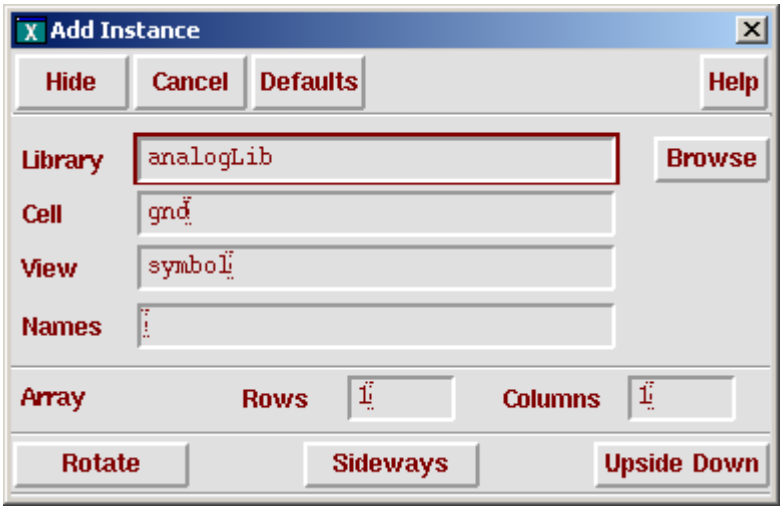


Figure 10.

Place the components as shown in the Figure 6. At this point you are ready to start the simulation.

From Tools-> Analog Environment

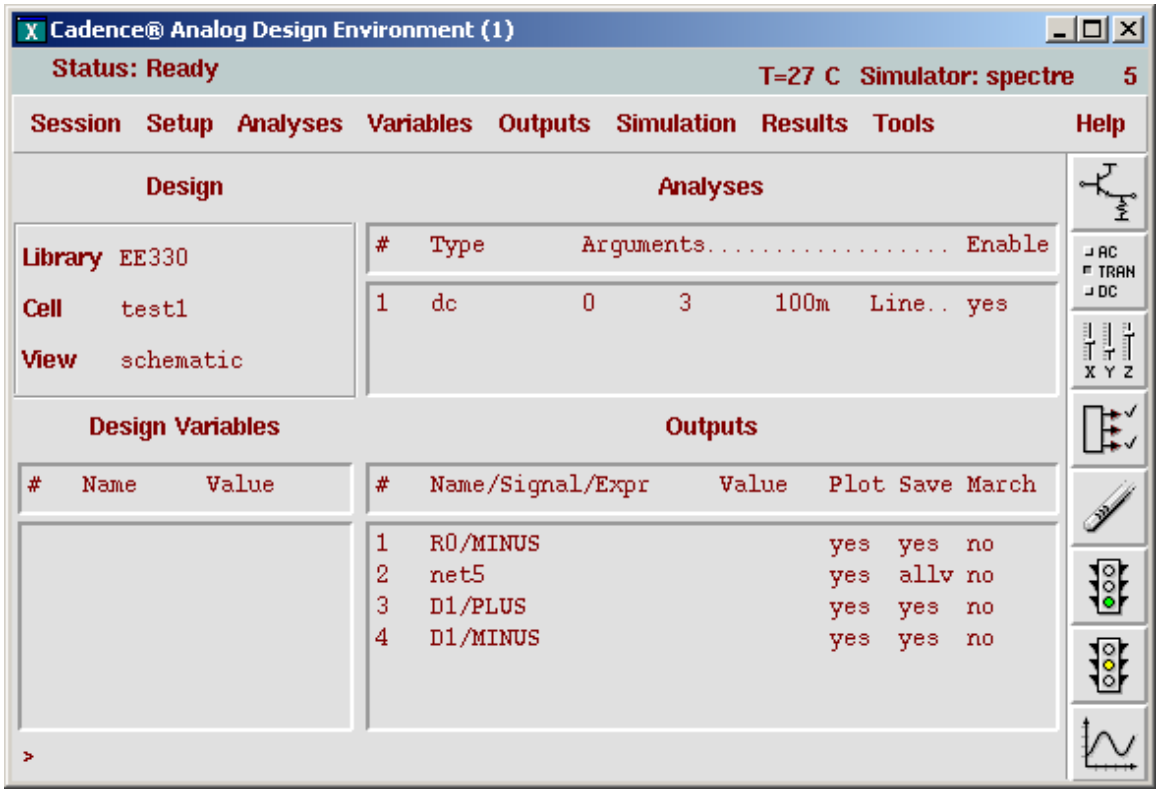


Figure 11.

Write the path for the model libraries

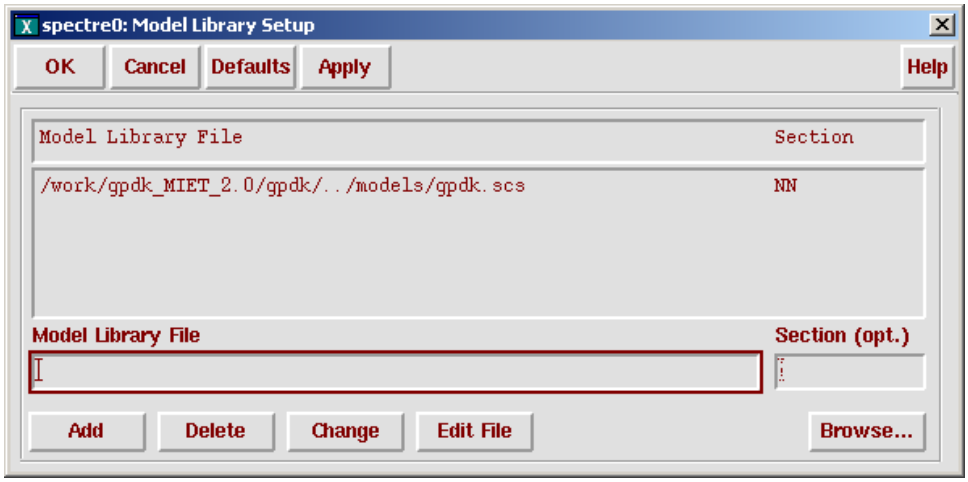


Figure 12.

Choose dc type of analysis from Analysis -> Choose

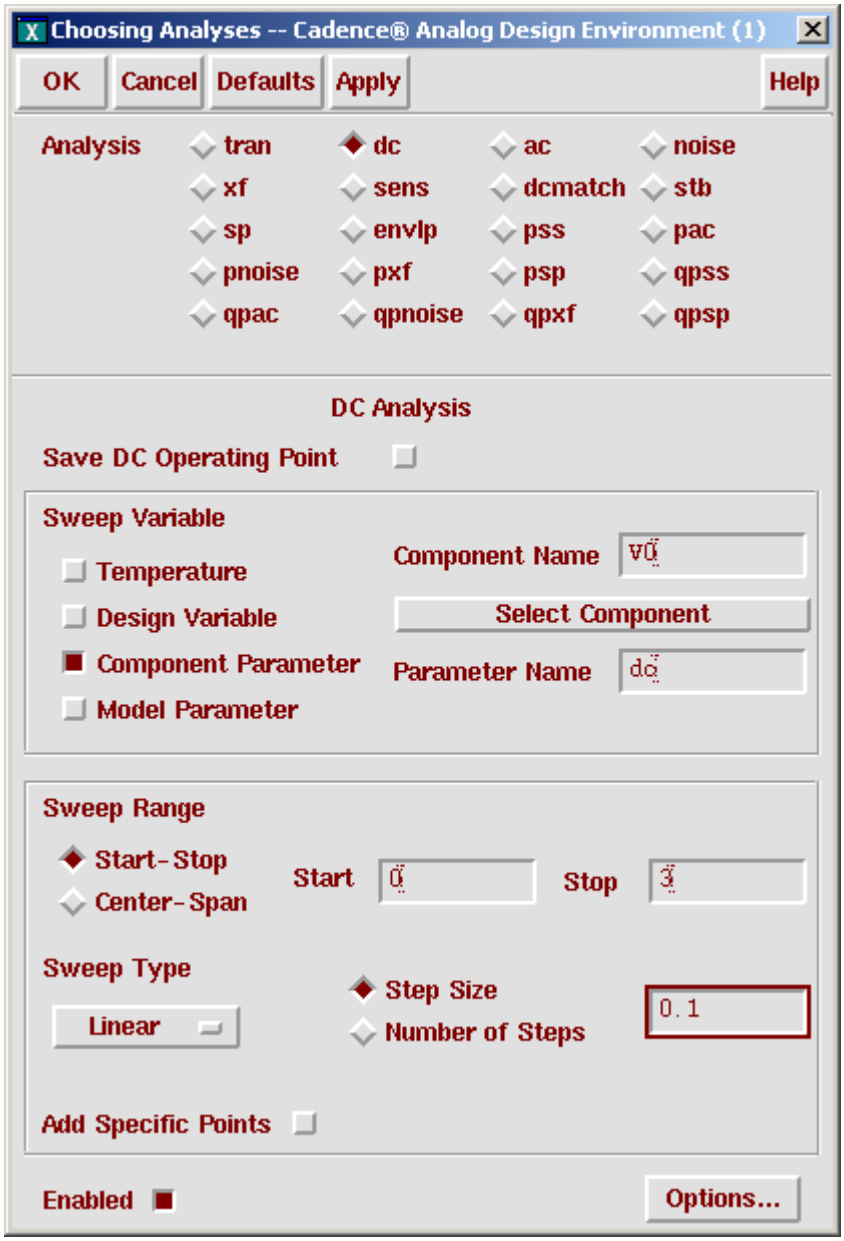


Figure 13.

Variables to be plotted are selected from the schematic

Figure 14.

To plot voltages select the wire, and to plot current select the red square nodes or select on the component. Figure 15 shows how the selected voltages and current nodes look line after being selected for simulation.

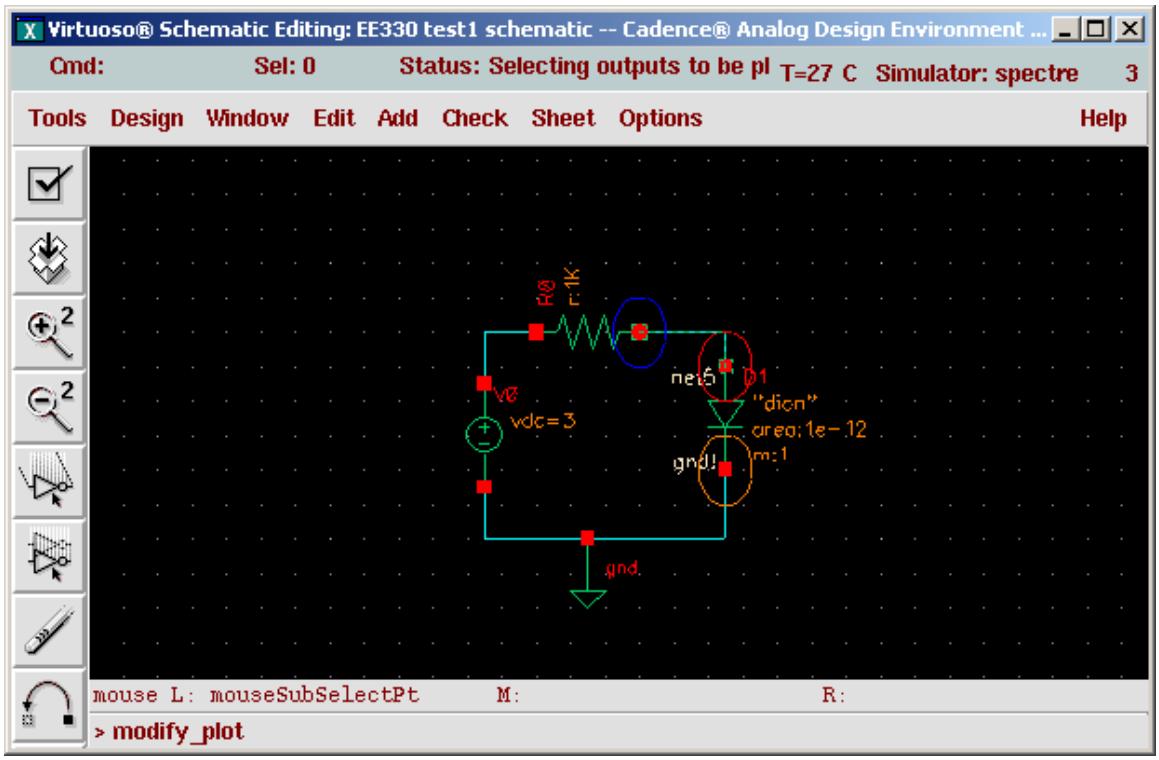


Figure 15.

Now we are ready to perform simulation. After clicking on Simulation-> Netlist and Run simulation starts.
Figure 16, shows the spectre output log file that gets generated for simulation.

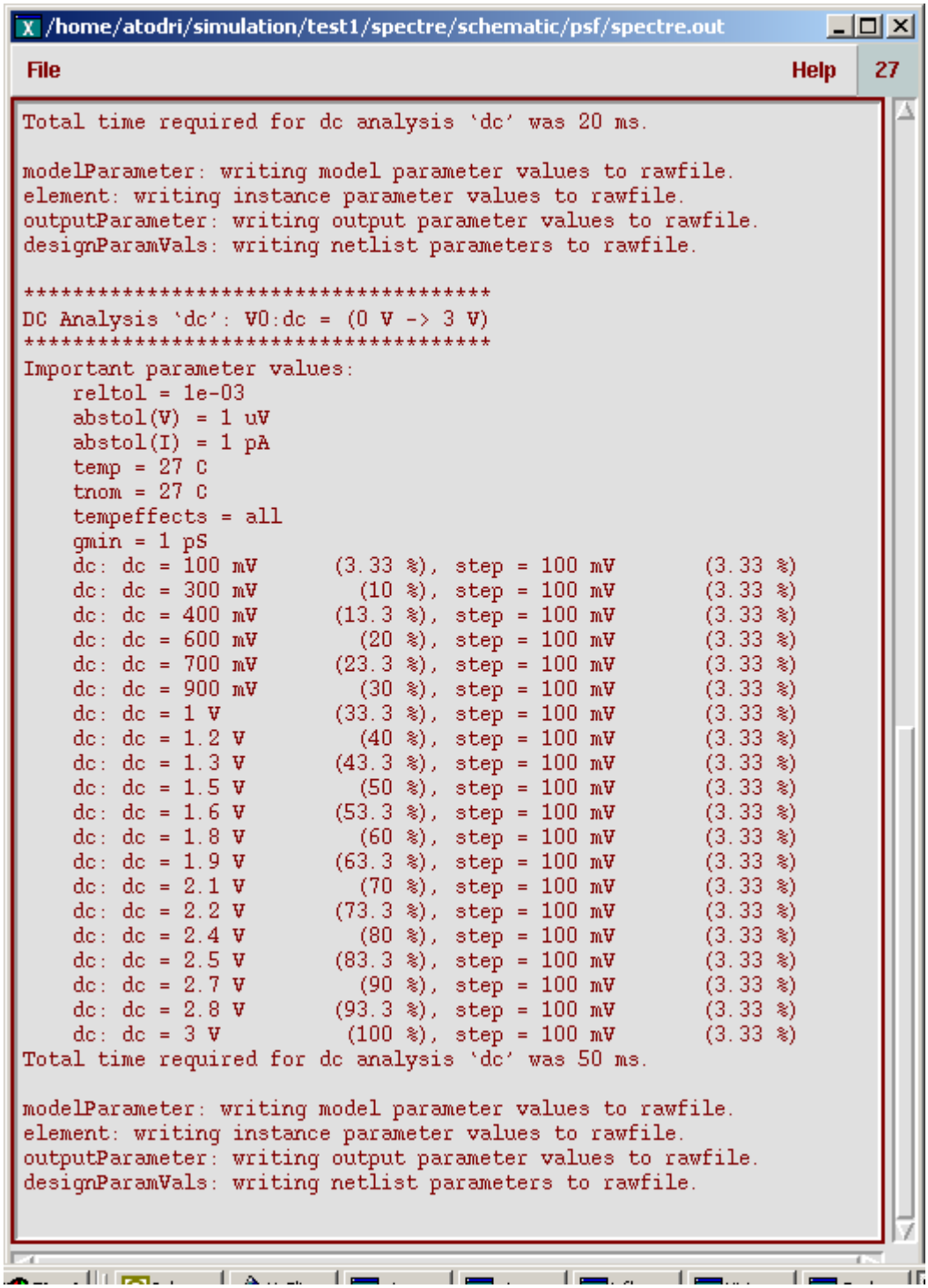


Figure 16.

The waveform created looks like :

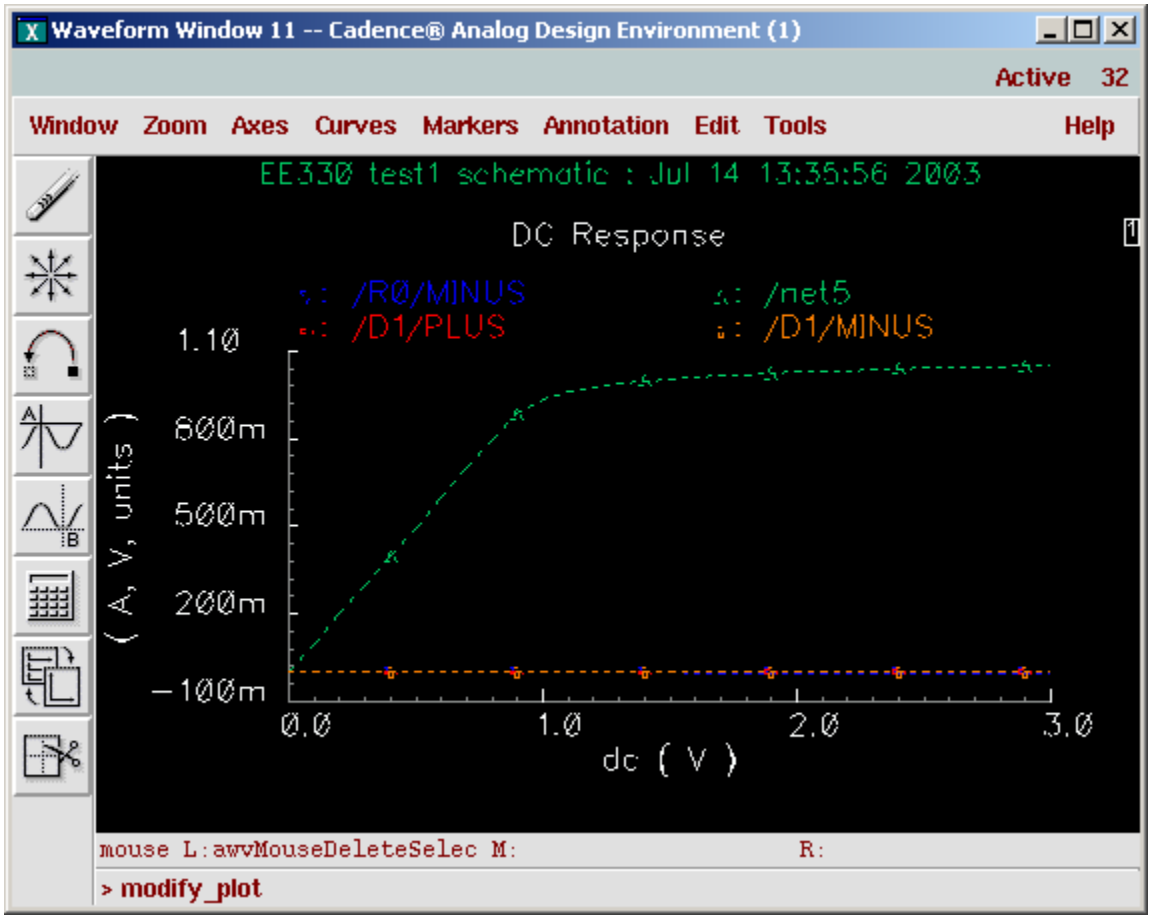


Figure 17

To display Current (I) versus Voltage (V) we start by setting the axis.
From Axis-> X Axis

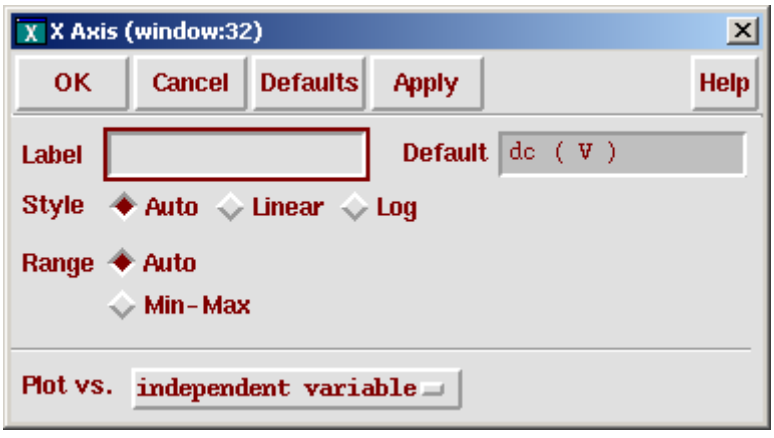


Figure 18.

Change the X axis to be the voltage drop on the diode or /net5 voltage as shown in the Figure 19.

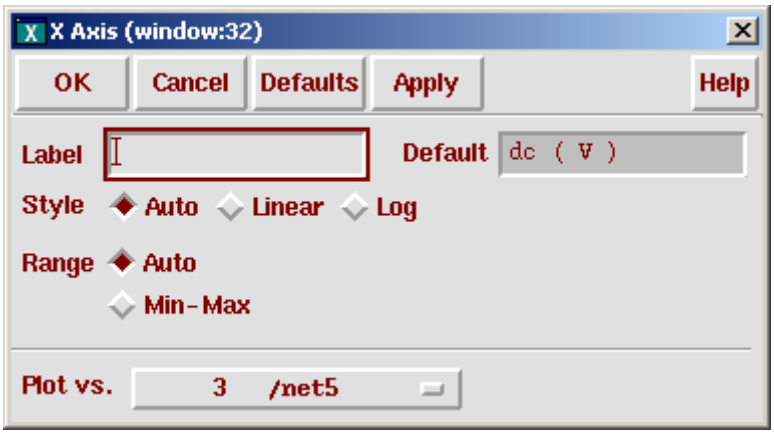


Figure 19.

After changing the X axis, the waveform looks like, as shown in Figure 20:

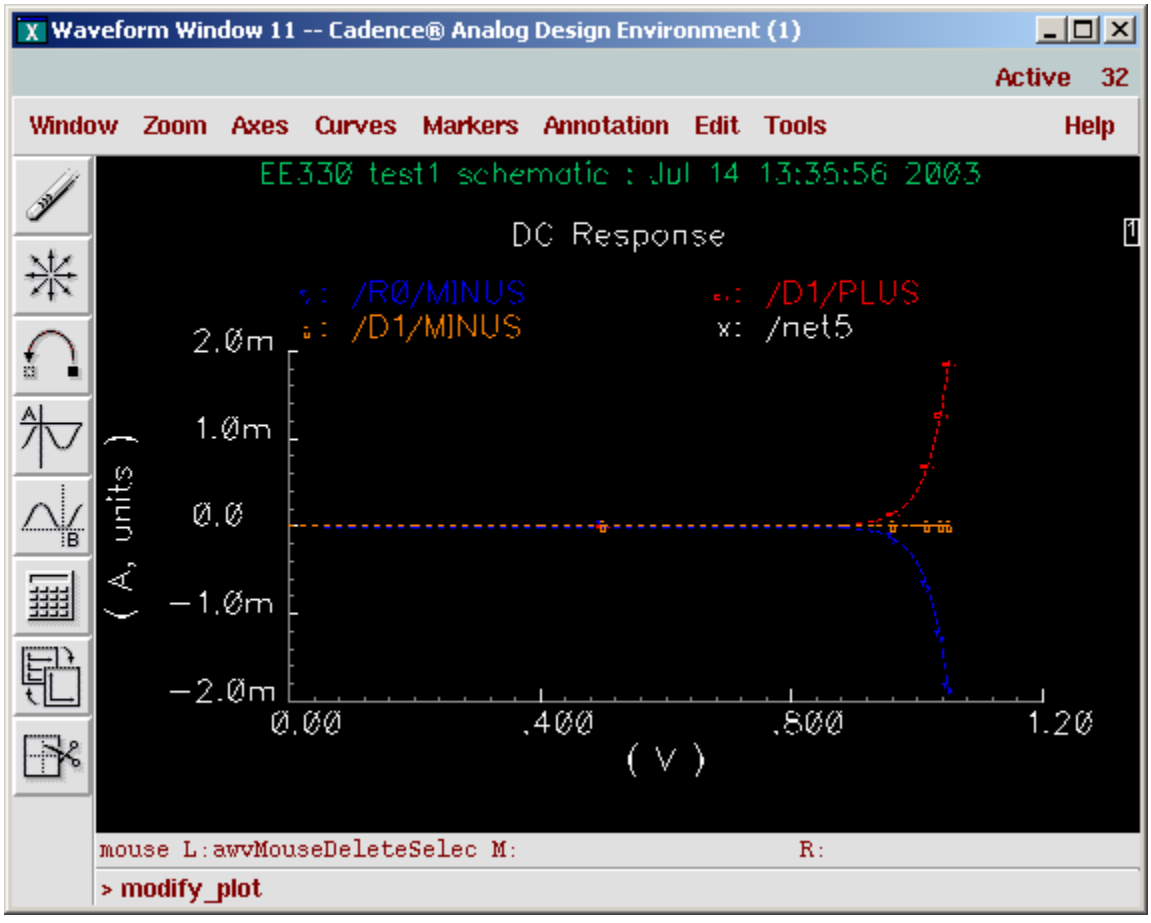


Figure 20.

Because we are interested only on the I-V plot for the current and voltage of the diode, we can select only the D1/PLUS current node and /net5 voltage drop of the diode. The new waveform will look like shown in Figure 21.

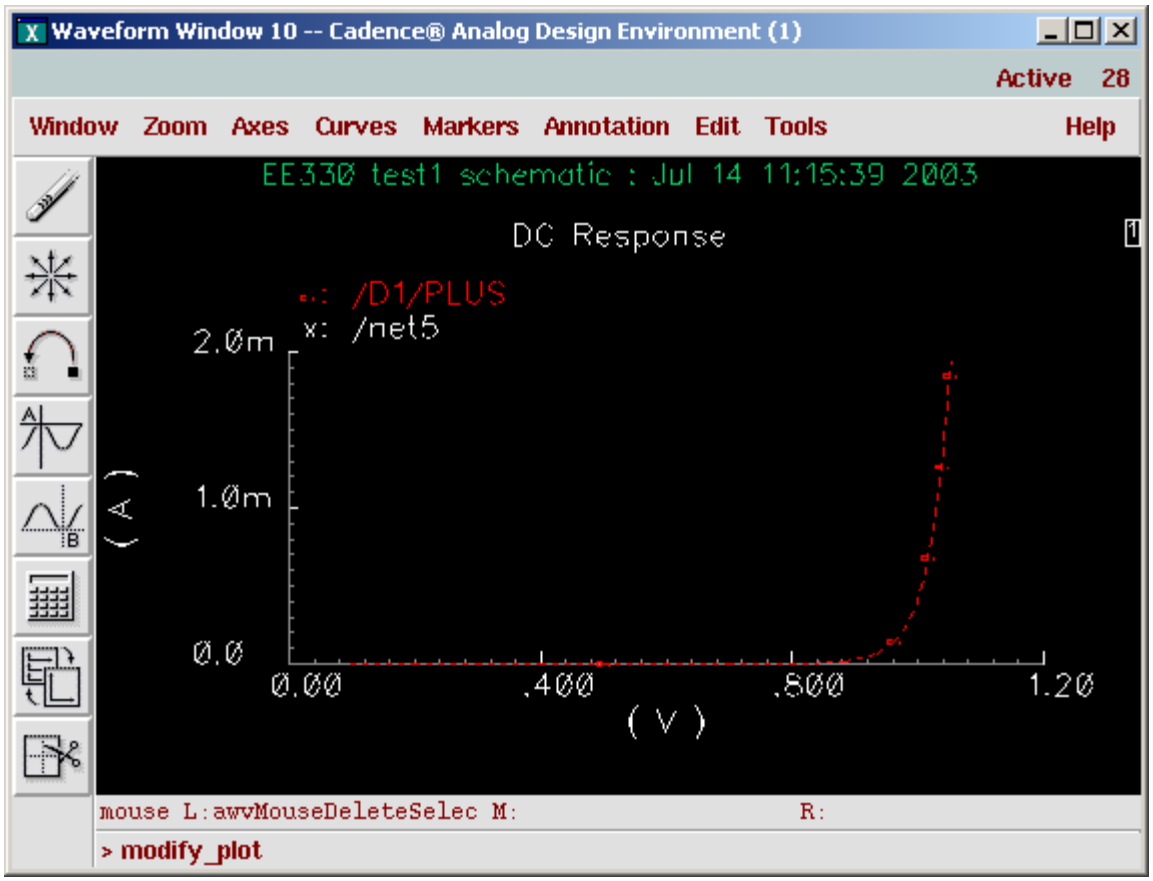


Figure 21.

I-V Characteristics of BJT

Initially start a new schematic cellview for the bjt circuit. Figure 22, displays the circuit used for simulation. After adding all the necessary components, connect them together and the last part is editing the variables.

The power supply “vdc” is identified with a variable voltage “VBB”. You can do this by editing the properties of the power supply.

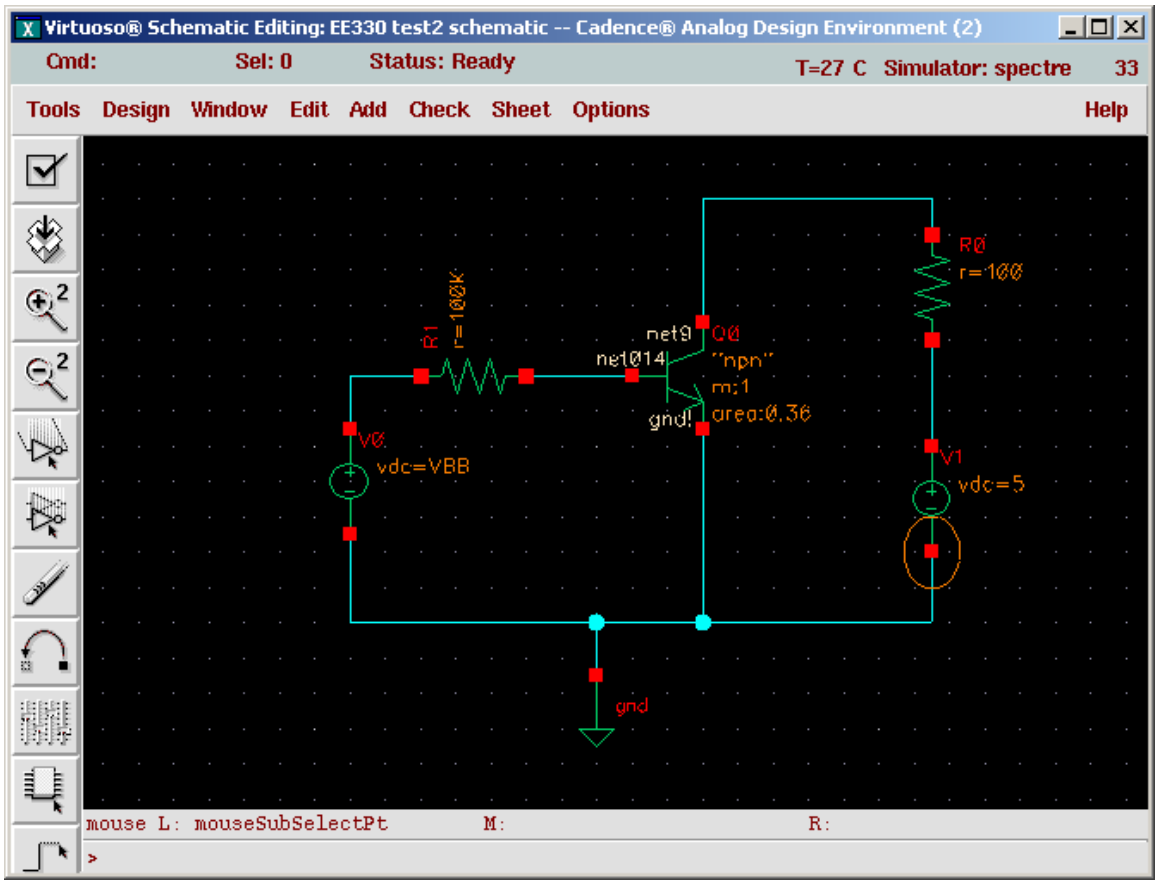


Figure 22.

After compltng the schematic, we are ready to start simulation.

From Tools -> Analog Enviroment, and the pop-up window as in Figure 23 shows up.

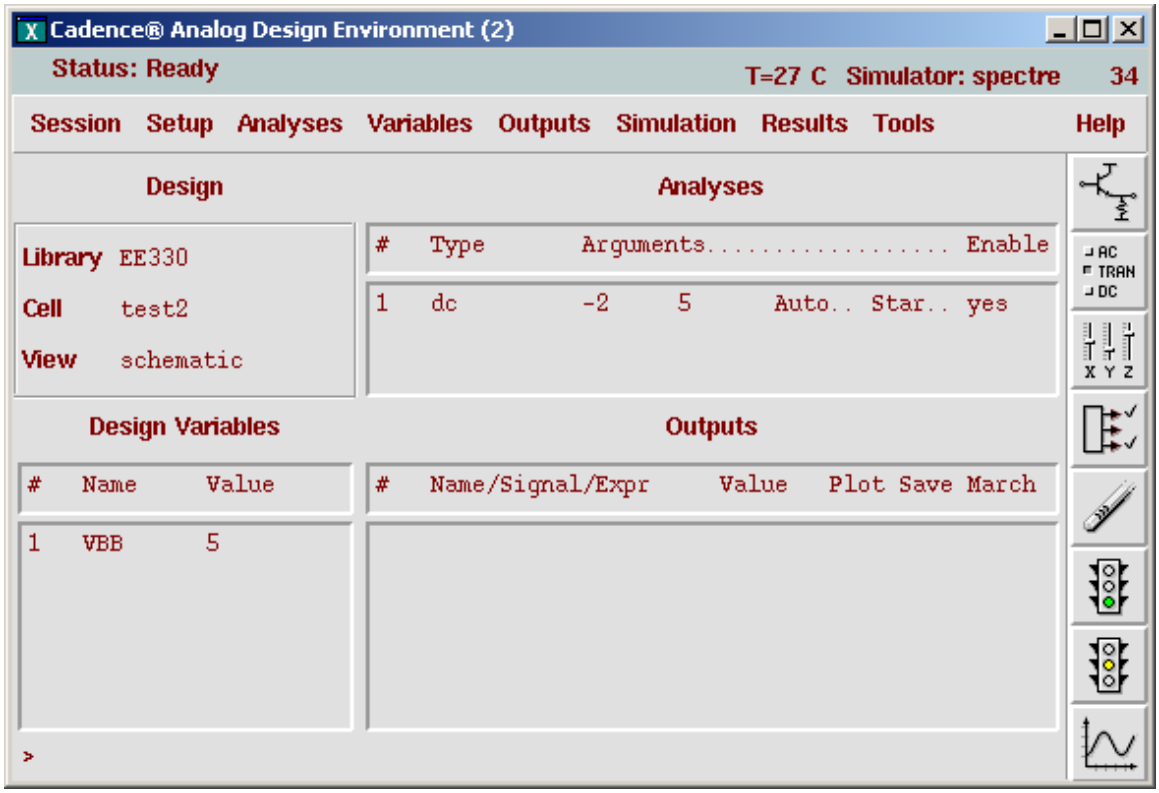


Figure 23.

Setting the Variables

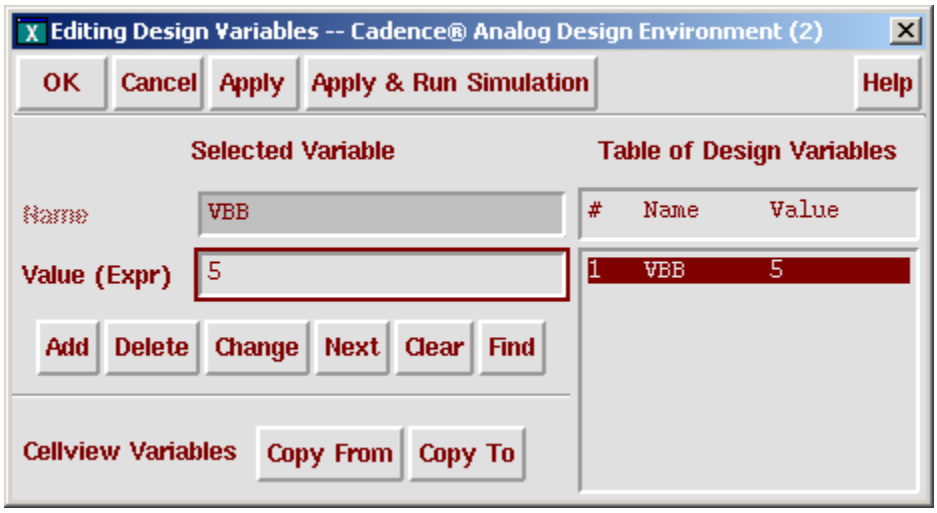


Figure 24.

Setting the type of Analysis

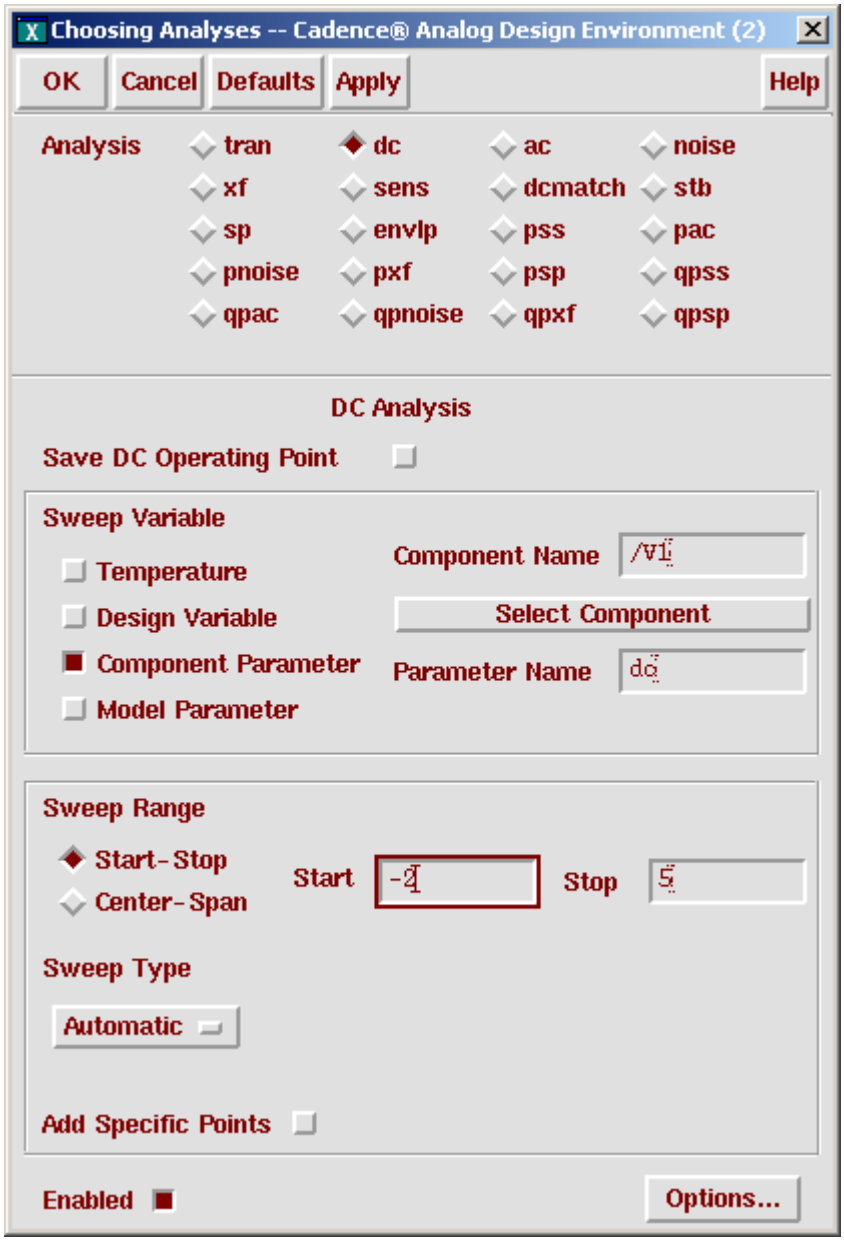


Figure 25.

After completing these steps you can start simulation by clicking on Simulation-> Netlist and Run.
At this point you can see the spectre output log file that is created.
After this point you will perform parametric analysis as shown in Figure 26, to view multiple curves in a single waveform.

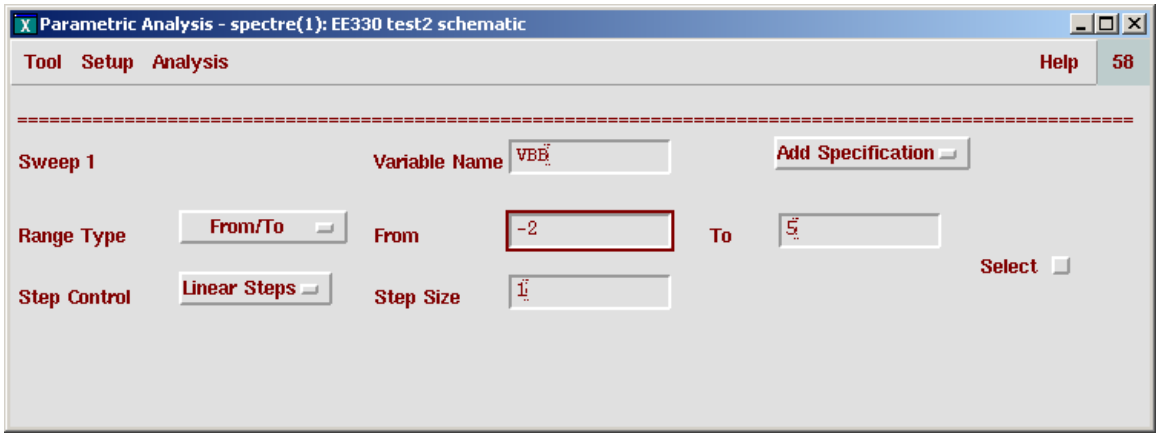


Figure 26.

Go to Analysis -> Start in the Parametric Analysis window. When the simulation is complete go to Results -> Direct Plot -> DC and then click on the terminal of the V1 supply, then hit ESC. Now you should again get a nice family of IV curves as shown in Figure 27.

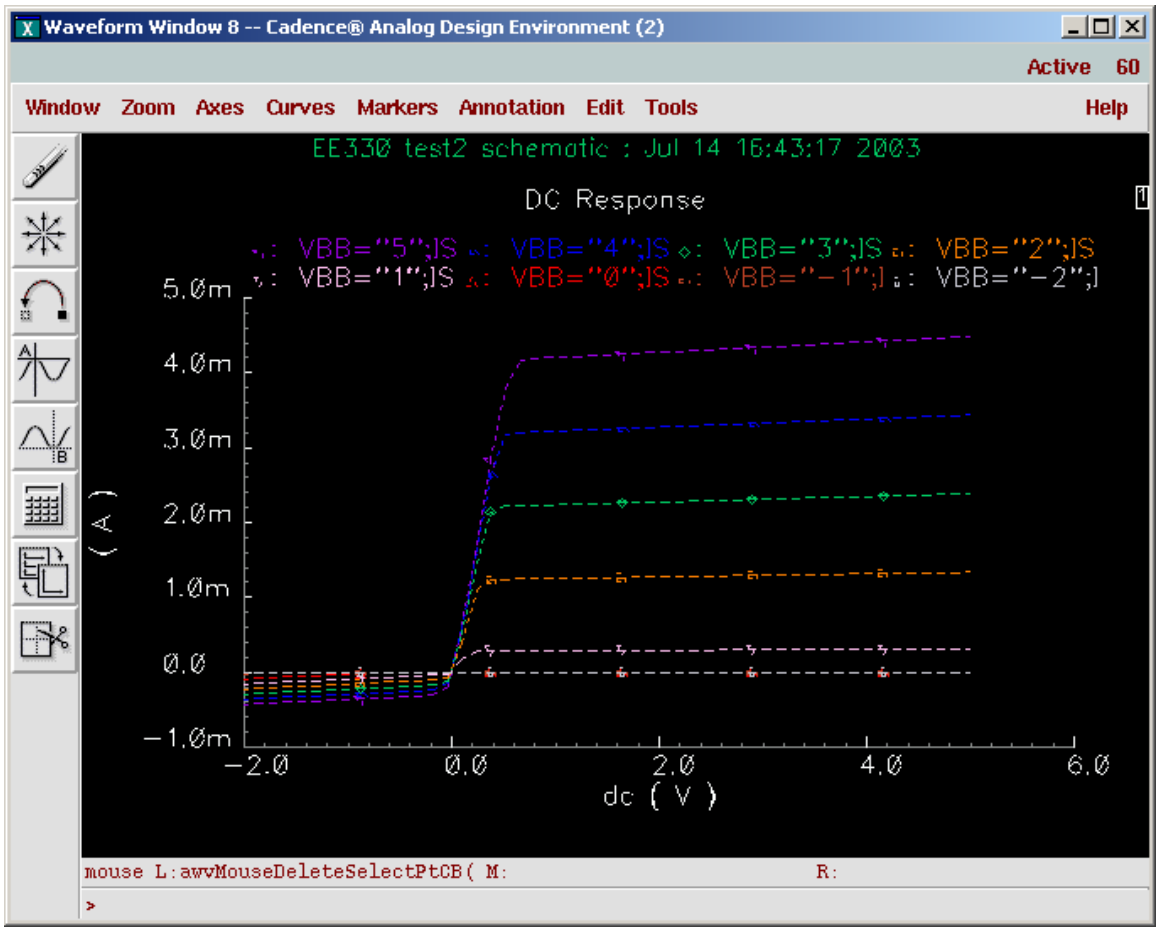


Figure 27.

Generating C-V Plots for MOS Capacitor Device

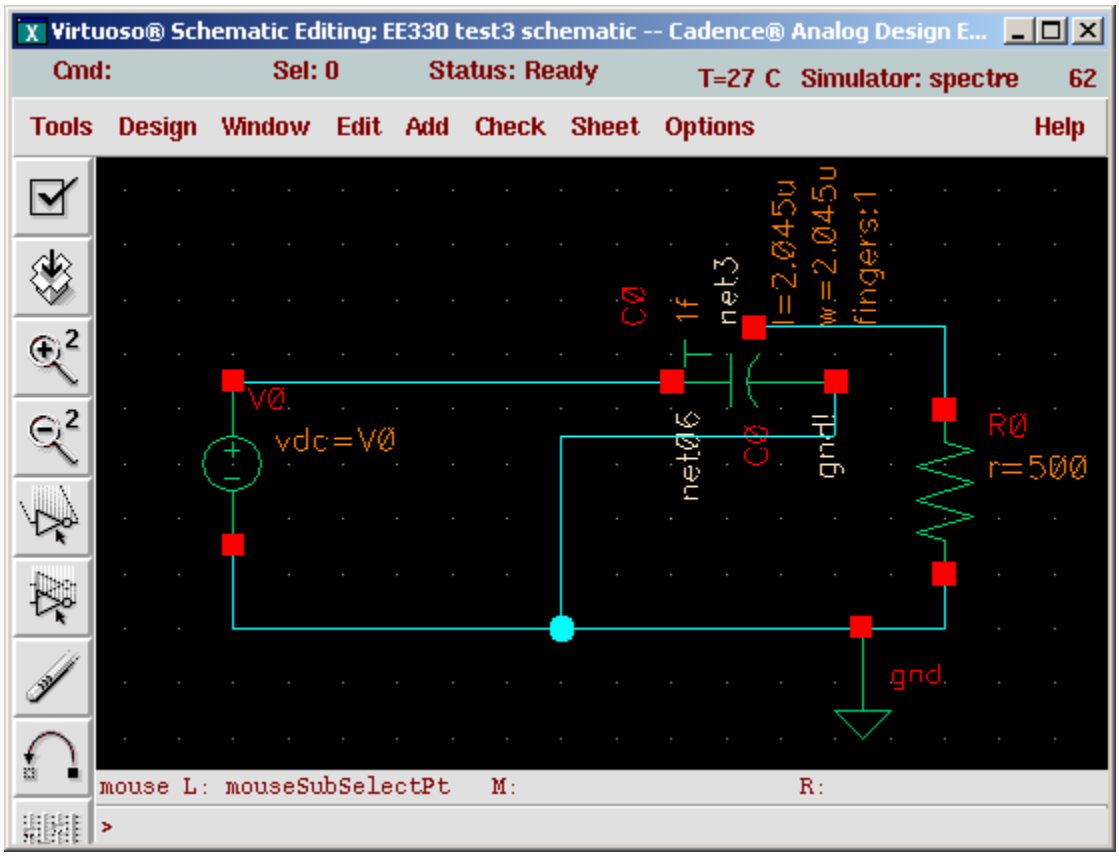


Figure 28.

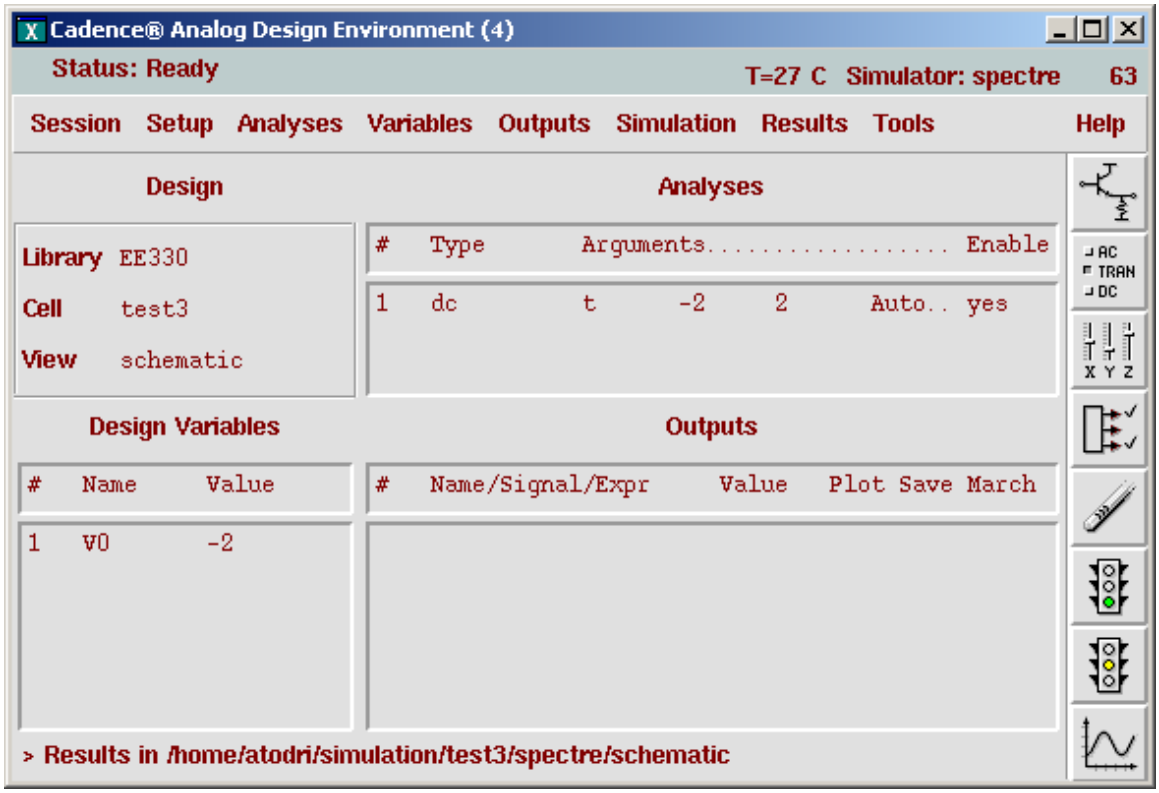

Cadence® Analog Design Environment (4)
Status: Ready
T=27 C Simulator: spectre 63
Session Setup Analyses Variables Outputs Simulation Results Tools Help
Design
Library EE330
Cell test3
View schematic
Analyses
Type Arguments Enable
1 dc t -2 2 Auto.. yes
AC
TRAN
DC
X Y Z
Design Variables
Name Value
1 V0 -2
Outputs
Name/Signal/Expr Value Plot Save March
> Results in /home/atodri/simulation/test3/spectre/schematic

Figure 29.

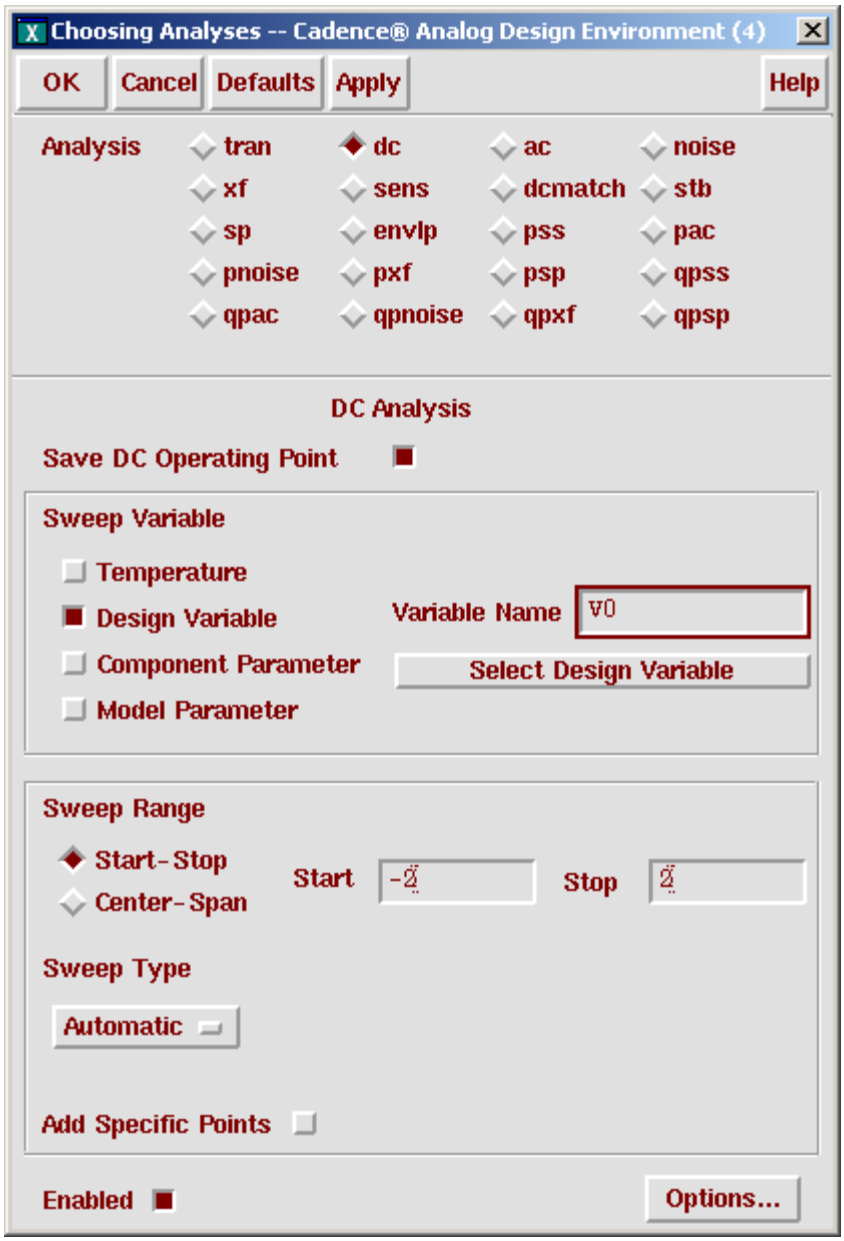

Choosing Analyses -- Cadence® Analog Design Environment (4)
OK
Cancel
Defaults
Apply
Help
Analysis
tran
dc
ac
noise
xf
sens
dcmatch
stb
sp
envlp
pss
pac
pnoise
pxf
psp
qpss
qpac
qpnoise
qpxf
qpsp
DC Analysis
Save DC Operating Point
Sweep Variable
Temperature
Design Variable
Variable Name
V0
Component Parameter
Select Design Variable
Model Parameter
Sweep Range
Start-Stop
Center-Span
Start
-2
Stop
2
Sweep Type
Automatic
Add Specific Points
Enabled
Options...

Figure 30.

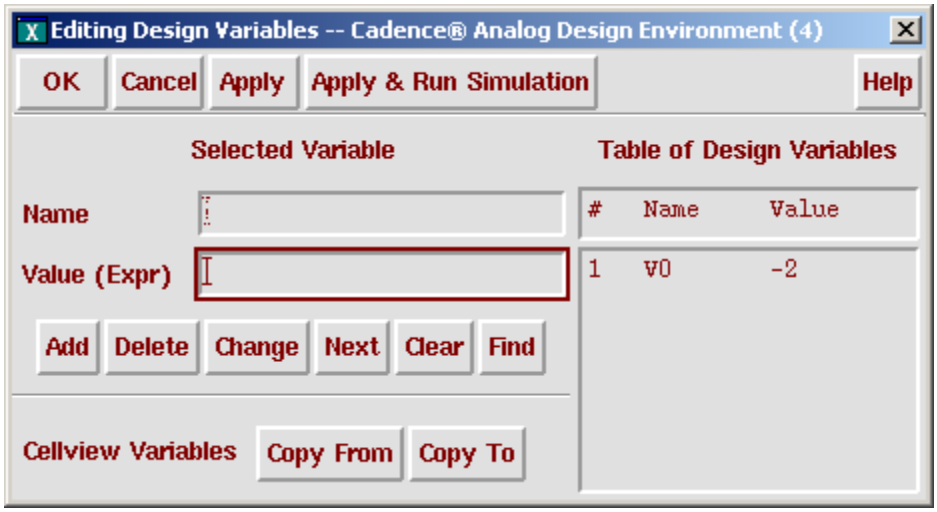


Figure 31

Perform simulation from Simulation -> Netlist and Run

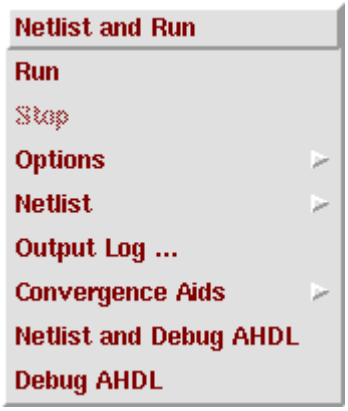


Figure 32

Then perform Parametric Analysis

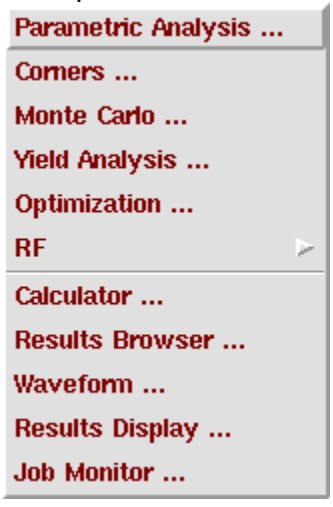


Figure 33

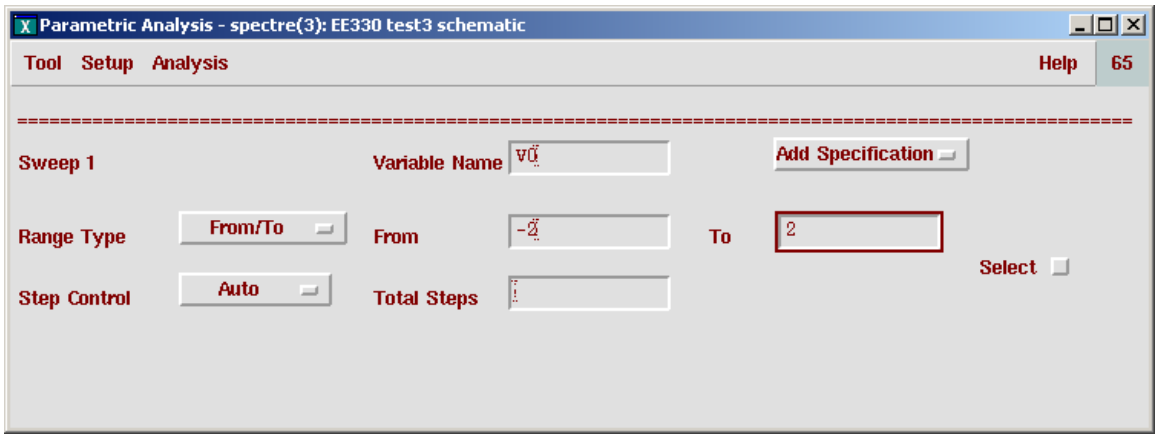


Figure 34

Parametric Analysis Form

Select output to be displayed: From Output -> Setup

Figure 35

The Form will look like:

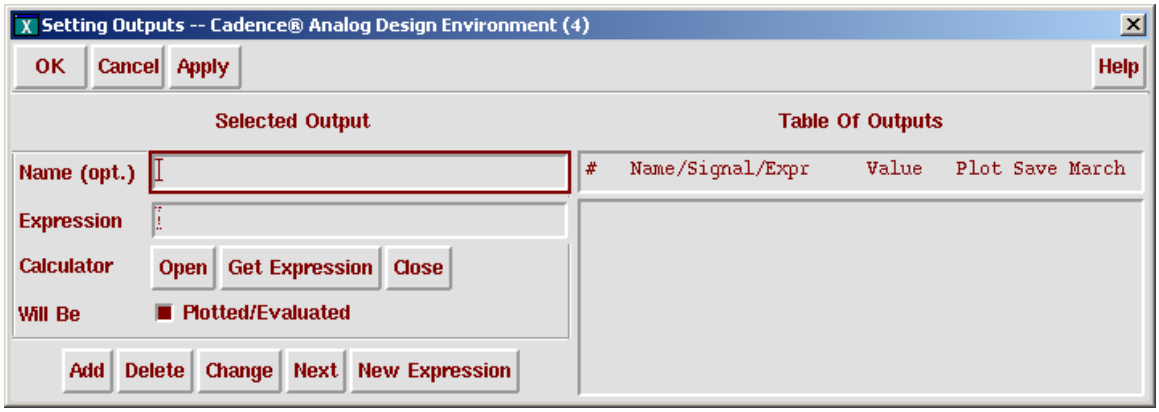


Figure 36

By clicking on “Open” , the Calculator will open

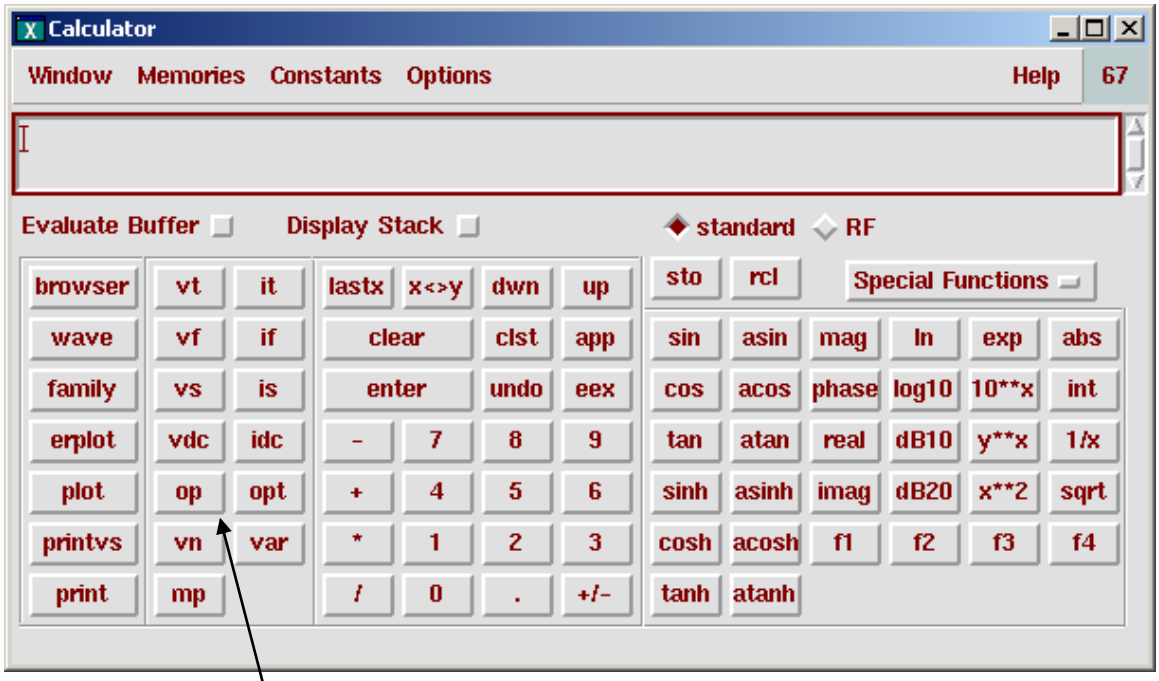


Figure 37

By clicking on “ OP” and then selecting the device from the schematic view, you will see a list of variables

Figure 38


List
cap
cdg
cgb
ids
vgs
vds
vbs
vth
vdsat
gm
gds
gmbs
betaeff
cjd
cjs
cgg
cgd
cgs
gmoverid
cbg
cdd
cds
cdb
csg
csd
css
csb
pwr
cbd
cbs
cbb
ron
id
ibulk

Figure 39

After selecting the variables to be plot, then just click on ERPLOT in the Calculator to plot.

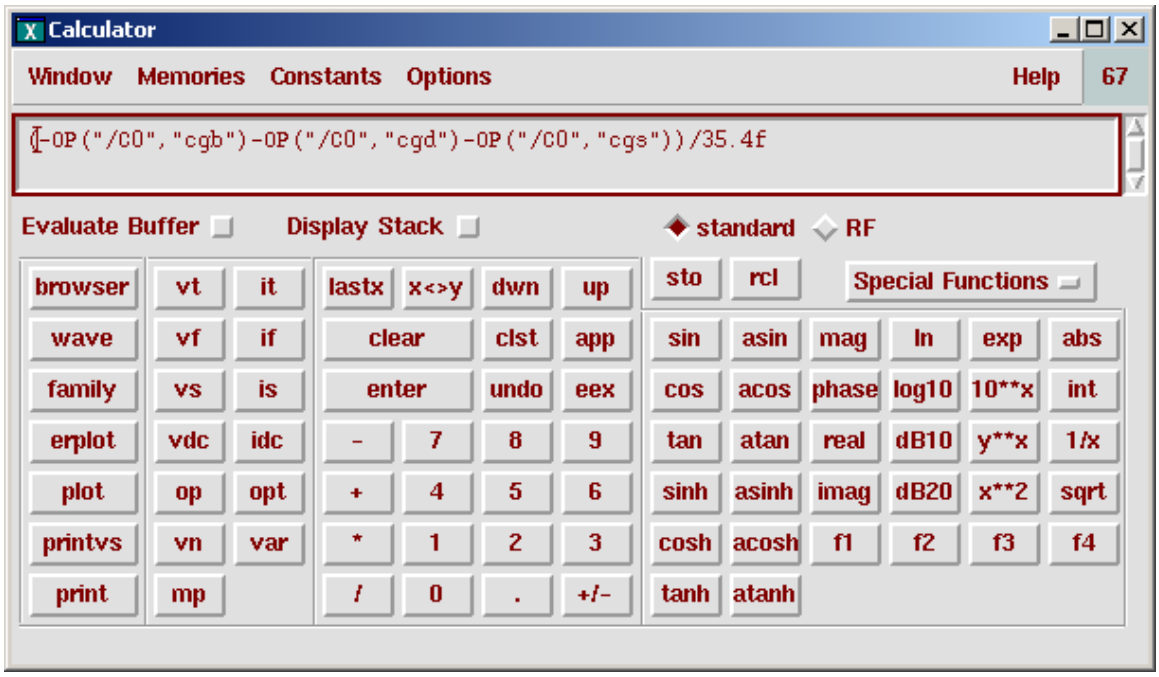


Figure 39

The waveform will look like:

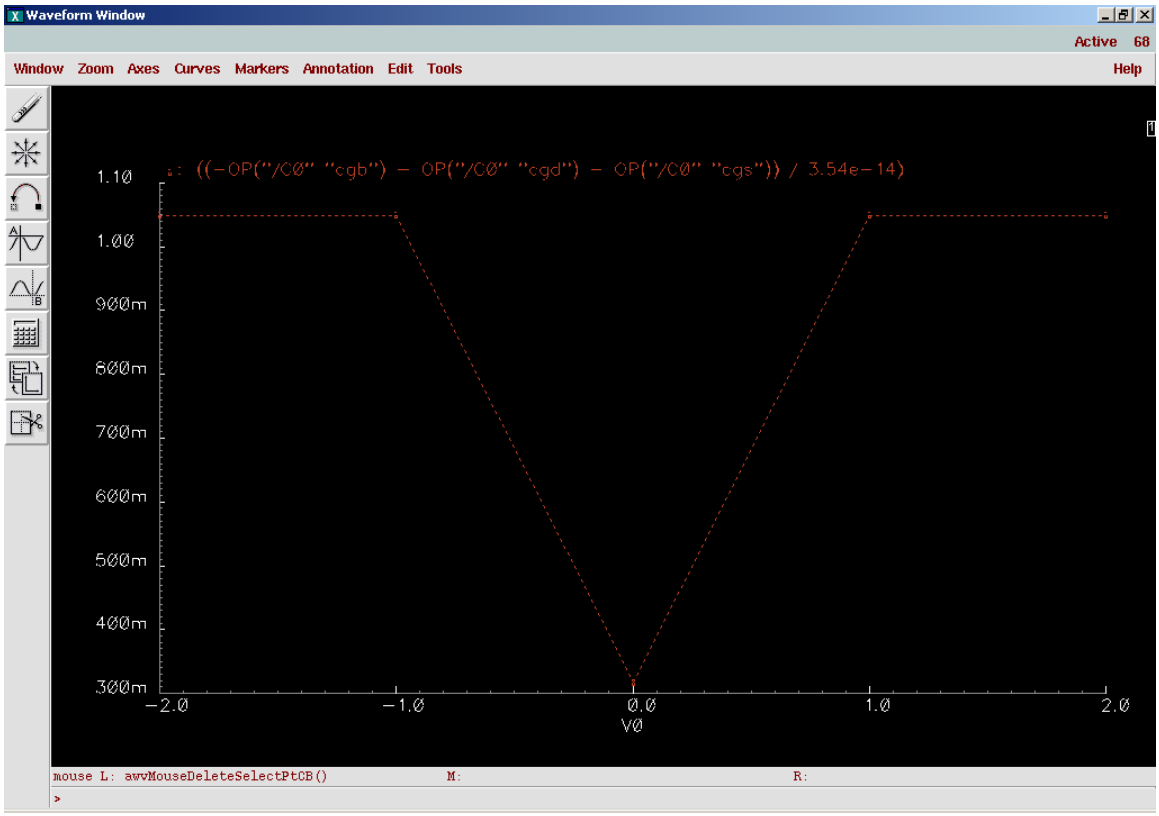

Waveform Window
Active 68
Window Zoom Axes Curves Markers Annotation Edit Tools Help
: ((-OP("/C0" "cgb") - OP("/C0" "cgd") - OP("/C0" "cgs")) / 3.54e-14)
1.10
1.00
900m
800m
700m
600m
500m
400m
300m
-2.0
-1.0
0.0
1.0
2.0
V0
mouse L: awvMouseDeleteSelectPtCB()
M:
R:
>

Figure 40

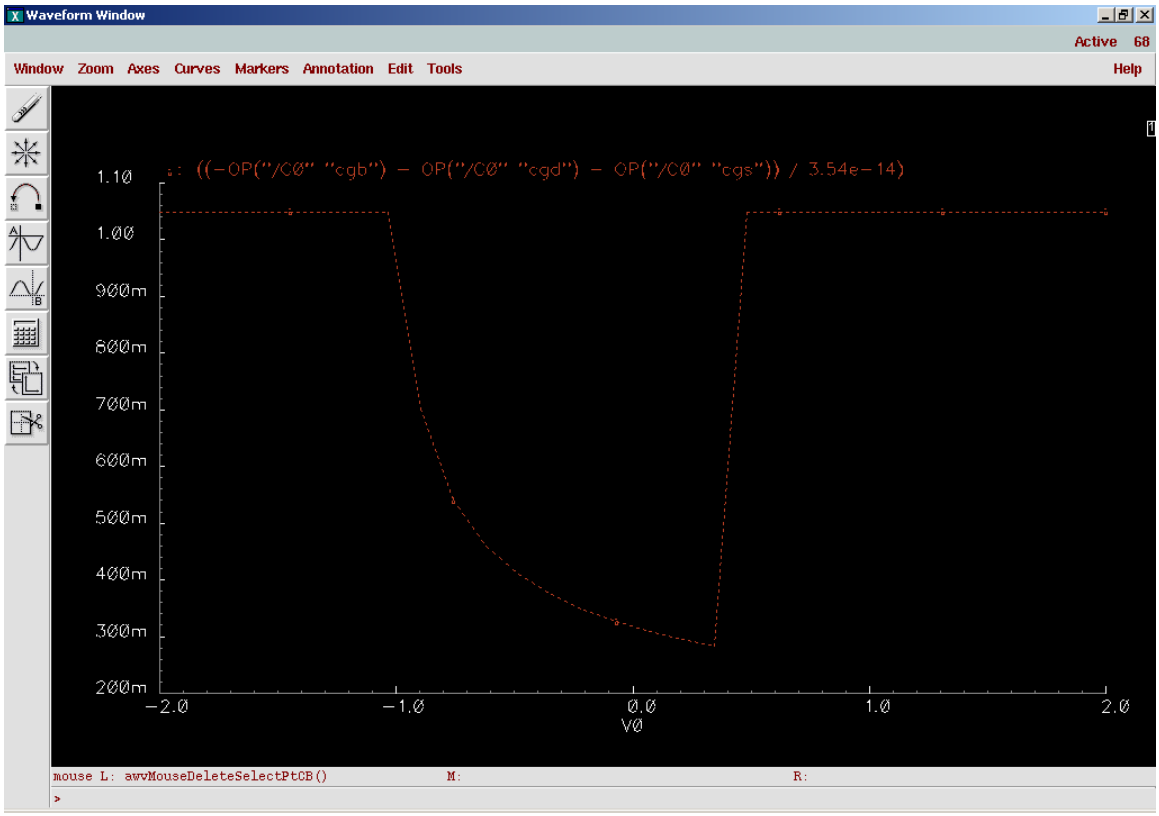

Waveform Window
Active 68
Window Zoom Axes Curves Markers Annotation Edit Tools Help
1: ((-OP("/C0" "cgb") - OP("/C0" "cgd") - OP("/C0" "cgs")) / 3.54e-14)
1.10
1.00
900m
800m
700m
600m
500m
400m
300m
200m
-2.0
-1.0
0.0
1.0
2.0
V0
mouse L: awvMouseDeleteSelectPtCB()
M:
R:

Figure 41

Variation of the Bandgap Reference Voltage with respect to Temperature

The example below is the classical Widlar Bandgap Voltage Reference

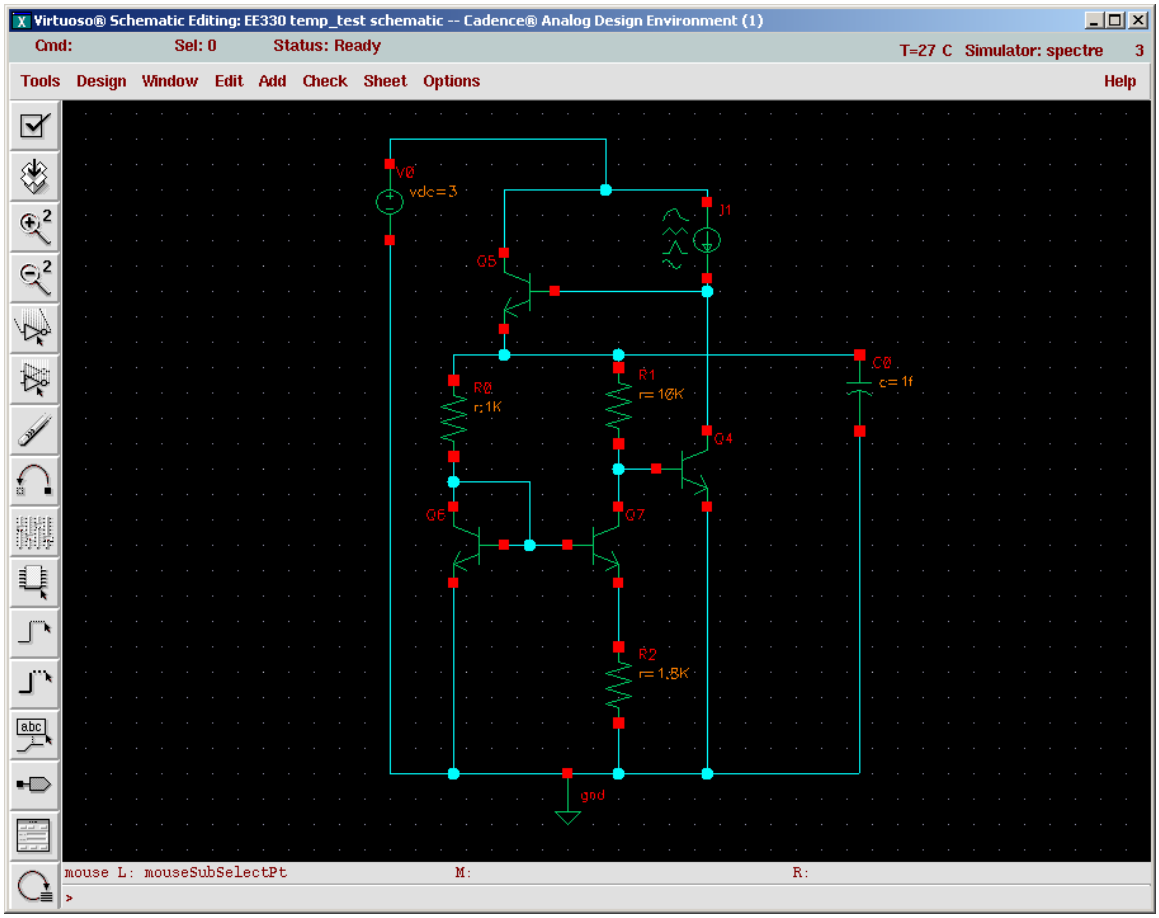


Figure 42

By clicking on Tools -> Analog Environment

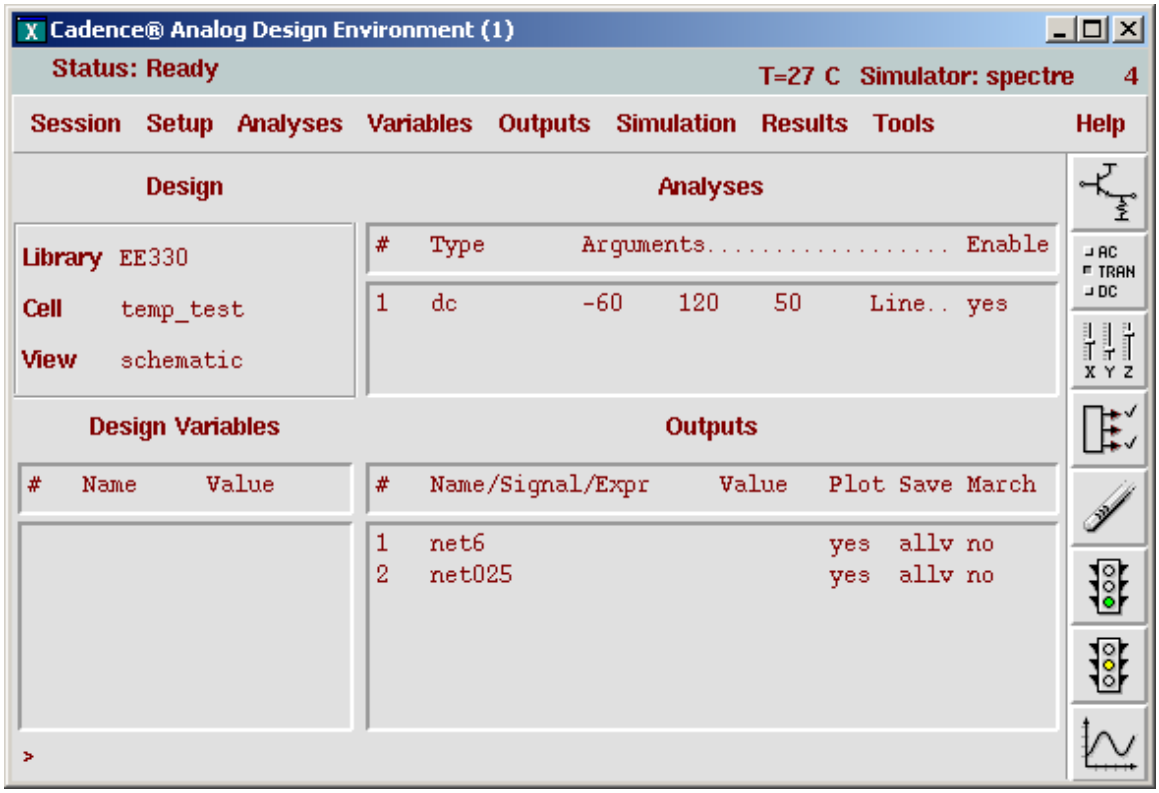


Figure 43.

The type of analysis is dc as in Figure 44.

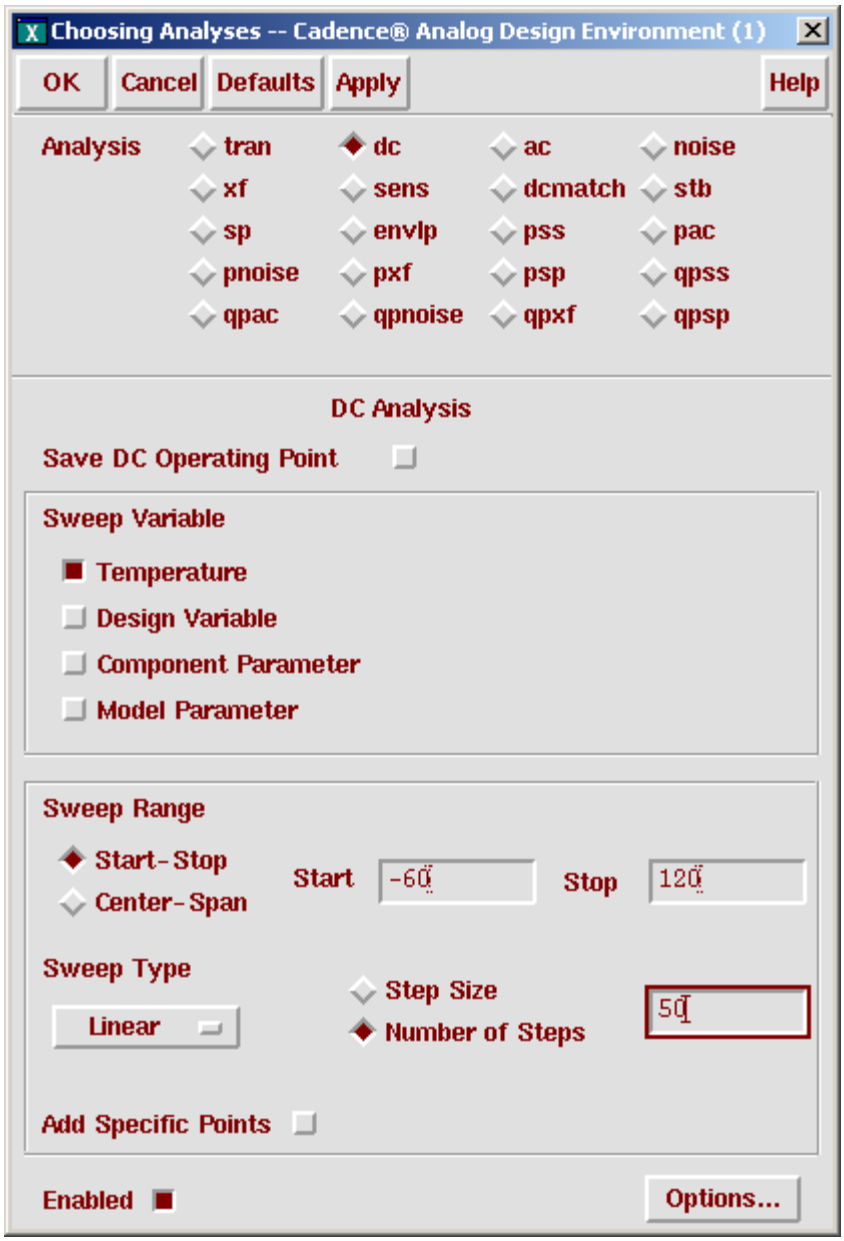

Choosing Analyses -- Cadence® Analog Design Environment (1)
OK
Cancel
Defaults
Apply
Help
Analysis
tran
dc
ac
noise
xf
sens
dcmatch
stb
sp
envlp
pss
pac
pnoise
pxf
psp
qpss
qpac
qpnoise
qpxf
qpsp
DC Analysis
Save DC Operating Point
Sweep Variable
Temperature
Design Variable
Component Parameter
Model Parameter
Sweep Range
Start-Stop
Center-Span
Start
-60
Stop
120
Sweep Type
Linear
Step Size
Number of Steps
50
Add Specific Points
Enabled
Options...

Figure 44

The output signals to be observed during the simulation are:

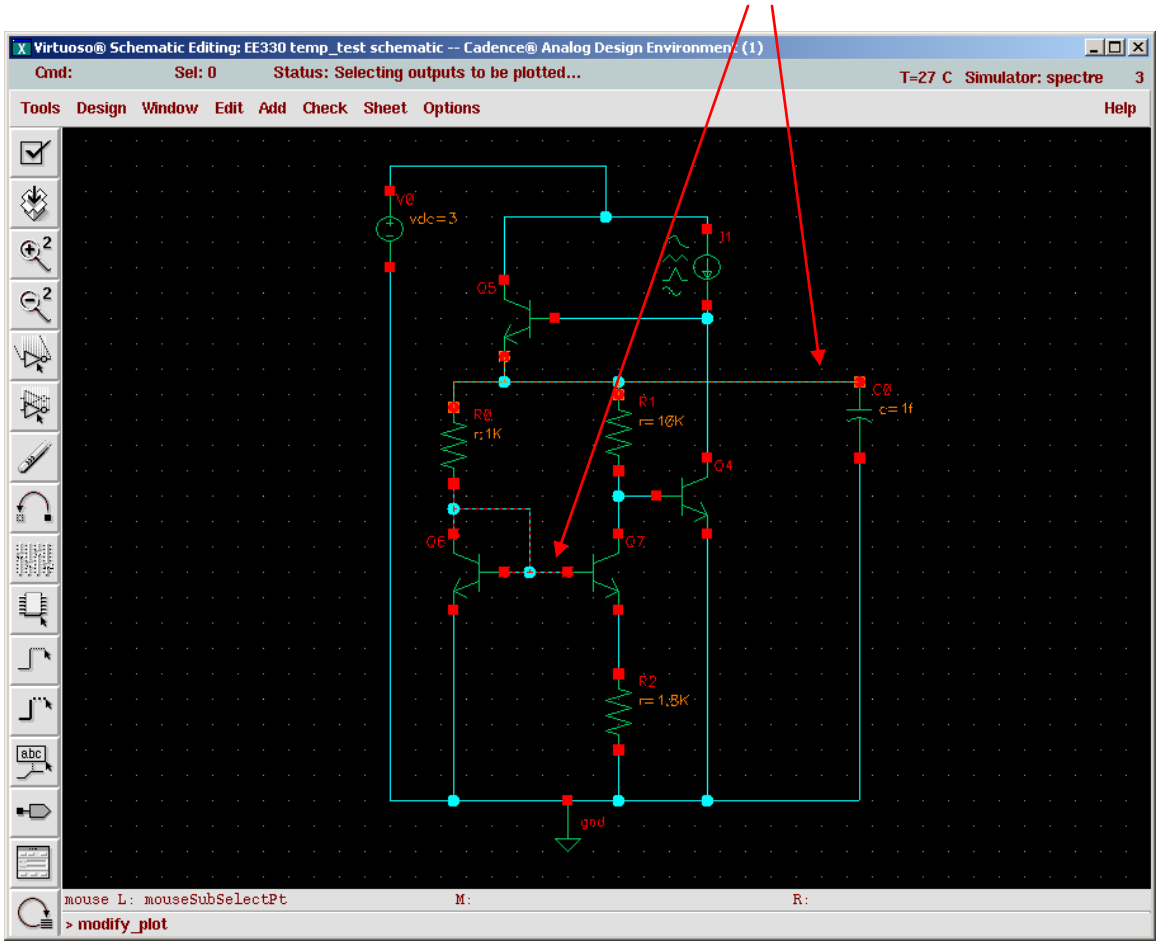


Figure 45

To start simulation from click on “Netlist and Run”

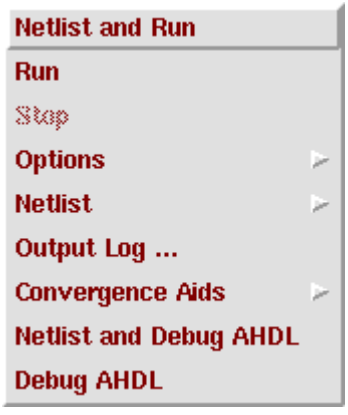


Figure 46

The waveforms for the output signals as we perform dc analysis on variable temperature:

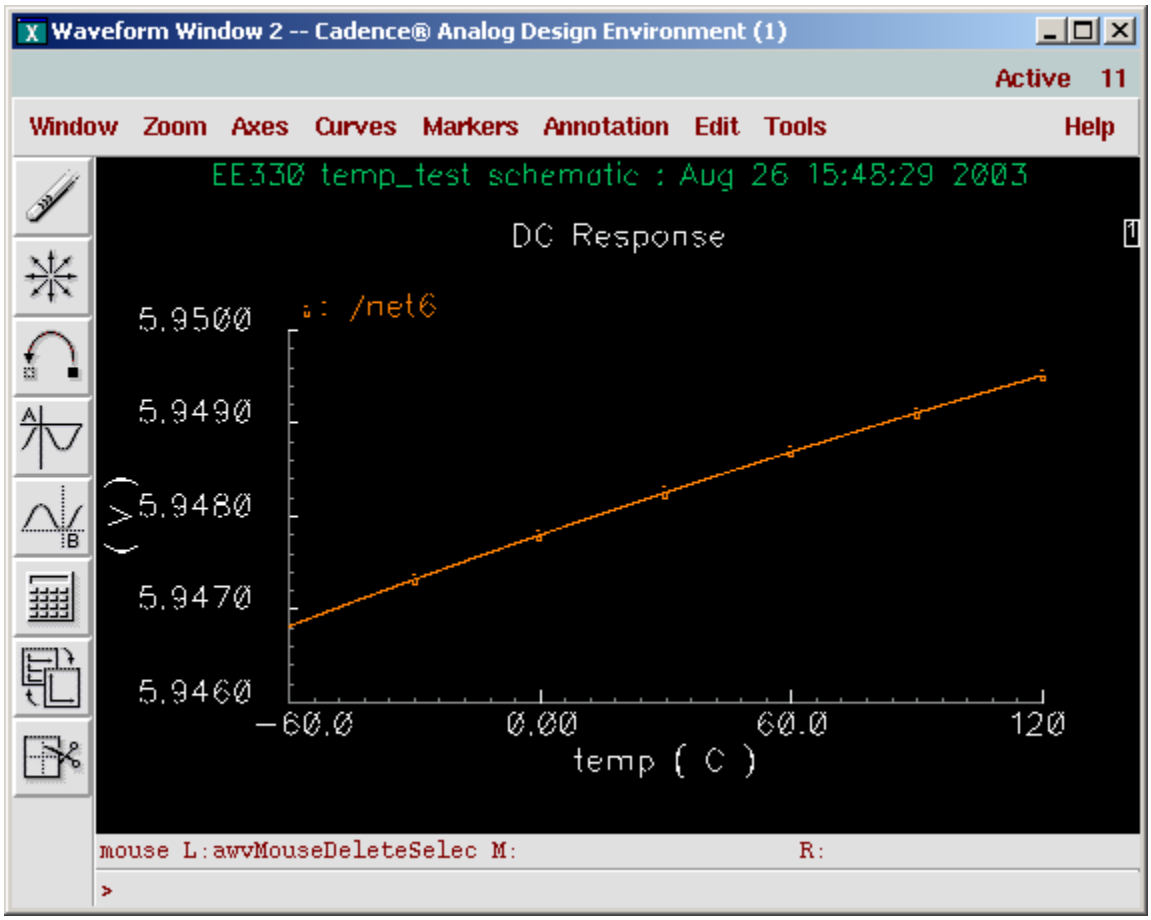


Figure 47

Bandgap Temperature Reference (Version 2)

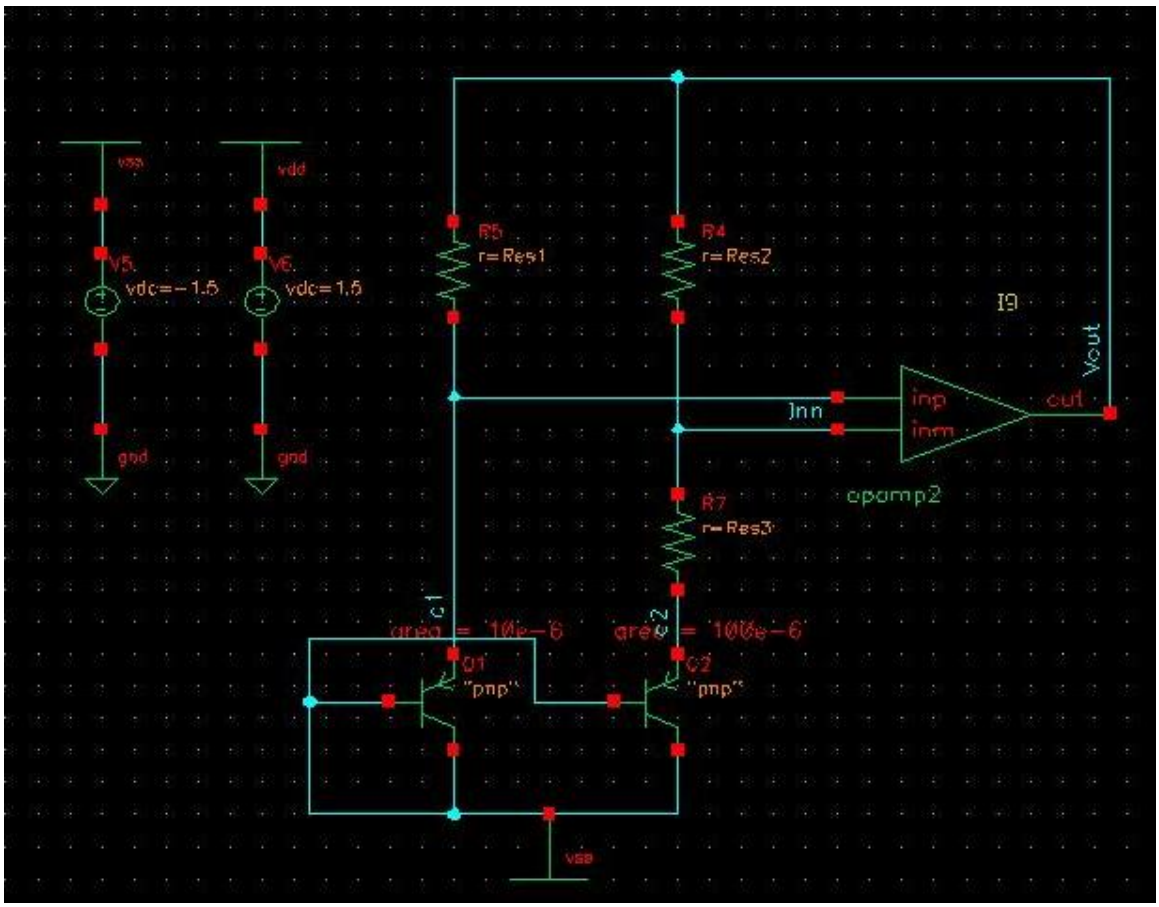


Figure 48

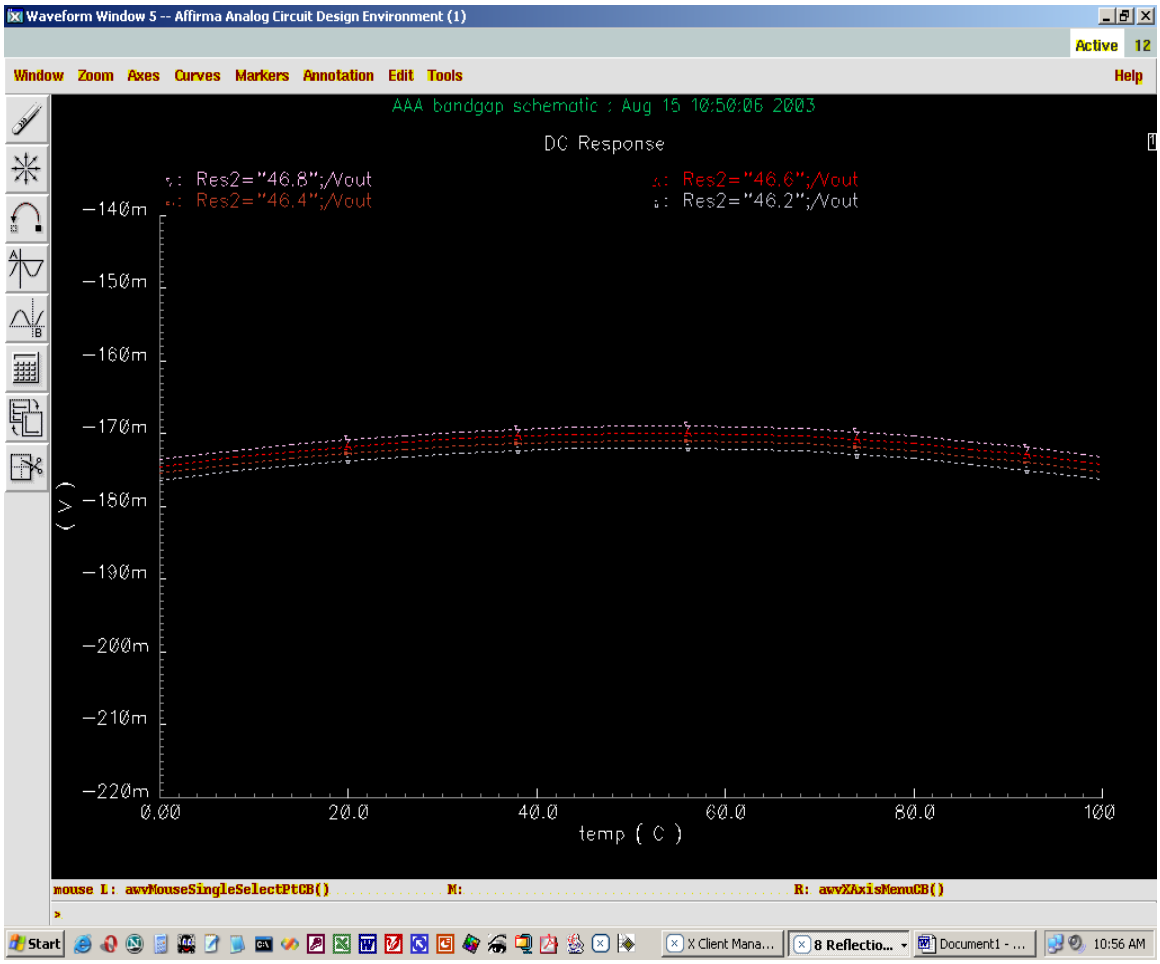
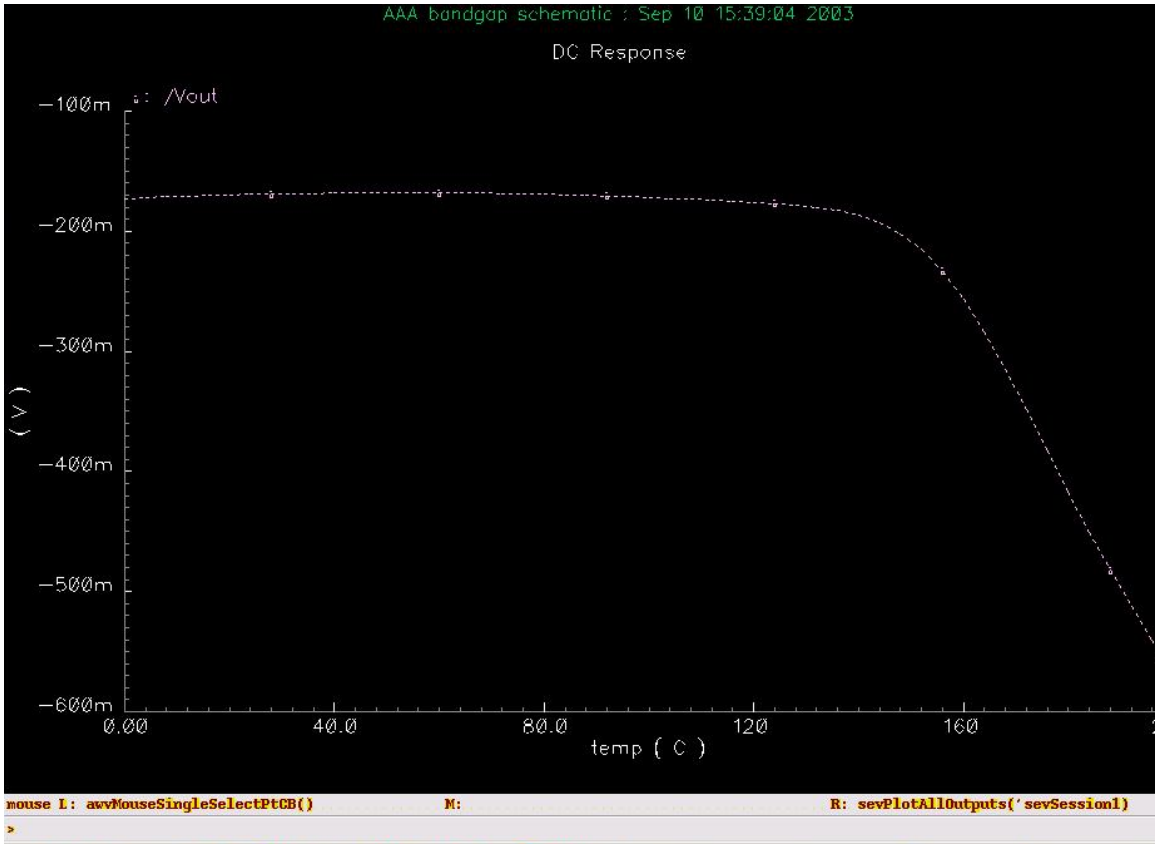

Waveform Window 5 -- Affirma Analog Circuit Design Environment (1)
Active 12
Window Zoom Axes Curves Markers Annotation Edit Tools Help
AAA bandgap schematic : Aug 15 10:50:06 2003
DC Response
Res2="46.8";/Vout
Res2="46.4";/Vout
Res2="46.6";/Vout
Res2="46.2";/Vout
−140m
−150m
−160m
−170m
−180m
−190m
−200m
−210m
−220m
0.00
20.0
40.0
60.0
80.0
100
temp (C)
mouse L: awvMouseSingleSelectPtCB()
M:
R: awvXAxisMenuCB()
Start
X Client Mana...
8 Reflectio...
Document1 - ...
10:56 AM

Figure 49


AAA bandgap schematic : Sep 10 15:39:04 2003
DC Response
: /Vout
−100m
−200m
−300m
−400m
−500m
−600m
(V)
0.00
40.0
80.0
120
160
temp (C)
mouse L: awvMouseSingleSelectPtCB()
M:
R: sevPlotAllOutputs('sevSession1)
>

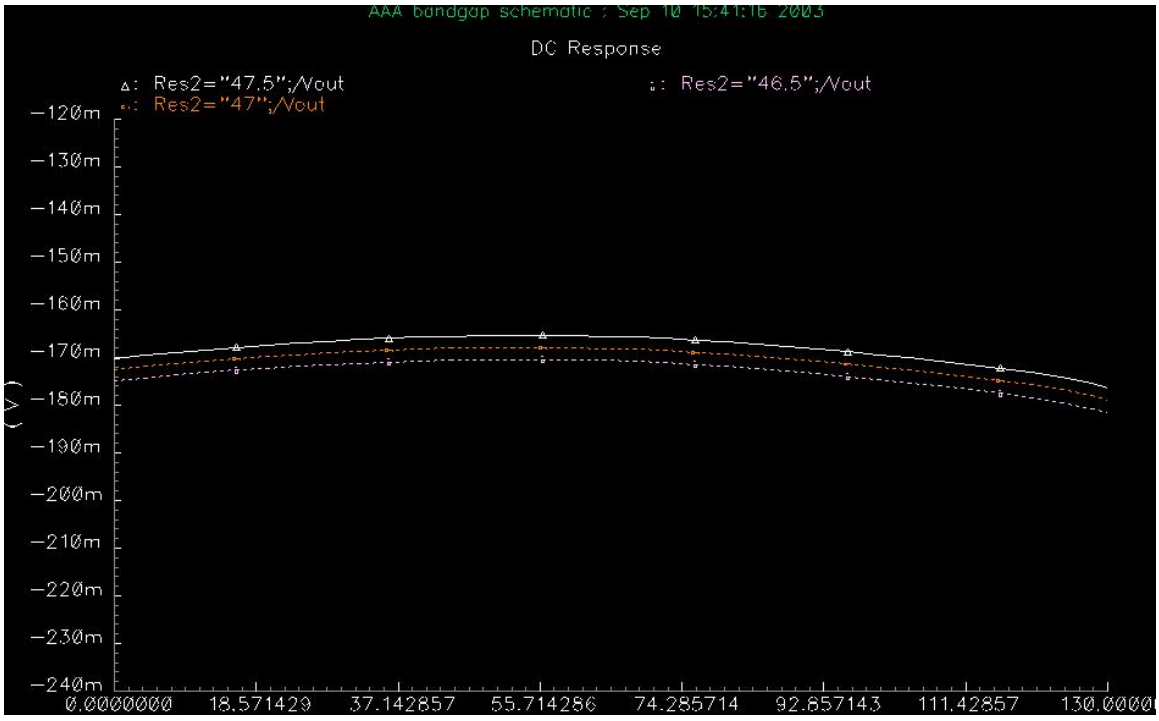

AAA bandgap schematic : Sep 10 15:41:16 2003
DC Response
: Res2="47.5";/Vout
: Res2="47";/Vout
: Res2="46.5";/Vout
−120m
−130m
−140m
−150m
−160m
−170m
−180m
−190m
−200m
−210m
−220m
−230m
−240m
(V)
0.0000000
18.571429
37.142857
55.714286
74.285714
92.857143
111.42857
130.0000

Figure 50

Single Stage Amplifiers

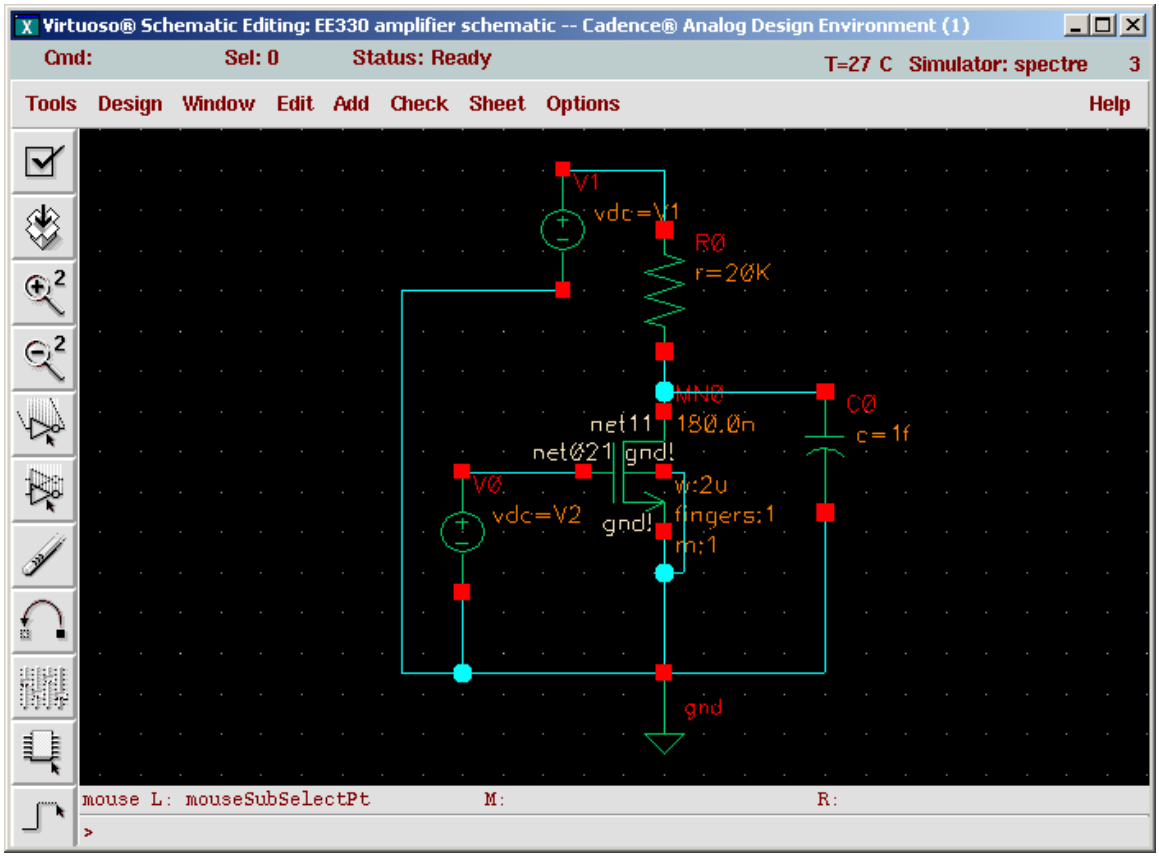


Figure 51

This is a common-source single-transistor amplifier.

Type of analysis performed:

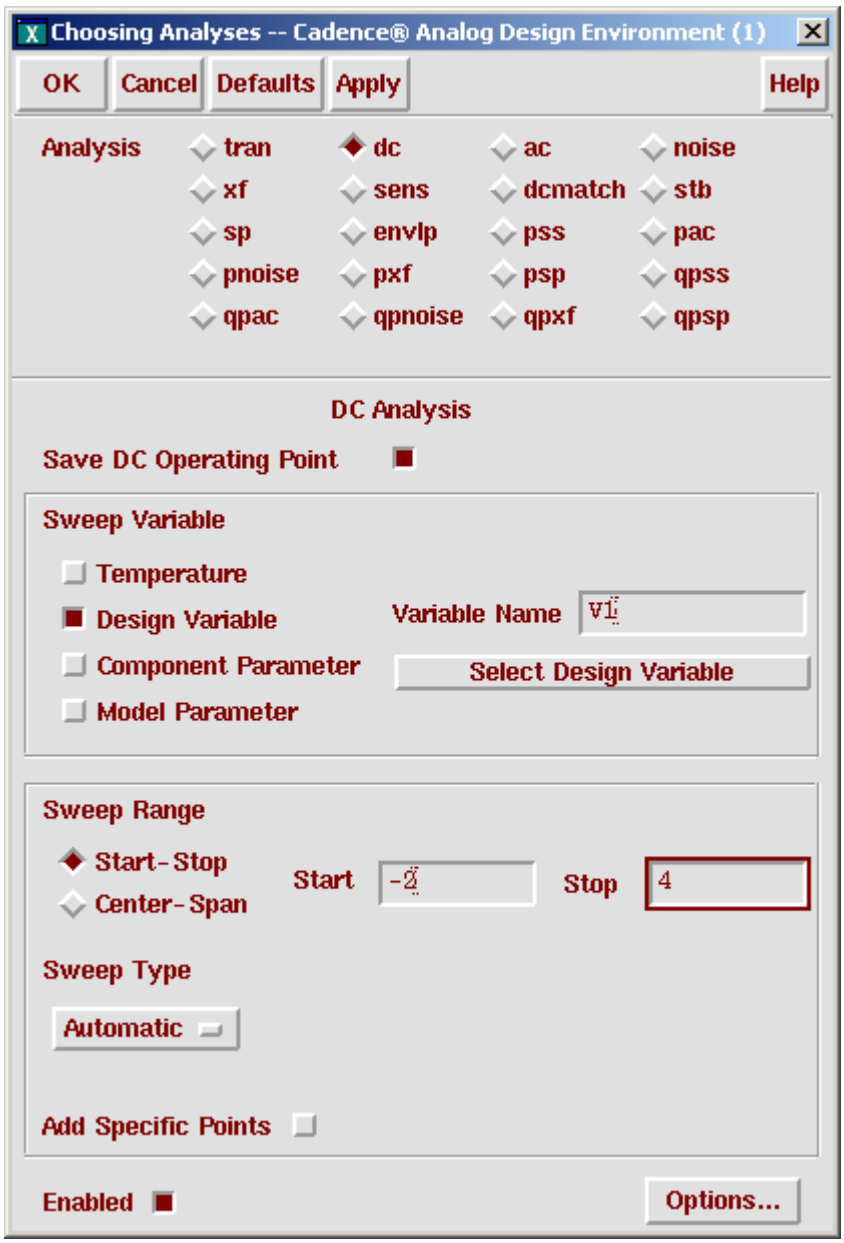


Figure 52

There are two voltage variables set in this circuit. One is for the VDD voltage and the other is for Vin source.

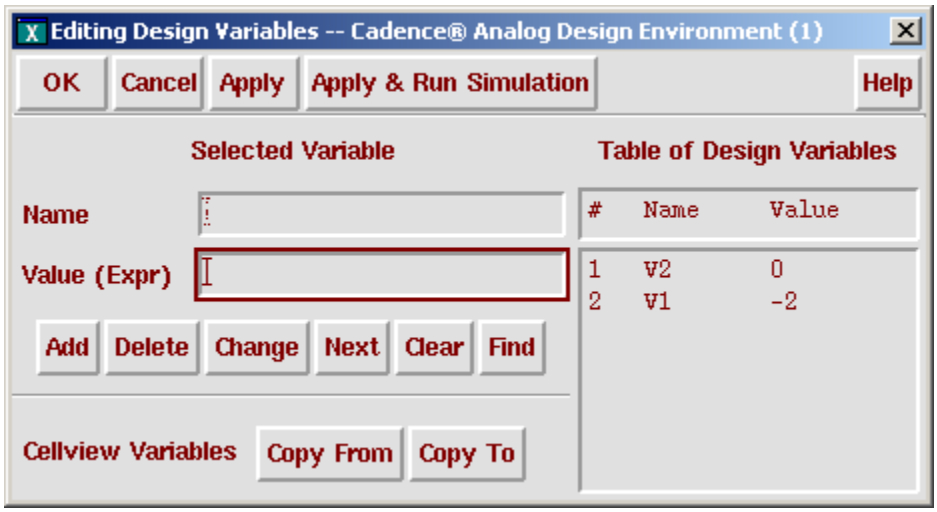


Figure 53

The output selected is as highlighted below:

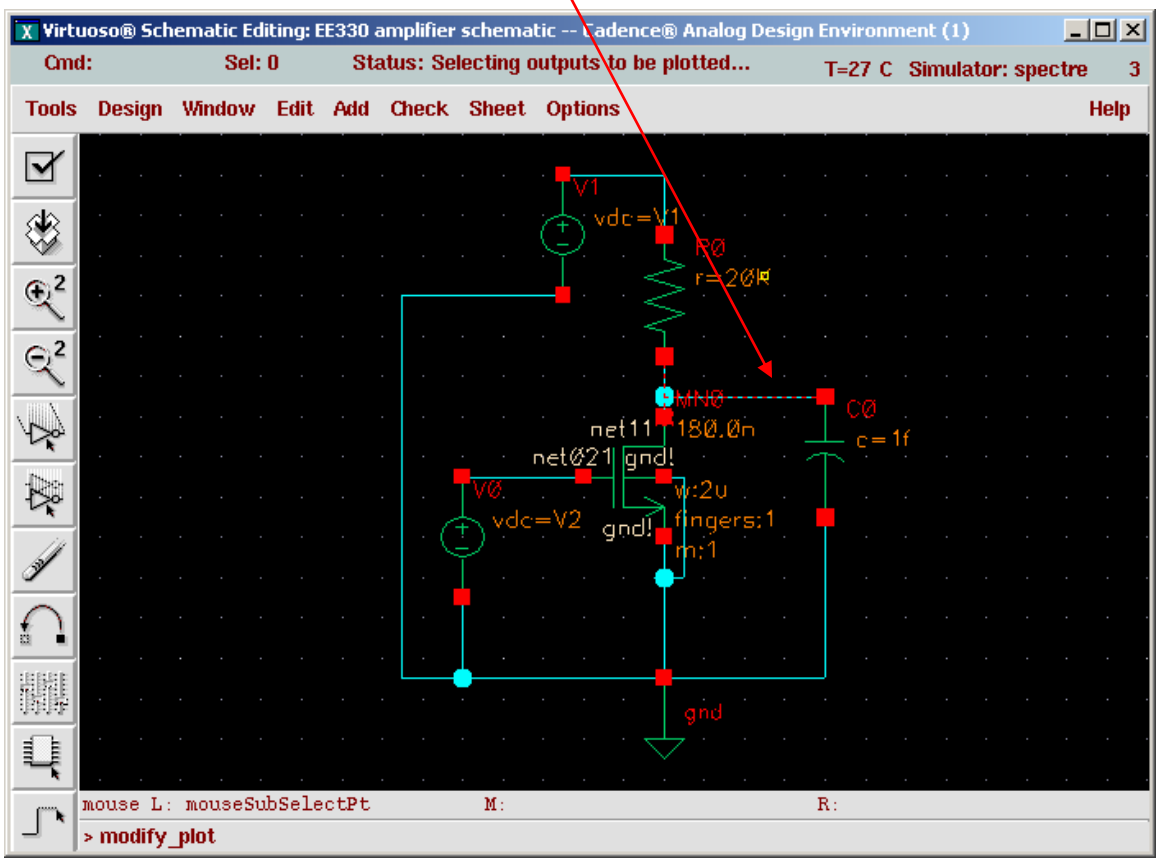
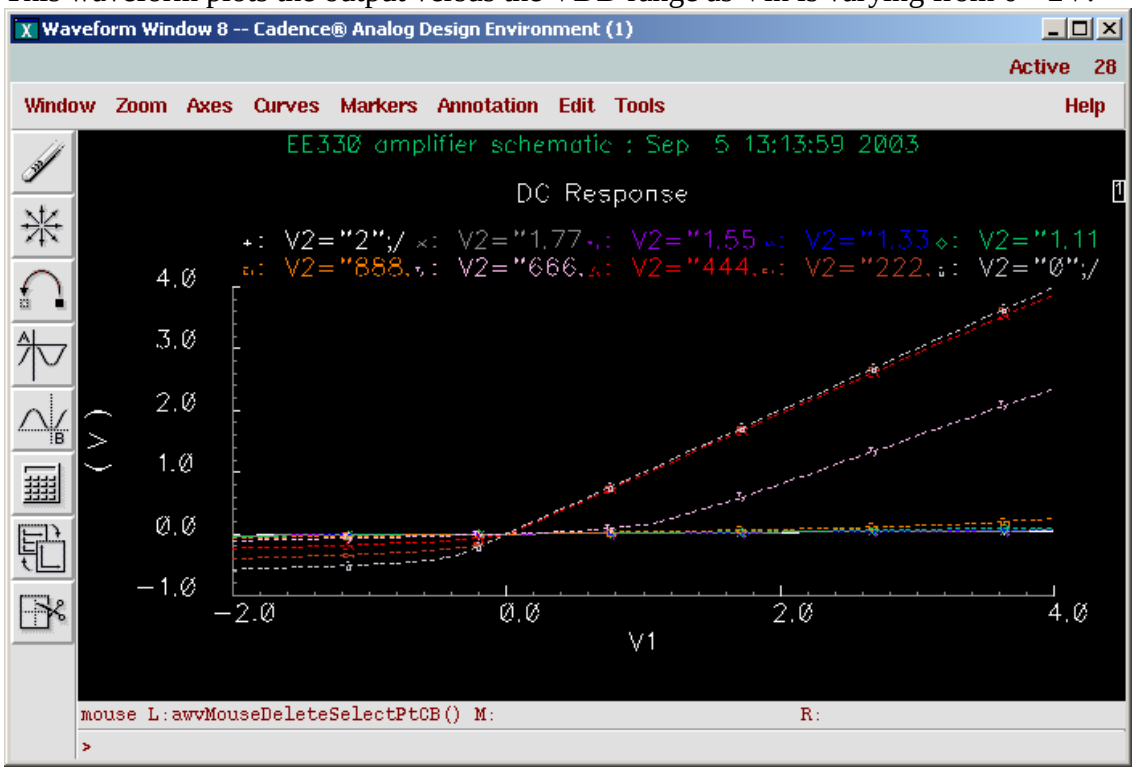


Figure 54

This is the waveform obtained form the common-source amplifier.
This waveform plots the output versus the VDD range as Vin is varying from 0->2V.



This waveform plots the Vin vs Vout as VDD varies.

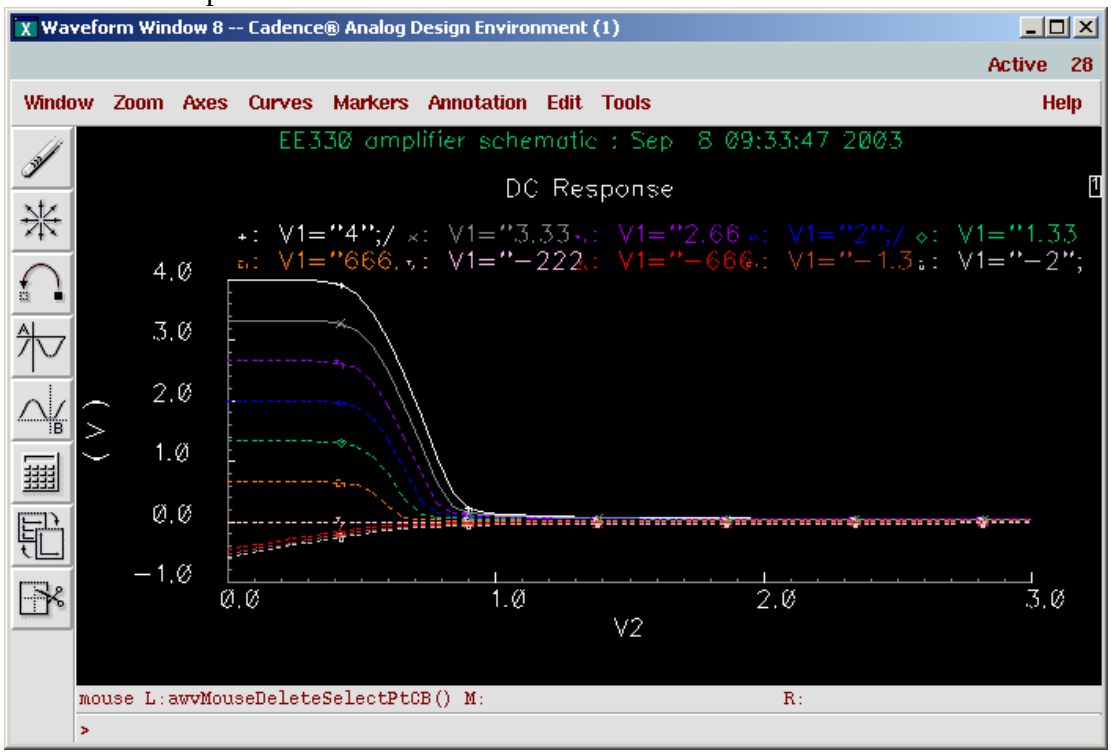


Figure 55 and 56

MOS Differential Amplifier with a Current Mirror Load

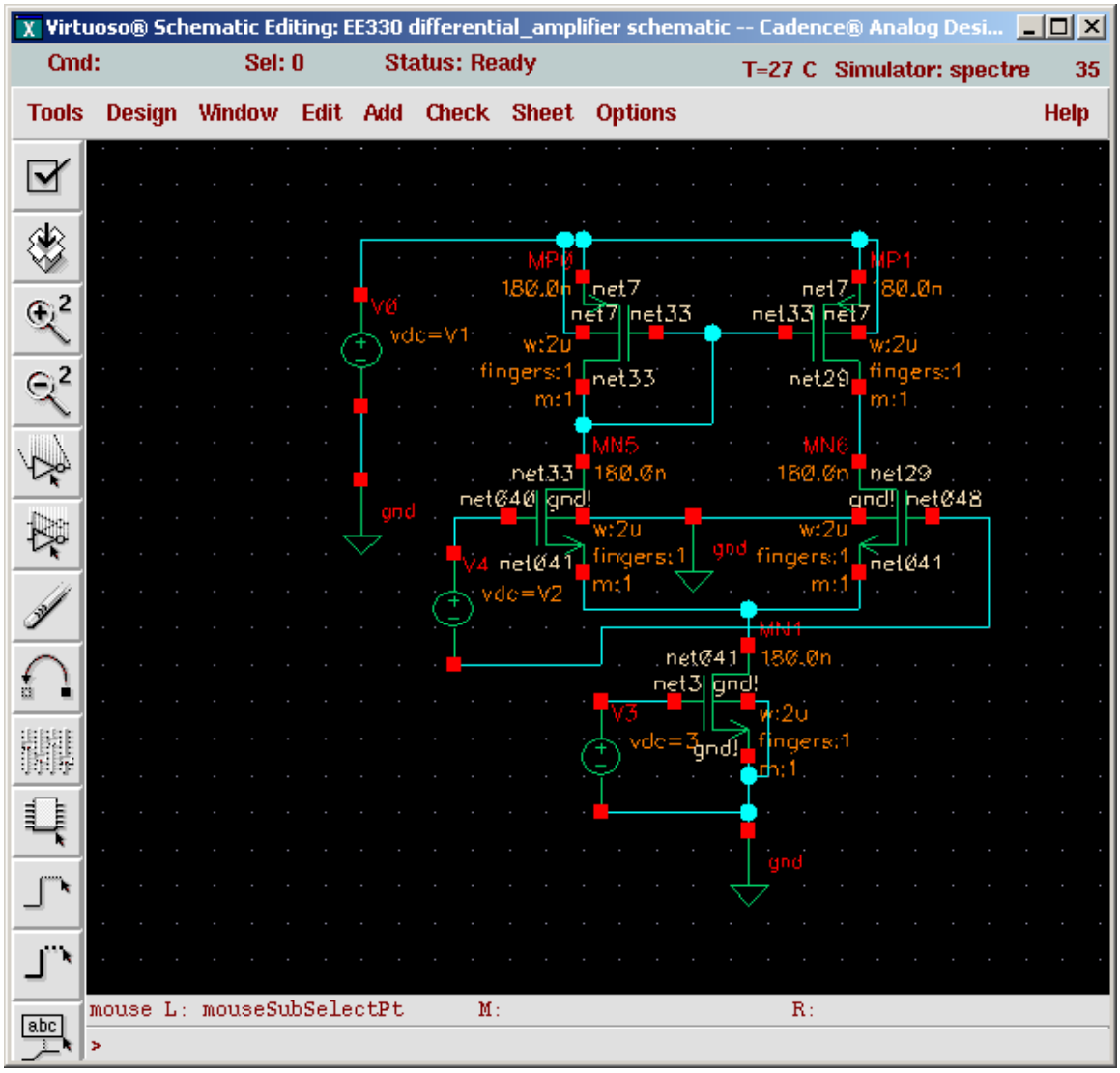


Figure 57

This is a MOS current mirror load differential amplifier.

The type of analysis performed is DC.

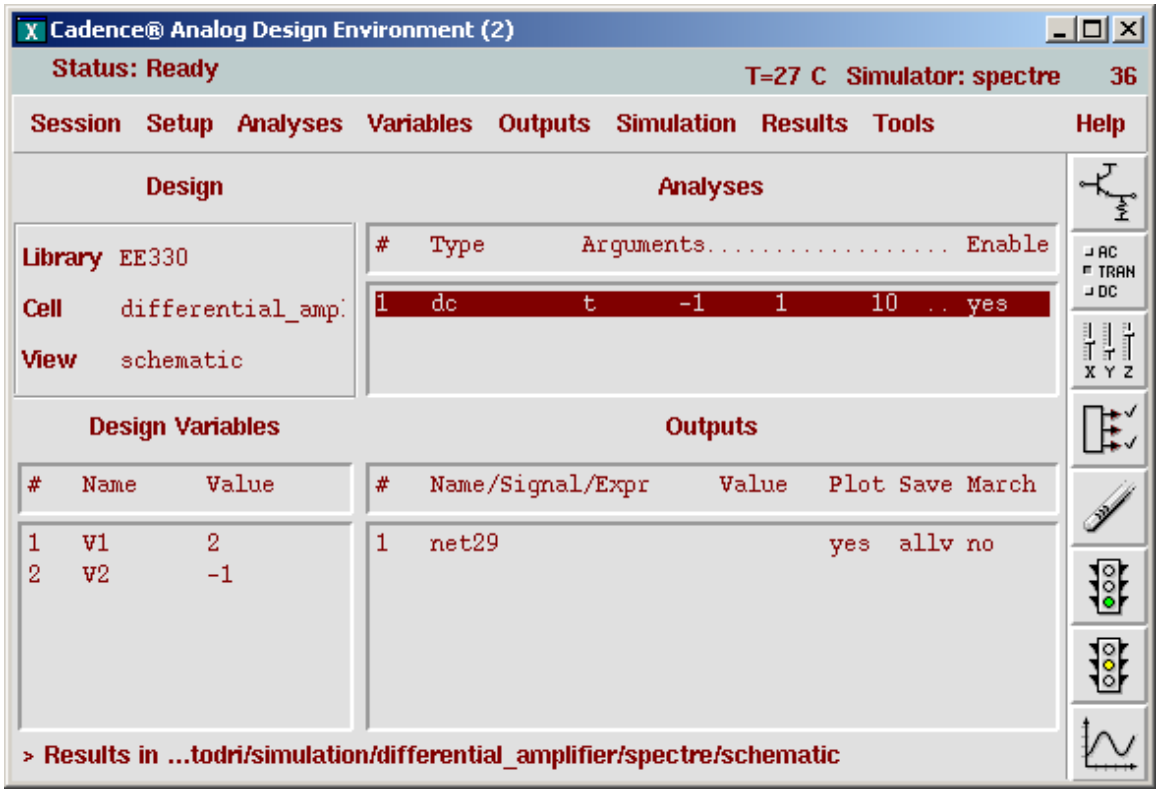


Figure 58

The analysis is performed on Variable V2 which is the input voltage.

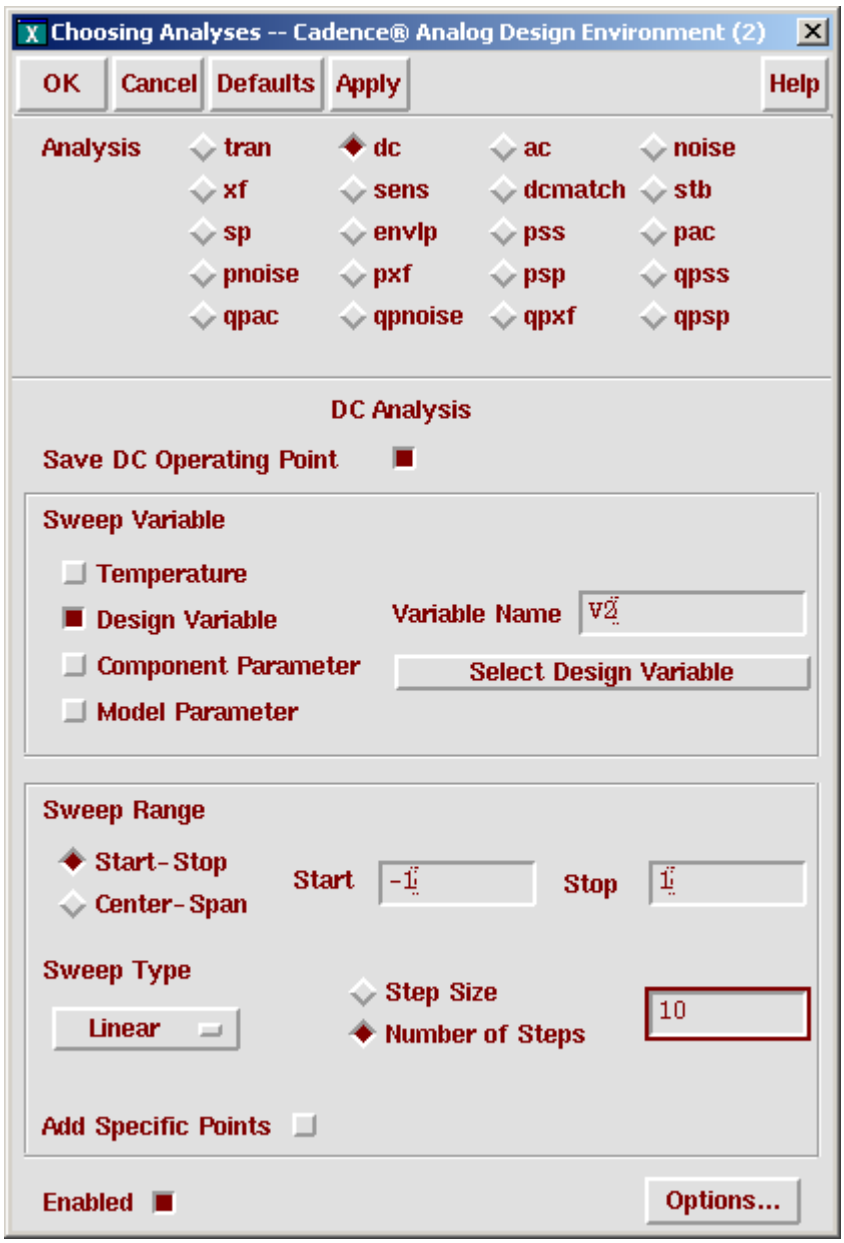


Figure 59

The variables used for this simulation are:

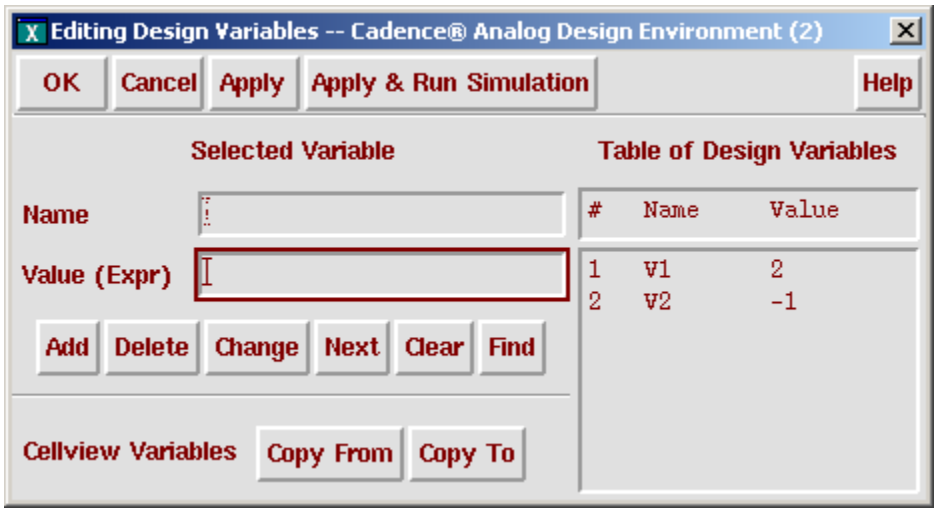


Figure 60

Where V1 is for the input voltage and V2 is for the VDD voltage source. Check schematic for more information.

The parametric analysis performed for variable V1 after performing Dc simulation.

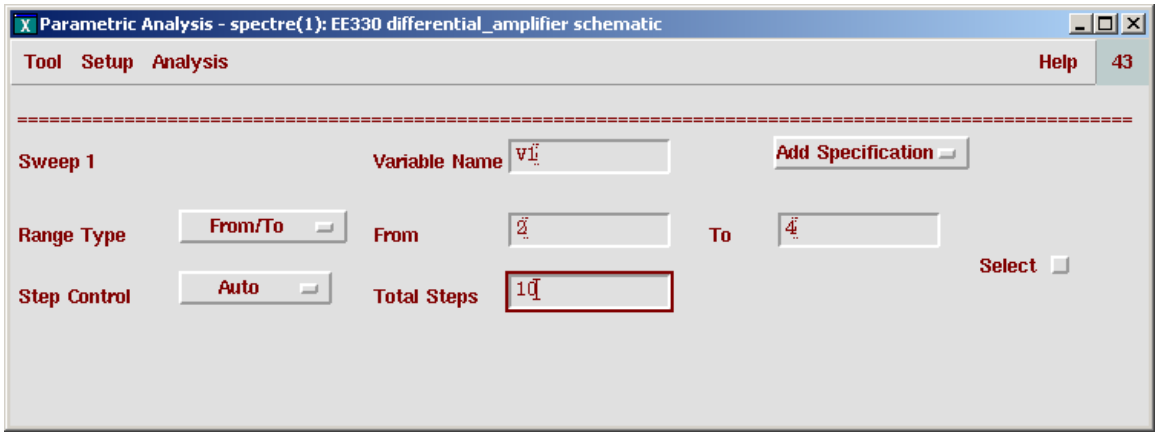


Figure 61

The waveform obtained looks like below.
This waveform is Vin vs Vout plot.

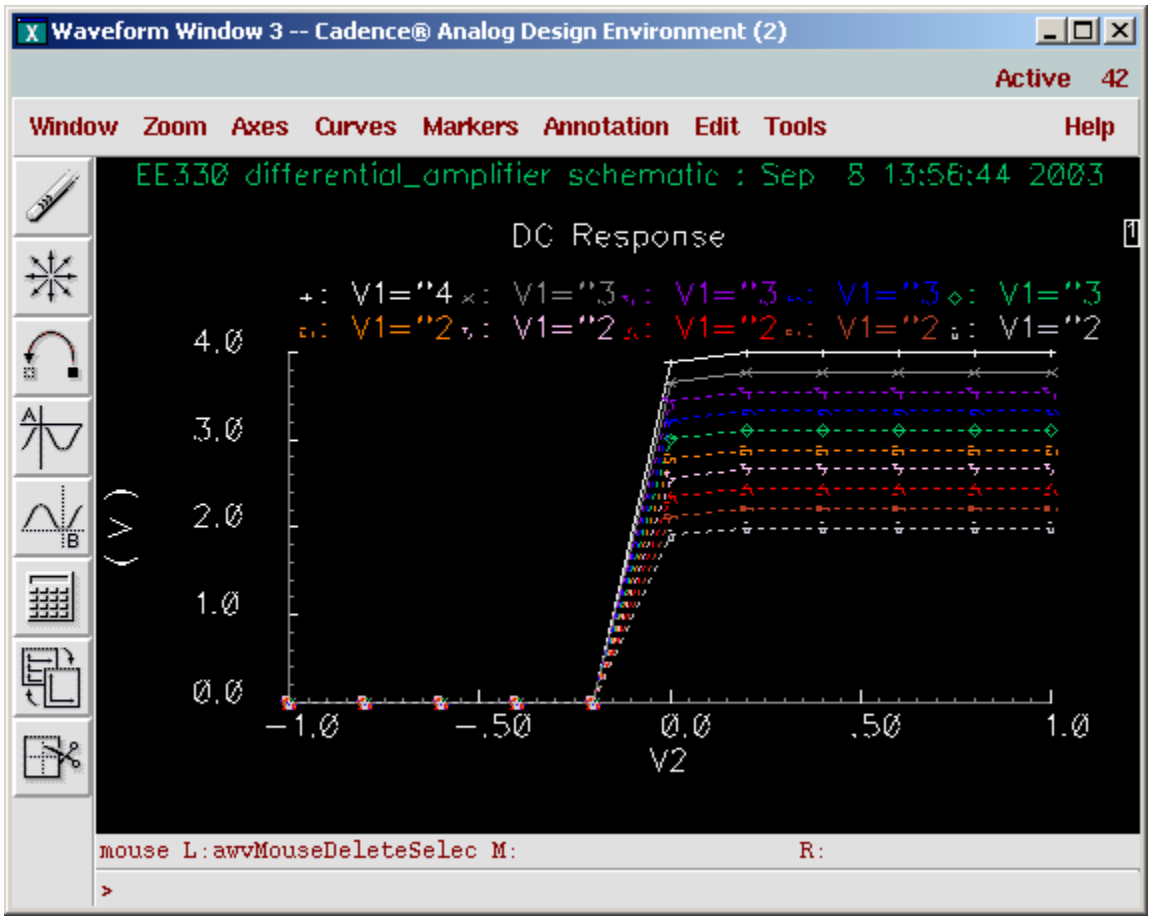


Figure 62

High Frequency Response in Diff. Pairs

In order to estimate the frequency response of the differential pair with active current mirror the schematic model shown below is used where all capacitances are neglected.

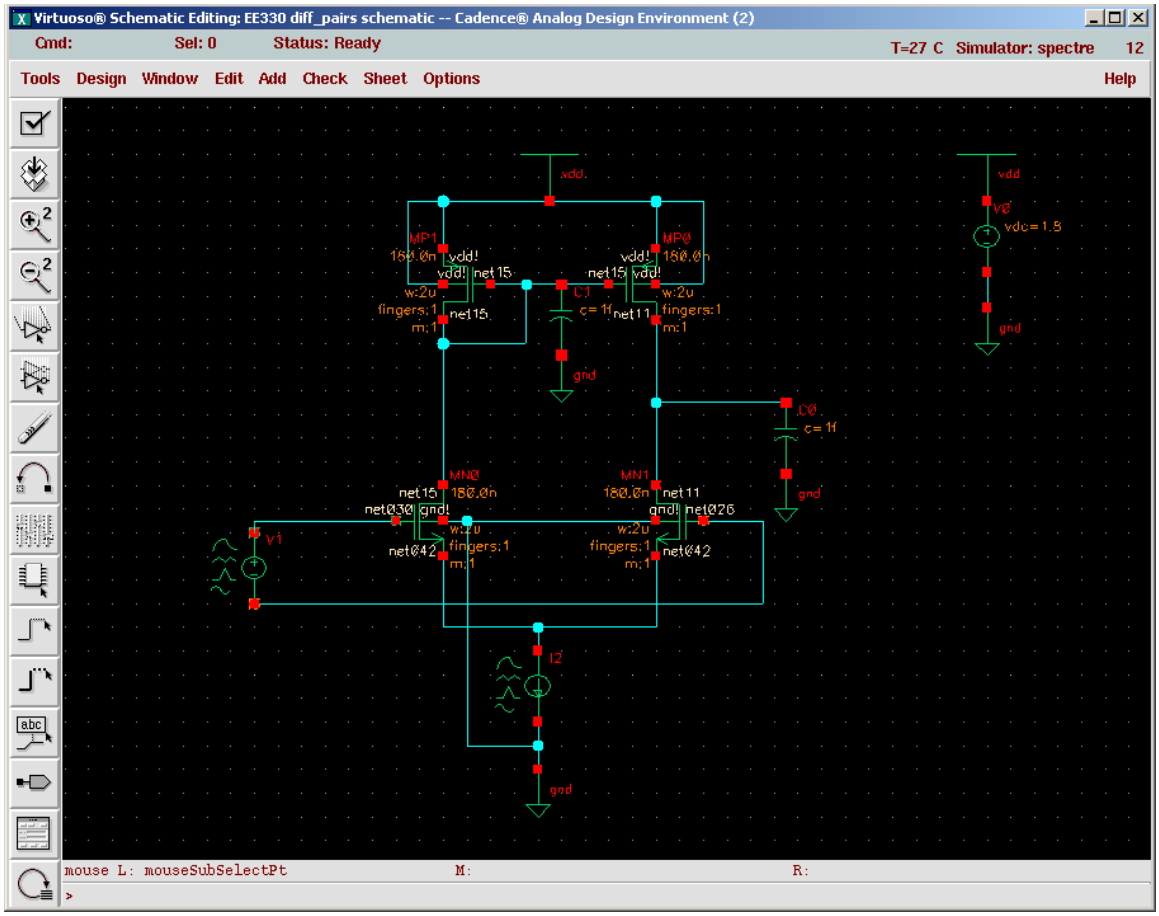


Figure 63

Performing Transient Analysis: The selected nets are input and output nets.

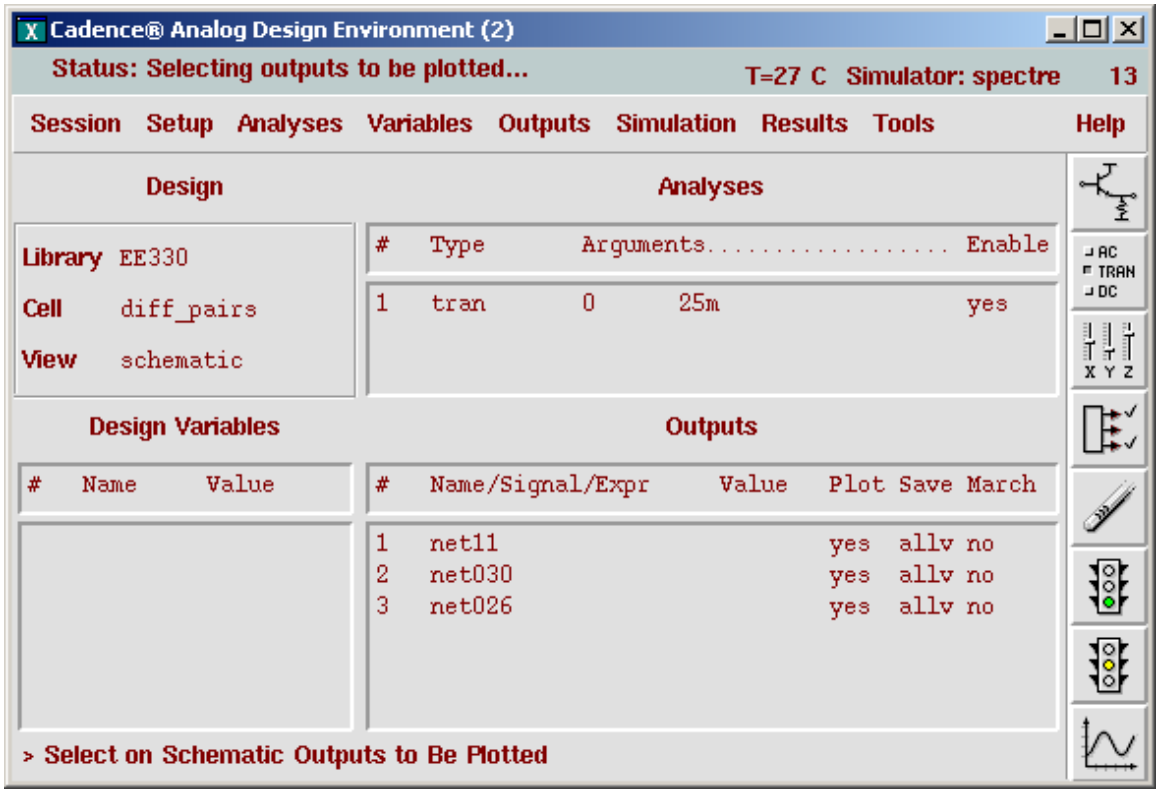


Figure 64

Transient analysis is performed.

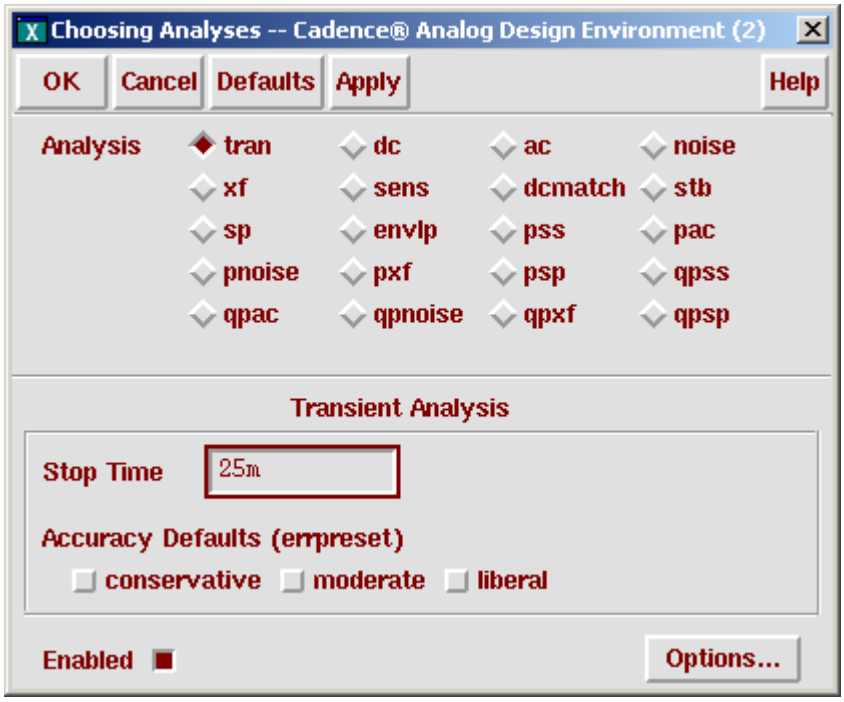
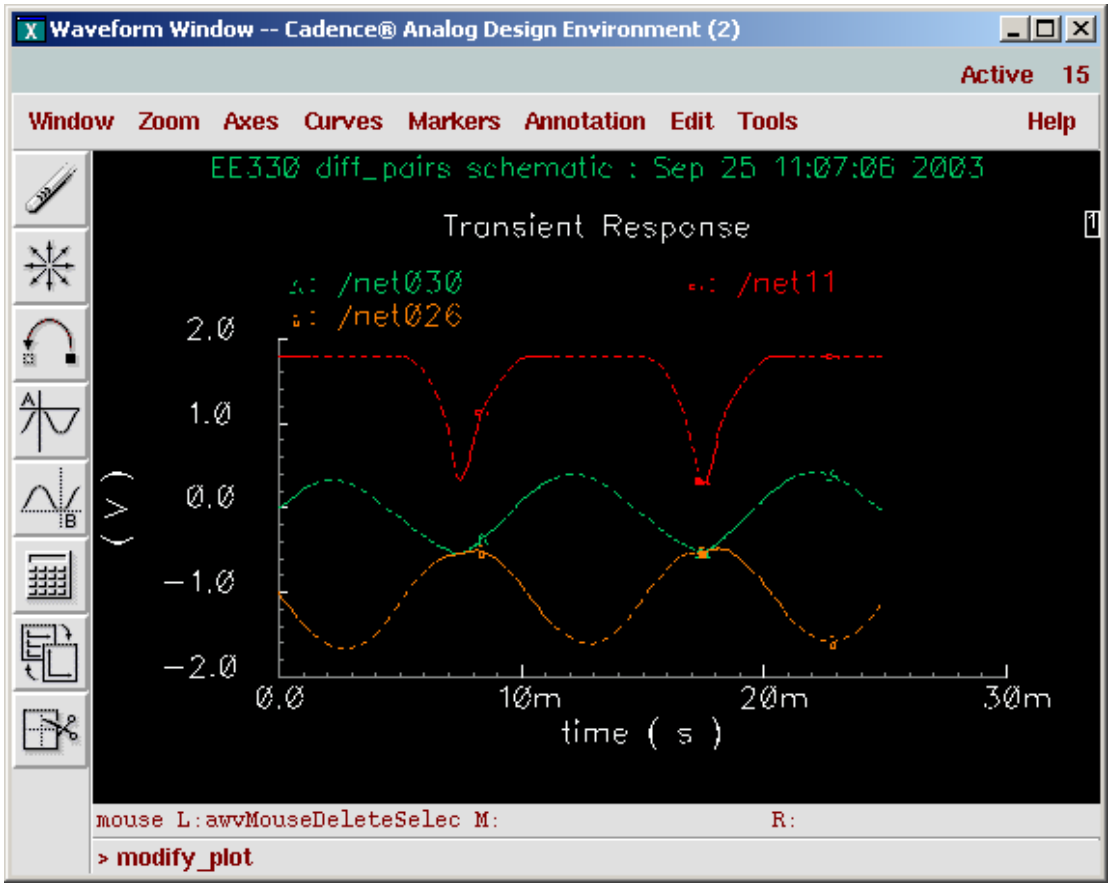


Figure 65

The waveforms obtained are: Figure 66



Noise in Differential Pairs

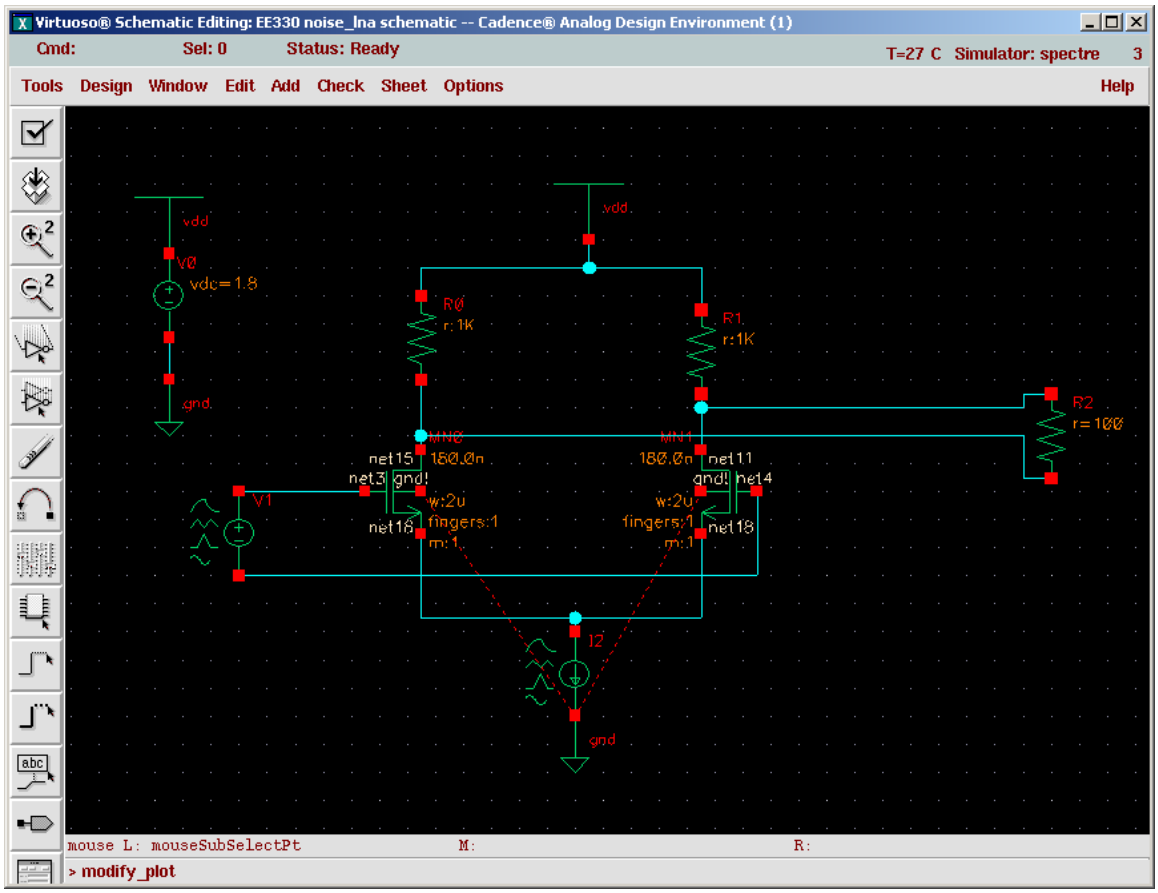


Figure 67

This type of modeling accounts for 1/f noise and input-referred noise.

Performing Transient Analysis: Nets selected are input and output nets.

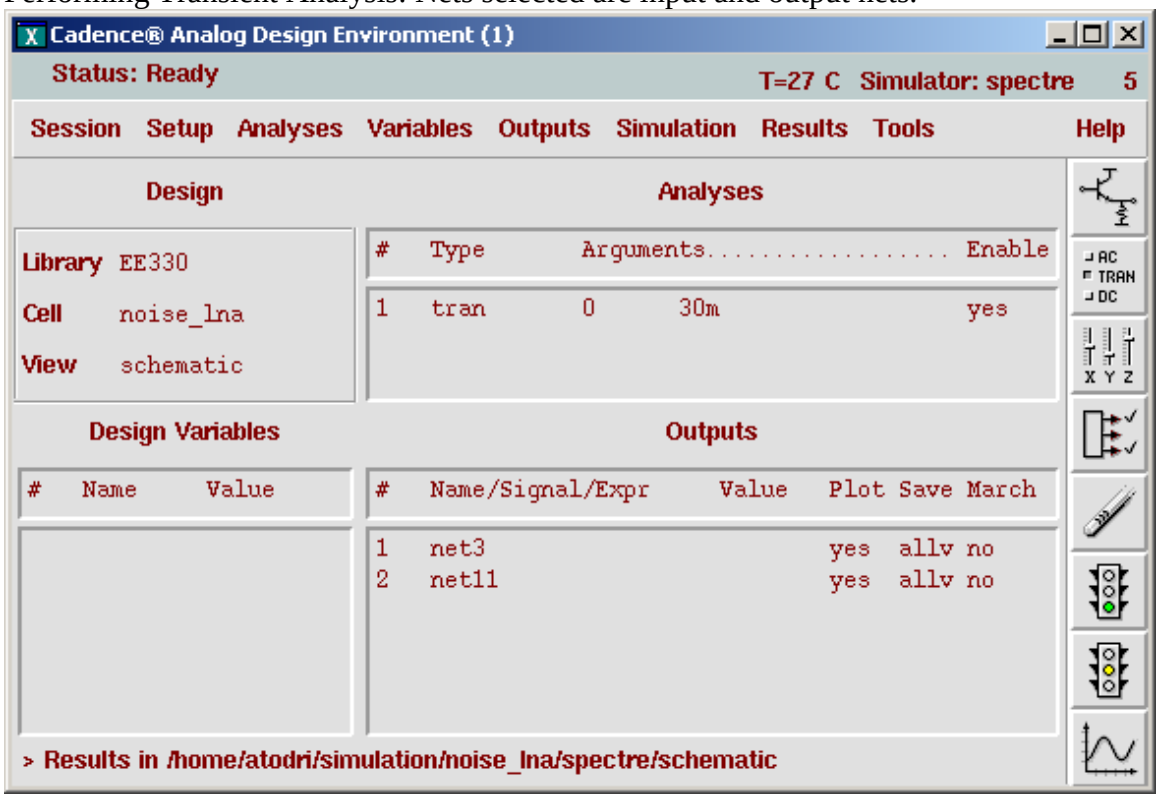


Figure 68

Transient Analysis

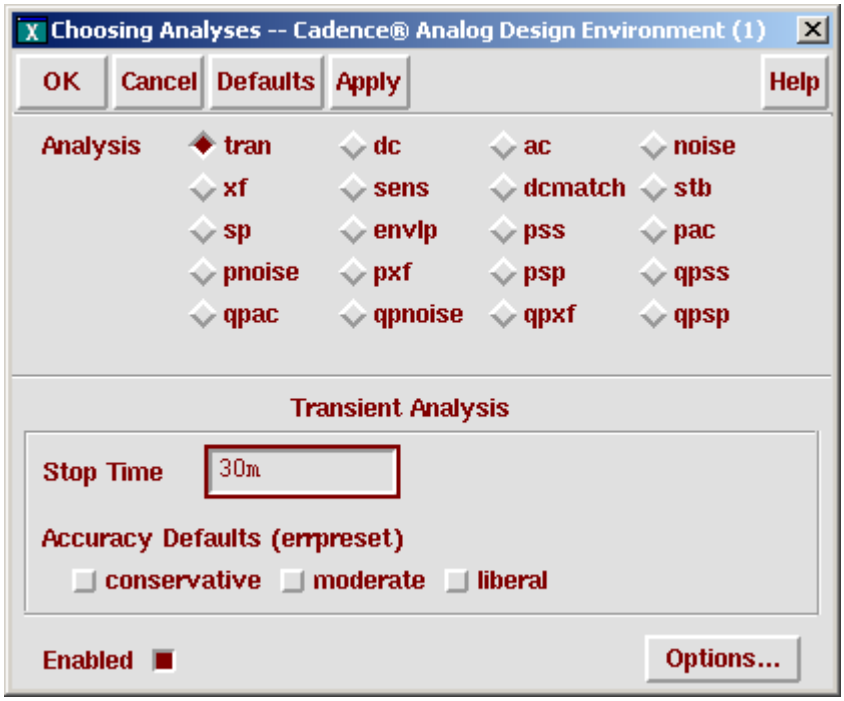


Figure 69

The waveforms obtained;

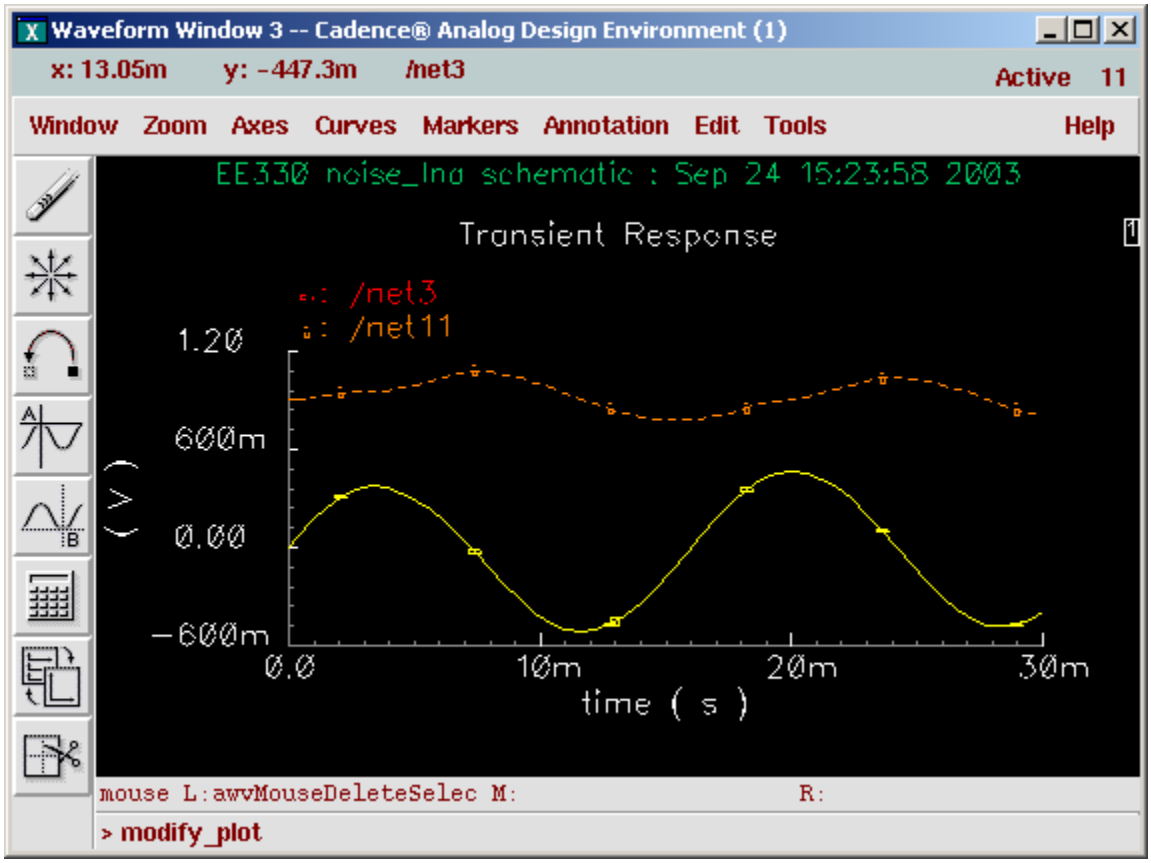


Figure 70