Senior Physical Design Engineer Resume Example

SEARCH FOR RESUMES BY INDUSTRY, JOB TITLE OR KEYWORD.

Senior Physical Design Engineer

Search

JESSICA CLAIRE

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SKILLS

- Expertise in execution and debugging PDN issues like Grid weakness, Dynamic/Static IR Drop, SignalEM, Electrostatic discharge (ESD) and Low Power Ramp-up analysis with Apache tools.
- Strong fundamentals in Physical design execution through handling diverse blocks in multiple projects (7nm-45nm). Expertise includes floor-planning, PnR, CTS, RC-extraction, timing closure, physical and electrical verification.
- Research experience which focused on the design, integration, and implementation of novel, digital on-chip voltage sensing schemes in nanometer CMOS.
- A big advocate of automation and was involved in product engineering and QA infrastructure development throughout the career using Perl, TCL, Makefile, and Shell scripting.
- EDA Tools: Synopsys (ICC, ICC2, PrimeTime, StarRC, Formality), Cadence (Innovus,Voltus), Mentor (Olympus, Calibre), Apache (Redhawk, Totem, Pathfinder), Dorado (Tweaker), RTDA (Flowtracer).

EXPERIENCE

Physical Design Engineer, 07/2018 - Current
Intel Corp. – Portland, OR

- PnR execution for multiple DDR blocks from netlist to GDS and coming up with recipes and methodologies for power,performance and area.
- Seahawk: Owned a block from floorpan to GDS as well as took ownership for DQ clocking
- Jade : Owned one of the most critical blocks in AMS from floorpan to GDS . Took ownership of the UPF flow and piloted it for AMS.
- Power Integrity for AMS : Leading the signoff for AMS which includes power grid exploration , analysis ,execution and coming up with strategies for hitting the IR targets. Worked closely with multiple teams across Apple to make sure EMIR clean IP delivery .
- Lead various methodology efforts to reduce the time for execution and improve the quality metrics.

Staff Physical Design Engineer, 05/2013 - 07/2018
Synopsys, Inc. – Texas, AL

- PnR execution for multiple graphics blocks from netlist to GDS which included floorplanning, clock and power distribution timing closure, physical and electrical verification.
- Graphics team PDN/IR lead : Responsible for signoff for Graphics blocks which included setting IR targets, power grid exploration , driving execution and coming up with Bump, Decap, Switch placement strategies.
- Responsible for working with logic design team to understand partition architecture and drive physical aspects early in the design cycle meeting schedule and design goals.
- Responsible for PPA(Power,Performance,Area) exploration for GPU blocks , identify potential solutions and drive execution.
- Developed flows and scripts for PDN and PnR for smoother execution and faster turnaround.
- Successfully completed several tapeouts under fast paced design environment with tough deadlines.

Physical Design Intern, 05/2012 - 01/2013
Marvell – Boise, ID

- Lead the Graphics section for closing quality rules and came up with strategies to fix the same.
- PnR execution for a graphics partition which included synthesis, CTS, timing, physical and electrical verification.
- Coming up with timing ECO's for the partition and implementing them.
- Product engineering work included developing scripts for reducing shorts and congestion in the design.

Graduate Research Assistant, 08/2011 - 05/2012
University Of Minnesota – Minneapolis, MN

- Circuits for Accurate Voltage drop/droop sensing (SRC-funded, Task 2083.001)
- Thesis research was focused on the design, integration, and implementation of novel, digital on-chip voltage sensing schemes in nanometer CMOS

Applications Engineer, 10/2008 - 08/2011
Flowserve Corp. – Bridgeport, NJ

- Product engineering and working with leading semiconductor design houses worldwide on cutting edge 45nm and below process technologies, to help adopt/integrate Apache tools into customer SoC CAD flows and methodologies.
- Technical support TIER-1 clients like ST, TI, ARM, LSI with activities like evaluations/benchmarks, Silicon debug product training, flow development, and foundry related support.
- Platforms supported include RedHawk, Totem, Pathfinder, and Sentinel.
- Lead developer of Apache's flagship product RedHawk Explorer.
- QA infrastructure development using Perl.
- Tool release validation and release note preparation for new features.

EDUCATION AND TRAINING

Master of Science: Electrical and Computer Engineering, 2013
University of Massachusetts - Boston - Boston, MA

- Power Optimization using XOR gating and Multivoltage scaling :In this project of two team members, we implemented a new algorithm based on Control data flow graphs. Implemented techniques like XOR Clock gating, Multivoltage scaling, Observability don't care and scheduling techniques. Compared to the existing techniques around 3% power gain was obtained
- Voltage Transient Induction and Detection:Project goals included the studying about various voltage sensors and testing of On Die Droop Detector system based on existing models and simulated the models in Spice. Performed Process variations on the system and the results were studied
- Relevant coursework: VLSI Design Principles, Computer Architecture, Advance VLSI, Advanced Computer Architecture, Synthesis and Verification, Nanoelectronics, Semiconductor Devices

Bachelor of Science: Electronics Engineering, 2008
Model Engineering College - Kochi, Kerala

- Projects: Voice Controlled Wheel Chair (community project), Micro ECG.
- Relevant coursework: Electronic Circuit, Linear Integrated Circuits, Digital Electronics, Solid State Electronics Microprocessors, Communication techniques, Advanced Microprocessors and Micro controllers, Power Electronics.
- Overall percentage: 84% (University first rank holder)

How this resume score could be improved?

Many factors go into creating a strong resume. Here are a few tweaks that could improve the score of this resume:

Resume Strength

Length

Personalization

Target Job

Resume Overview

School Attended

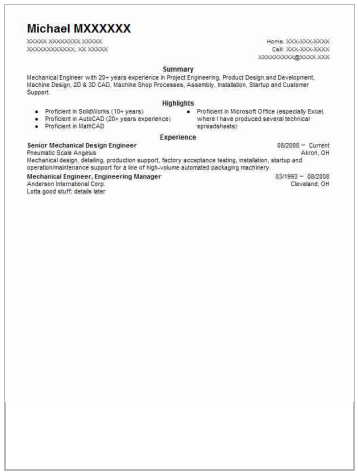
University of Massachusetts - Boston
Model Engineering College

Job Titles Held:

Physical Design Engineer
Staff Physical Design Engineer
Physical Design Intern
Graduate Research Assistant
Applications Engineer

Degrees
Similar Resume

Bachelor of Science


Michael MXXXXXX

Summary

Highlights

Experience

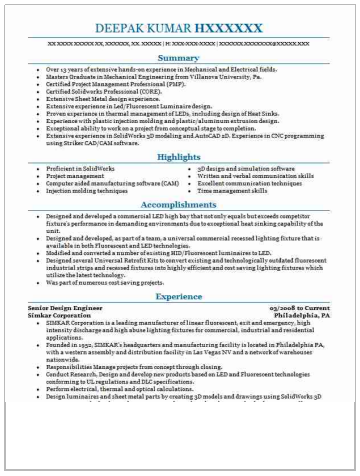
Senior Mechanical Design Engineer 08/2006 – Current
Pneumatic Scale Angelus Akron, OH

Mechanical Engineer, Engineering Manager 03/1993 – 08/2006
Anderson International Corp. Cleveland, OH

Senior Mechanical Design Engineer

Pneumatic Scale Angelus

Strongsville, Ohio


DEEPAK KUMAR HXXXXXX

Summary

Highlights

Accomplishments

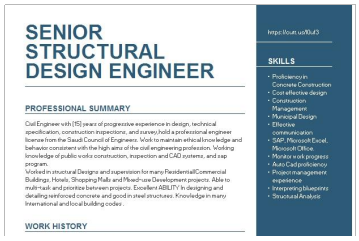
Experience

Senior Design Engineer 03/2008 to Current
Simkar Corporation Philadelphia, PA

Senior Design Engineer

Simkar Corporation

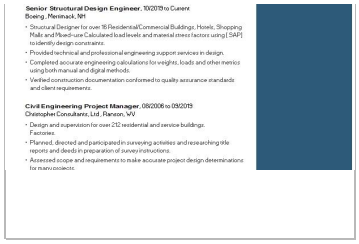
Newark, Delaware


SENIOR STRUCTURAL DESIGN ENGINEER

PROFESSIONAL SUMMARY

SKILLS

WORK HISTORY



Senior Structural Design Engineer, 10/2013 to Current
Boeing , Plesnacd , NH

- Structural Designer for over 15 Residential/Commercial Buildings; Hotels, Shopping Malls; and Mixed-use Calculated load levels and material stress factors using (SAP) to identify design constraints.
- Provided technical and professional engineering support services in design.
- Completed accurate engineering calculations for weights, loads and other metrics using both manual and digital methods.
- Verified construction documentation conformed to quality assurance standards and client requirements.

Civil Engineering Project Manager, 08/2006 to 09/2013
Christopher Consultants, Ltd. , Rancon , WV

- Design and supervision for over 212 residential and service buildings; Factories.
- Planned, directed and participated in surveying activities and researching title reports and deeds in preparation of survey instructions.
- Accessed scope and requirements to make accurate project design determinations for many projects.

Senior Structural Design Engineer

Design Concept Consultant Engineering Office

San Diego, California

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