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> Layout Engineer Resume Samples

Layout Engineer Resume Samples

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THE GUIDE TO RESUME TAILORING

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Gonzalo Monahan

7968 Hettinger Grove, New York, NY ♦ Phone: +1 (555) 736 7317

EXPERIENCE

SCHMIDT GROUP Houston, TX

- Make PCB layouts for automotive audio amplifiers according to specifications from HW developers
- Provide reasonably accurate estimates of timescales for work

- Develops and prepares multi-dimensional layouts and detailed drawings of the semiconductor devices from schematics and related geometry provided by design engineering. Work may be completed through use of CAD or other computerized equipment. Checks dimensions, writes specifications, and verifies completed drawings, artwork or digitized plots. May check design layouts and detailed drawings. The Engineer will also
- Create transistor level sub block layout, based on schematics provided by designers (including careful analog considerations)
- Create state-of-the-art analog IC layouts
- Perform layout reviews
- Contribute to the innovation of product, design, way of working etc

VEUM, BECHTELAR AND JACOBSON**Houston, TX**

- Execute specific working packages according to the deadline interacting with Design Engineering and Project Management
- Execute Layout Reviews and create proper documentation
- Identify best cost-effective and performance-effective solution working in team with design engineers
- Execute Tape Out procedures and task, support or drive Mask Orders submissions
- Cooperate with the development team on continuous improvement activities (methodologies, checklist, working instructions) and contribute to Technology and Design Methodology improvements
- Guarantee compliance to technology design rules (DRC) and perform Physical Verification (LVS) as well as support post-Layout verification
- Prepare packaging technical drawings and support feasibility analysis

DIBBERT INC**Dallas, TX**

present

- Driving/delivering floorplan activities at both IPs and/or SOC level
- Driving the top-level integration using the Mixed Signal on Top flow
- Leading a layout team for the SoC execution and scheduling its activities through the project
- Delivering Analog layout blocks and/or top floorplan strategy
- Participating to the power supply strategy, signals distribution between blocks
- Running all physical verifications as DRC/LVS/DFM and parasitic extractions to achieve high quality layout deliveries
- Participating to design reviews, write documentation and support for integration into products

EDUCATION**TULANE UNIVERSITY****Bachelor's Degree in Electrical Engineering****SKILLS**

- Knowledge and understanding of KONE equipment offering, technical design, structure and details and of the technical strengths and limitations of products
- Good written and spoken English, other languages are benefit
- Basic office and ERP usage skills
- Skills and knowledge about CAD engineering systems
- As a member of an engineering team, shares his/her knowledge and skills with colleagues and participates actively in meetings and workshops
- Takes safety aspects into account and selects environmentally sustainable solutions when possible
- Draws layout drawings for the solution
- Modifies the Bill of Material for the equipment and selects customer specific components when necessary
- Creates design drawings (M-drawings) as requested (signalisation, doors, cabin etc)
- Updates order progress to other stakeholders on a timely basis

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15 LAYOUT ENGINEER RESUME TEMPLATES

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TRUMAN BREITENBERG
8095B Koepf Mount, Phoenix, AZ

PHONE
+1 (505) 506 6533

EXPERIENCE

Zboncak Inc
Chicago, IL // Layout Engineer // 04/2020 – present

- Management and knowledge of specifications for permitted distances, types of demarcation and symbols
- Development of scenarios (variables) to model the production floor
- Have knowledge to identify possible conflicts with machine facilities, product areas and evacuation routes
- Coordination with clients or business units to capture requirements
- Knowledge in Revit desirable
- Knowledge of topographic equipment

Simons I
Chicago, IL

- Team
- Revit
- Work
- Co-op
- Devik
- Delive

EDUCATION

School of the Art Institute of Chicago
Bachelor's in Electrical Engineering

SKILLS

- Completes all design quality checks and data quality checks
- Does design reviews across global team
- May collaborate in package design (Integrator design, RDL design)
- Works with design team in Viet Nam, USA and Italy to ensure the success of the whole product
- May join research programs to implement new ideas for future products and flows
- Work with many experts from around the world and talented highly motivated Viet Nam engineering team

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DUSTY MAGGIO
7962 Francisco Trask, New York, NY
+1 (555) 789 0434

EXPERIENCE

Kutch-Lesch
04/2020 – present
Detroit, MI // Layout Engineer

- Familiar with Cadence Skill, parameterized cells (Pcell), CDF, and colbacks
- Good knowledge of Mentor Calibre nmDRC, mLVs, and PEX
- Familiar with LTPS process
- Good knowledge of device level electrical measurement
- Experience with Siemens TVX
- Working DRC
- O Strong principle
- Fluorplar and subs

Adams and
Detroit, MI

- Active communication and alignment with circuit designers
- Proficient in usage of industry standard tools from Cadence, Mentor and SNPS
- Has developed several mixed signal silicon development and has performed simulation vs silicon was analysis
- Good understanding of ESD structures and Latch-up guidelines
- Good understanding of Advanced CMOS technologies and Foundry Design rules
- Work closely with circuit designers to ensure successful project deliveries
- Run the full mask ordering process until mask release
- Professional, innovative, fair and fun working environment and company culture

EDUCATION

Kent State University
Bachelor's in Electrical Engineering

SKILLS

- an engineer into top
- complete a r junior
- technologies to Die centers
- API/ML, 3rd applications
- Work with ASIC and mixed signal engineers to customize designs for integration in VLSI products
- An Electronics Physical Engineer certificate or a B.Sc. in Electrical Engineering
- Experience running and debugging DRC and LVs with verification tools such as ICI, Calibre
- Proficiency in scripting languages like python, skill

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Katie Koch
6019 Stokes Stravenue, Houston, TX

PHONE
+1 (510) 289 0842

EXPERIENCE

Streich, Kessler and Fritsch
New York, NY // Layout Engineer // 11/2020 – present

- Typically requires an MSCE or BSEE with a minimum of 5+ years of related experience
- Responsible for opening and delivering large sub-blocks to the integration team
- Uses good communication skills to collaborate and delegate work to global layout design teams
- Familiar with various layout design tools such as Calibre, matchit
- Proficient in Cadence
- Has exp
- Experience with circ

Schuster and
New York, NY // Layout Engineer // 02/2017 – 05/2020

- Interpreting LVs, DRC, and ERC reports finding the fastest way to complete layout
- Obtaining advanced CAD tools and mask design knowledge to deliver a correct and robust layout that meet stringent matching performance, area, and power requirements
- Experience in analog/mixed signal layout design of deep submicron CMOS-circuits and at least 3+ years of recent experience on advanced nodes including FinFET technologies
- Experience leading complex layout macros during the full design cycle from floorplan analysis to completion of physical design verification
- Great understanding of CAD flows and tools related to analog/mixed-signal layout design

EDUCATION

Massachusetts College of Art
Bachelor's in Electrical Engineering

SKILLS

- Prior experience in layout generation
- Experience with Siemens EDA Calibre layout verification
- especially
- intronic and spoken
- Cadenceskills and
- engineering.

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FELTON HILPERT
4799 DEWEY HIGHWAY, HOUSTON, TX

PHONE
+1 (555) 239 7409

EXPERIENCE

Hagens and Sons -> 06/2019 – present
SAN FRANCISCO, CA // LAYOUT ENGINEER

- Strong layout knowledge with a minimum of 3 to 4 years of experience
- Skills include Cadence layout, Cadence schematic capture, using CALIBRE & Hercules verification tools
- Strong layout knowledge in submission process, e.g., 16nm, 10nm, 7nm, 5nm
- Experienced
- Experienced
- Good team in self-motivat

Bailey-Ferry
SAN FRANCISCO

- Strong debug and problem-solving skills for LVs, analog layout issues
- Experience in analog/mixed-signal layout
- Good team work and problem solving skills. Hardworking and self-motivated
- Entry level graduates with Bachelor's degree in Electronics and Electrical Engineering
- Familiarity with Cadence Virtuoso, Calibre dvfiles is
- Programming skills such as C++/Python/Verilog
- Experience designer in top level floorplanning and layout convergence activities
- Complete the physical layout design with the constraints of circuit design requirements

EDUCATION

Fashion Institute of Technology // Bachelor's in Electrical Engineering

SKILLS

- Solid Altiver specialization
- er and sales
- / processes and
- ig, project
- son
- ig technical
- customer meetings
- Professional experience in industrial environment, preferably in the construction business

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JAIME HANE

Information

Address
129 Highland Bypass, San Francisco, CA

Phone
+1 (555) 757 0918

EXPERIENCE

10/2019 – present
AUER WILDERMAN
Philadelphia, PA
Layout Engineer

- Create layout and holder's work plan based on architectural drawings and as
- Review purchase order with significant layout dates (PO Check)
- Support sales engineering regarding layout feasibility
- Support project manager and application engineer regarding layout

06/2013 – 06/2019
CREMIN-ZIEMANN
Philadelphia, PA
Layout Engineer

- AutoCAD Mechanical 2014, LintDesigner 2015, internal calculation tools, Building Information Modeling experience
- igital on top,

EDUCATION

LIM COLLEGE
Bachelor's in Electrical Engineering

SKILLS

- Create a system description when needed
- Transfer information about the solution to relevant functions in accordance with the Market to Order process, e.g. making a correct quotation for scope and price for the customer and according the relevant standards

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Stacy Osinski
635 Rachel Mountains, Detroit, MI

Mobile phone
+1 (555) 764 7609

EXPERIENCE

Layout Engineer – Bogan Group, Philadelphia, PA
07/2020 – Present

- Collect project technical info during startup and commissioning phase and provide quality feedback to the industry and Manufacturing facilities for improvement
- Experience in analog/mixed signal layout design of deep submicron CMOS-circuits and at least 3+ years of recent experience on advanced nodes including FinFET technologies
- Design the optimal layout solution for the customer

Layout En
– 06/2020

- For indu
- Experi
- Deliver r

EDUCATION

Savannah College of Art and Design – Bachelor's in Electrical Engineering


SKILLS

- Experienced in digital (standard cell, memory) layout

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How to Mention Achievements
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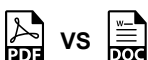
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1 Block Layout Engineer

Resume Examples & Samples

- ▶ Lead CAD validation studies using CATIA and VISMOCKUP
- ▶ 3+ years of experience in variation management componentry sub system assembly or manufacturing
- ▶ Proficient in desktop computer skills (Excel, Word, PowerPoint, Outlook)

2 Layout Engineer

Resume Examples & Samples

- ▶ Design physical layout of complex, high speed, low power CMOS circuits in deep sub-micron processes
- ▶ Be responsible for cell level, block level, PHY level floor planning, layout and integration
- ▶ Work with circuit design team to deliver quality layout design
- ▶ BSEE with 5+ years of mixed-signal layout with deep sub-micron ($\leq 40\text{nm}$) CMOS processes
- ▶ Familiar with Cadence Virtuoso, VXL and Calibre. Understanding of CMOS devices
- ▶ Be capable to learn new design rules for new processes
- ▶ High speed, low power mixed-signal CMOS layout experience is a plus. SKILL programming knowledge is a plus
- ▶ Must be a team player with good verbal communication skills, self-motivated, detail oriented, work with multiple functional teams and with good engineering practices

3 Analog Mixed Signal Layout Engineer

Resume Examples & Samples

- ▶ CMOS circuit design and technology (0.18 μm & 0.13 μm)
- ▶ Switched capacitor circuits
- ▶ Charge pumps and voltage multipliers
- ▶ Capacitive amplifiers
- ▶ Current sources
- ▶ Bandgap voltage references, voltage regulators (LDO), relaxation/feedback oscillators

- ▶ High performance feedback amplifiers, capacitance sensing interfaces,
- ▶ On-chip temperature sensors
- ▶ High resolution Sigma-Delta modulators
- ▶ A/D – D/A converters
- ▶ Experience with digital signal processing will be a plus
- ▶ Strong knowledge of analog design using Cadence tools, low noise, low voltage amplifier design, switched and cap filter design
- ▶ Experience in IC bench evaluation and validation
- ▶ Understanding of pop and click, ultra-low power design techniques
- ▶ Good interpersonal skills for cross functional work
- ▶ 10+ years of experience designing audio chips for handheld market
- ▶ B.S. or Masters degree in electrical engineering with emphasis on CMOS analog and Mixed signal design

4 **Layout Engineer** Resume Examples & Samples

- ▶ Full chip integration for memory chips and ADM's
- ▶ Full chip DRC verification
- ▶ Full chip LVS verification
- ▶ Define full chip signal routing methodology
- ▶ Define full chip voltage grids and power distribution
- ▶ Voltage and reference decoupling cap methodologies that work with signal, power, and fill requirements
- ▶ Floor plans of entire chips as well as subsystems
- ▶ Expert layout of logic, analog, and hierarchical systems
- ▶ Mastery of industry standard physical design and layout tools
- ▶ 5 years experience with semiconductor circuit layout
- ▶ 7 years experience with semiconductor circuit layout

5 **System Layout Engineer** Resume Examples & Samples

- ▶ Experience with computer-aided design (CAD) tools and programming concepts required
- ▶ Relentless attention to details; capability to meticulously follow complicated procedures
- ▶ Excellent communication skills paired with proven analytical and problem solving skills
- ▶ Dedication and energy to thrive in a high-pressure, fast-paced environment; adaptive to changing priorities

6 Systems Layout Engineer

Resume Examples & Samples

- ▶ Comfort with conceiving and executing complicated designs driven by state-of-the-art technology including software, hardware and robotics
- ▶ Skilled at project planning, comfortable using tools to manage milestones, deadlines, and process improvements
- ▶ Proven success as both an independent performer and a contributing member of a high-performing dynamic team
- ▶ Basic Understanding of programming (IE.: Java, C++, or Matlab), required

7 Senior Chip Top Layout Engineer

Resume Examples & Samples

- ▶ Designs full-custom IC layout design and verification, including analog blocks and whole chip level top layout
- ▶ Translates hierarchical schematics into layout with DRC LVS ANT ERC soft-check clean
- ▶ Be familiar with different foundry and different process
- ▶ Assists with tight tape-out schedules if needed

8 Senior Mgr Layout Engineer

Resume Examples & Samples

- ▶ Work close with circuit designers to optimize the floor plan
- ▶ Perform daily layout editing, DRC/LVS tasks to ensure the quality of the layout
- ▶ Employ efficient design methodologies to reduce the number of iterations and to deliver the product promptly
- ▶ Extremely familiar with layout editing tools, such as Virtuoso and Laker
- ▶ Highly proficient with DRC/LVS/ERC related tools and flows, such as Calibre, PVS (or IC Validator)
- ▶ Have extensive experience designing layout in deep sub-micron CMOS technologies, especially FinFET technologies

- ▶ Decent understanding in the issues of electro-migration and IR drop, RC delay, self-heating, capacitive cross-talk, etc
- ▶ Decent understanding in analog layout requirements, such as matching and shielding
- ▶ Knowledge in automatic P&R or chip-level floor planning / integration
- ▶ Decent Understanding in analog design methodologies, including the use of layout constraints
- ▶ Knowledge in performing RC extraction and EM/IR analysis
- ▶ Knowledge in CAD tool setup and maintenance
- ▶ Ability to generate pCell / pyCell to facilitate layout design
- ▶ Excellent communication skills and team spirit to work with members across multiple sites and functionalities
- ▶ Experience in designing layout for high-speed high-performance analog / mixed-signal circuits
- ▶ Have more than 15+ years' experience in analog/mixed signal layout design

9 Rfic Layout Engineer

Resume Examples & Samples

- ▶ 10+ years experience in custom RF/analog layout with extensive knowledge on deep subK micron CMOS (40nm, 28nm, etc.)
- ▶ Capability to lead other layout engineers for top level integration
- ▶ Knowledgeable on layout techniques for device matching, minimizing parasitics, RF shielding, and high frequency routing
- ▶ Must understand issues of RC delay, electro-migration, and cross capacitance
- ▶ Must understand guard rings, DNW, PN junctions, and advanced process effects such as LOD, WPE, etc
- ▶ Must recognize failure prone circuit and layout structures, proactively work with circuit designer for best approach to problems
- ▶ High level proficiency in interpretation of CALIBRE DRC, ERC, LVS, etc
- ▶ Knowledge of CADENCE layout tools
- ▶ Scripting skills in PERL or SKILL or AMPLE are considered a plus, but not required
- ▶ Excellent communication skills and able to work with cross-functional teams

10 Analog Layout Engineer

Resume Examples & Samples

- ▶ 3+ years analog layout experience in deep sub-micron processes (40nm, 28nm, etc.) RF layout experience is a plus
- ▶ Experience in floor planning and layout of analog blocks such as ADC, DAC, LDO, PLL, filters, etc
- ▶ Solid knowledge in device structures

- ▶ Understand tradeoffs in matching, coupling, parasitic effects, area, etc
- ▶ Understand causes and preventions of ESD and latch-up
- ▶ Proficient in interpreting verification DRC, LVS, ERC, ANT results
- ▶ Working knowledge of Cadence Virtuoso and Mentor Calibre preferred
- ▶ Team player with excellent communication skills

11 Rfic Layout Engineer

Resume Examples & Samples

- ▶ Positions are available for multiple experience levels
- ▶ The ideal candidate will have the following qualifications
- ▶ Experience in custom RF/analog layout with extensive knowledge of deep sub-micron CMOS (40nm, 28nm, FinFET, etc.)
- ▶ Knowledgeable in layout techniques for device matching, minimizing parasitics, RF shielding, and high frequency routing
- ▶ Must understand issues of RC delay, electromigration, and coupling
- ▶ For more experienced candidates
- ▶ Capability to lead other layout engineers for top-level integration
- ▶ Must recognize failure prone circuit and layout structures and proactively work with circuit designers for best approach to resolve problems
- ▶ Scripting skills in PERL or SKILL are considered a plus, but not required

12 Layout Engineer

Resume Examples & Samples

- ▶ Layout design delivery on time and quality
- ▶ Problem solving for Layout/PCB related technical issue
- ▶ Contribute to the innovation of product, design, way of working etc
- ▶ Contribute to the activities for the excellent operation
- ▶ More than 2 years' experience in layout design, have experience in Power Supply as plus
- ▶ Familiar with E-CAD tools, such as Cadence...
- ▶ Have knowledge in related technical areas, e.g. EMC, Safety, Thermal, Mechanical, Industry Standards as plus
- ▶ Have knowledge in cross function related areas, e.g. production, industrialization, PCB manufacturing as plus
- ▶ Capability of analyzing, problem solving and make prompt and clear decisions
- ▶ Can communicate in both English and Chinese
- ▶ Can be self-driving to complete the task

- ▶ Result and customer orientation
- ▶ Working proactively, effectively

13 Plant Layout Engineer

Resume Examples & Samples

- ▶ General engineer. Experience in one or several areas of engineering: civil engineering, piping engineering, mechanical, safety etc
- ▶ Good knowledge and understanding of general layout rules for an industrial project. Knowledge of the general operation of a nuclear power station and the associated safety aspects (in particular, aspects relating to flooding, fire, radiological protection, high energy line ruptures, etc.)
- ▶ Microsoft Word/Excel. Good knowledge of PDMS (or any 3D design software), Autocad 2D and Navisworks software (consultation)
- ▶ Fluent in English, French desirable

14 Layout Engineer Leader

Resume Examples & Samples

- ▶ You will be familiar with manual and automated Circuit/Layout design methods and tools used at Mellanox
- ▶ You will work closely with your design team on circuit implementation of your design
- ▶ You will be familiar with Design environment, flow, tools, methodologies and optimization methods used at Mellanox
- ▶ You will be exposed to leading technologies used in Interconnect IC design at Mellanox
- ▶ You will be familiar with the whole design process and be part of the team delivering leading Interconnect IC products
- ▶ At least 7 year experience in analog layout
- ▶ Management/leadership experience is an advantage

15 Layout Engineer

Resume Examples & Samples

- ▶ Engineer/Master of Science in Mechanical Engineering
- ▶ Professional experience in production areas (e.g. General Assembly), as well as in factory planning
- ▶ Organizational and negotiation skills, safe conduct as well as decision-making and enforcement
- ▶ Communication skills, team spirit and commitment
- ▶ International mobility or travel
- ▶ Good written and spoken English knowledge

- ▶ Good MS Office skills, AutoCAD skills

16 Industrial Simulation & Layout Engineer

Resume Examples & Samples

- ▶ Recent college graduate or Minimum of 5 years' experience including plant manufacturing experience
- ▶ Experience working with Simulation software Simul8, Delmia, Process Simulate, or other manufacturing simulation software
- ▶ Experience in work / production cell layout
- ▶ Strong Analytical, Problem Solving, Decision Making, Communication, Computer, and Interpersonal Skills
- ▶ Thorough Knowledge of Engineering Techniques and Plant Manufacturing Processes
- ▶ Must be able to Work Effectively at Various Levels of the Organization and with Outside Partners
- ▶ Ability to successfully interact on an international level
- ▶ Results Oriented
- ▶ Commitment to the highest ethical standards and willingness to adhere to Faurecia's Code of Ethics and Code of Management

17 Junior IC Layout Engineer for Industrial Product

Resume Examples & Samples

- ▶ Design the Product Layout starting from electrical schematics within process technology specific design rules
- ▶ Define and finalize various projects according to the deadline interacting with Design Engineering and Project Management
- ▶ Guaranteed compliance with technology design rules (DRC) and perform Physical Verification (LVS)
- ▶ Execute Layout Reviews and create proper documentation
- ▶ Execute Tape Out procedures and task, support or drive Mask Orders submissions
- ▶ Prepare packaging technical drawings and support feasibility analysis

18 Analog IC Layout Engineer, Harlow Near

Resume Examples & Samples

- ▶ BSc. in Electrical or Electronic Engineering is preferred. A minimum of two to four years industrial experience working on analog or mixed signal IC layouts
- ▶ A good working knowledge of Analog IC layout and verification tools
- ▶ Experience in "routing" using latest IC616 Virtuoso tools, i.e. wires, busses, pin-to-trunk, etc
- ▶ Experience in schematic driven layout connectivity, e.g. VXL/GXL

- ▶ Adherence to a formal layout methodology that is both robust and compatible with existing IP, thereby creating further re-useable IP blocks
- ▶ A “can-do” attitude and ability to meet deadlines, with a strong desire for success
- ▶ Written and verbal English language proficiency required

19 **Layout Engineer**

Resume Examples & Samples

- ▶ Make PCB layouts for automotive audio amplifiers according to specifications from HW developers
- ▶ Create pre-placement studies during RFIs/RFQs
- ▶ Create layouts with respect to good EMC and thermal properties
- ▶ Offer guidance to HW developers with respect to best practices for layouts
- ▶ Collaborate in the definition of the interfaces of several PCBs in a complex HW system
- ▶ Contribute to define a suitable PCB stack-up
- ▶ Assure adherence to company design rules
- ▶ Perform layout reviews
- ▶ Attend to schematic reviews
- ▶ Generate documentation for PCB production
- ▶ Master or Bachelor's degree in Electrical Engineering, Communications Engineering or a related technical discipline
- ▶ Deep knowledge in and experience with Mentor Expedition PCB SW + Constraint Editor
- ▶ Fundamental understanding of HW circuits and the properties relevant for PCB layouts
- ▶ Minimum of 6 years' experience in embedded real-time hardware development
- ▶ Experience with layout designs for high speed busses (impedance control)
- ▶ Experience in automotive industry is an advantage
- ▶ Good written and verbal communication skills both in German and English
- ▶ Flexible in terms of tasks and responsibility
- ▶ Self-motivated, passionate about audio and high sense of responsibility

20 **High Speed Layout Engineer**

Resume Examples & Samples

- ▶ BSEE/MSEE with 10+ years of relevant high speed layout products delivered into mass production
- ▶ Proven track record of performing formal analysis for achieving speeds of 20Gbps or higher for serial communication and state of the art speeds for parallel interface – e.g. DDR4, GDDR5, etc
- ▶ Excellent knowledge of Allegro design tools
- ▶ Proficiency in scripting – Bash, Python, PERL, etc

- ▶ Ability to perform SPICE simulations, IBIS Simulations, schematic entry, board bringup & debug, etc. a plus
- ▶ Proven track record of designing bringup boards with breakouts for measurement of high speed signals
- ▶ Strong hands-on skills in debug and simulation lab validation
- ▶ Demonstrated leadership in mentoring, training and coaching, including working with external vendors
- ▶ Excellent oral and written communication skills, especially at writing specifications

21 **Layout Engineer**

Resume Examples & Samples

- ▶ More than 3 years of related work experience
- ▶ Above associate's degree
- ▶ Fluent in English will be plus
- ▶ Big analog chip layout experience as a lead LD

22 **Senior Layout Engineer**

Resume Examples & Samples

- ▶ Experience with Cadence layout tool (virtuoso)
- ▶ Experience with Mentor Calibre verification tools
- ▶ Experience with Mentor PERC tool
- ▶ Good written and oral communication skills (English language)
- ▶ Good Analytical skills and being creative is plus

23 **Senior Layout Engineer**

Resume Examples & Samples

- ▶ Candidate must be familiar with analog CMOS development environment
- ▶ Block level ownership of layout, unit level verification, layout design reviews. Work closely with circuit designers to optimize the floor plan and layout for LDE/Parasitics
- ▶ Plan and schedule work within team to meet project milestones. Ensuring compliance with all checks at each stage of the design flow
- ▶ Active involvement in problem solving and implementing superior solutions as part of continuous improvement principle of Microchip
- ▶ Interaction with offsite counterparts specifically with our design centers located in USA and Hungary

24 **SI / Layout Engineer** Resume Examples & Samples

- ▶ Solid understanding of PCB technologies and the usage of EDA tools
- ▶ Thorough understanding of transmission line and microwave theories
- ▶ Integrity, insistence and team work spirits are needed

25 **Layout Engineer** Resume Examples & Samples

- ▶ Design multi-layer printed circuit board layouts incorporating the latest fabrication and assembly standards
- ▶ Collaborate with mechanical, design, fabrication, manufacturing and test engineers for a functional, cost effective layout
- ▶ Participate and provide input during design reviews at key points during the layout process
- ▶ Associate Degree in Electronics Technology or equivalent
- ▶ Understand how to layout digital, analog and power supply circuits
- ▶ Basic understanding of electrical schematic symbols and functions
- ▶ Ability to create dimensioned drawings for release
- ▶ Possess functional knowledge of IPC guidelines
- ▶ 3+ years of previous experience designing printed circuit boards, Mentor Graphics Expedition CAD software
- ▶ IPC CID (Certified Interconnect Designer – Basic) and CID+ (Advanced)
- ▶ Experience using Valor, SAP and GerbTool software

26 **Rfic Layout Engineer** Resume Examples & Samples

- ▶ During the design phase you will work closely with design engineers creating the layout of RFIC circuit blocks/subsystems (e.g. LNA, mixer, VGA, driver, VCO, PLL) in modern CMOS technologies and checking them via DRC, ERC, LVS etc
- ▶ After design finalization you perform the tape out, which includes ordering the production masks and checking them for correctness (JDV)
- ▶ You will also create the bonding diagram for embedding the IC into the package
- ▶ During the mass production phase of the product you might be called upon to support failure analysis of FARs

27 **Layout Engineer**

Resume Examples & Samples

- ▶ Mechanical or electrical engineering education
- ▶ Skills and knowledge about CAD engineering systems
- ▶ Basic office and ERP usage skills
- ▶ Good written and spoken English, other languages are benefit

28 **IC Layout Engineer**

Resume Examples & Samples

- ▶ BS in Electrical Engineering or similar. Equivalent experience gained through work projects may be acceptable
- ▶ At least 5 year experience in IC Layout
- ▶ Fundamental knowledge of digital/analog layout flows
- ▶ Writing IC layout rules (LVS,DRC,ERC) would be a plus
- ▶ Experience with Place & Route CAD tools and approaches
- ▶ Demonstrated analytical and systematic teamwork approach to troubleshooting
- ▶ Due to Government requirements, candidate must be a U.S. Citizen with the ability to obtain and maintain a security clearance

29 **Plant Layout Engineer**

Resume Examples & Samples

- ▶ Nuclear experience needed with experience of Layout, Engineer/Chartered Engineer level with significant experience
- ▶ Experience in one or several areas of engineering: civil engineering, piping engineering, mechanical, HVAC, safety etc
- ▶ Good knowledge and understanding of general layout rules for an industrial project
- ▶ Knowledge of the general operation of a nuclear power station and the associated safety aspects (in particular, aspects relating to flooding, fire, radiological protection, high energy line ruptures, etc.)

30 **RF Layout Engineer**

Resume Examples & Samples

- ▶ Bachelor of Electronic Engineering (Minimum Level 7)
- ▶ 5 - 7 years experience in a layout role at cell, block and full chip level

- ▶ Proficient user of Cadence suite of layout tools (Composer, Virtuoso, Virtuoso-xl, VCR) and verification tool
- ▶ Skilled in digital implementation with experience in Synopsys tool suite (Design Compiler, IC Compiler, PrimeTime, Formality, PrimeRail, Hercules, etc.)
- ▶ Solid understanding of ESD, Latch-up, mixed signal routing and isolation
- ▶ Knowledge of Unix and Linux preferred
- ▶ Analog circuit layout experience and/or place and route
- ▶ Self motivated with good communication and problem solving skills are necessary
- ▶ Ability to work on own initiative and follow-through to ensure results
- ▶ Interest and proven ability in mentoring/teaching as well as team leadership

31 Integrated Circuit Virtuoso Layout Engineer

Resume Examples & Samples

- ▶ Generate Virtuoso layouts for Process Control Monitor (PCM) structures with guidance from process development engineers
- ▶ Generate Virtuoso layouts for alignment marks with guidance from photo lithography engineers
- ▶ Generate Virtuoso layouts for physical measurement structures with guidance from process development and photo lithography engineers
- ▶ Generate Virtuoso schematics and layouts for test circuits that are sub-circuits of larger integrated circuits with guidance from design engineers
- ▶ Participate in reticle composition and tapeout support activities
- ▶ Aid in troubleshooting related to all of the above
- ▶ Create and document flows for future re-use and quality control
- ▶ Bachelor's degree in a technical area (BSEE or other Engineering discipline preferred) with 5 years of relevant experience. Relevant Master's level coursework or projects will be considered in lieu of relevant work experience (relevant MS with 3 years of experience)
- ▶ Demonstrated ability to script capabilities within the Virtuoso environment using one of several compatible scripting languages
- ▶ Experience using Cadence Virtuoso to layout Integrated Circuits, perform Mask Layout, Full Custom Layout and/or draw structures used typically in a Microelectronics Foundry environment
- ▶ Knowledge of semiconductor device physics, process development and/or manufacturing
- ▶ Experience using Cadence Virtuoso Schematic Editor to create circuits
- ▶ Solid knowledge of DRC/LVS/PEX within Cadence DIVA, Assura or Mentor Graphics Calibre
- ▶ Solid interpersonal and team skills for cross-functional collaboration. High attention to detail and ability to self-check work outputs
- ▶ Must be able to obtain and maintain a DoD TS/SCI clearance (U.S. Citizenship is a prerequisite for this)
- ▶ Bachelor's degree in a technical area (BSEE or other Engineering discipline preferred) with 9 years of relevant experience. Relevant Master's level coursework or projects will be considered in lieu of

relevant work experience (relevant MS with 7 years; 4 years with a PhD)

- ▶ Solid interpersonal and team skills for cross-functional collaboration. High attention to detail, ability to self check work outputs and ability to lead technical projects
- ▶ Knowledge of Layout XL/GXL capabilities that enhance layout task efficiency
- ▶ Knowledge of analog/mixed signal integrated circuit design and testing
- ▶ Experience taking lab measurements on process control monitor (PCM) test structures, interpreting results from automated testing of those structures or modeling
- ▶ Experience utilizing the spectre simulator to verify models match measurements
- ▶ Experience laying out digital standard cells and memory elements or characterizing standard cells and memories
- ▶ Experience with Process Design Kit (PDK) Development (techfiles, verification rulefiles, p-cells)

32 Concept & Layout Engineer

Resume Examples & Samples

- ▶ Optimise the wind farm layout, the conceptual technical design and the installation setup to improve the technical solution and business case
- ▶ Analyse and coordinate internal stakeholders and occasional external stakeholders in relation to the technical design envelope and consent processes
- ▶ Analyse different wind farm scenarios by combining WTG's, foundation concepts, positioning of substations, turbines and array cables in close cooperation with the project managers, engineering leads and consent managers for each area
- ▶ Perform technical scope management and coordinate technical interfaces
- ▶ Coordinate, challenge and ensure alignment across all case drivers, including technical specifications, CAPEX, OPEX, ABEX, yield and risk
- ▶ Preferably, have a master's degree in engineering and have experience with offshore wind farms or offshore works within the fields of wind turbines, electrical systems or offshore installation processes
- ▶ Have good analytical understanding of the cross disciplinary effects between the technical solutions and the business cases
- ▶ Are able to work with many stakeholders and have a strong personal communication style
- ▶ Are very proactive by nature and your drive to create results are visible and proven from previous positions
- ▶ Have the desire to use your specialist competences in a project development environment where you will play a key role in ensuring that our conceptual design of the wind farms is challenged and secured throughout the development process
- ▶ Speak and write English fluently
- ▶ Thrive in an international environment and are able to create good relationships with your stakeholders

33 Senior Layout Engineer

Resume Examples & Samples

- ▶ Experience in using latest Virtuoso tools
- ▶ An appreciation of parasitic related issues and ability to layout circuits to minimize coupling issues
- ▶ A good working knowledge of constraints-driven layout is useful but not essential
- ▶ Able to use OCEAN or SKILL to facilitate the analog layout process
- ▶ LI-LS1

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Layout Engineer

Resume Examples & Samples

- ▶ During the design phase you will work closely with design engineers creating the layout of analog circuit blocks/subsystems in modern CMOS technologies and checking them via DRC, ERC, LVS etc
- ▶ You will also create the bonding diagram for embedding the IC into the package
- ▶ During the mass production phase of the product you might be called upon to support failure analysis of FARs

35

Photonics Layout Engineer

Resume Examples & Samples

- ▶ Design complex layouts for silicon photonic chips
- ▶ Design test structures for process control and process tolerance monitoring
- ▶ Add to a growing building block library based on process flows and design rules
- ▶ Perform design rule checks (DRC) for design verification
- ▶ Bachelor's degree in related field or highly relevant experience in integrated photonics and devices
- ▶ Minimum of 10 years industrial experience
- ▶ Proven ability to deliver results under tight deadlines
- ▶ Enthusiasm for new challenges, hard-working and flexible
- ▶ Scripting for layout design automation
- ▶ Basic knowledge of silicon photonics is considered a plus
- ▶ Basic knowledge of electrical circuitry

36

Layout Engineer

Resume Examples & Samples

- ▶ Create state-of-the-art analog IC layouts
- ▶ Create transistor level sub block layout, based on schematics provided by designers (including careful analog considerations)

- ▶ Runfull verification sequencesusing advanced EDA tools
- ▶ Perform chip floor planning, power/clock distribution
- ▶ Participate in establishing CAD and physicaldesign methodologies

37 **Frame / Layout Engineer**

Resume Examples & Samples

- ▶ Use or customize internally developed software code and commercially available software tools to generate documentation as well as numerical files that drive automation within our Fabs and Mask House
- ▶ Help communicate inputs and assess progress to our project schedules
- ▶ Participate in meetings with peer Frame teams located in the US and Singapore
- ▶ Bachelor's Degree in Electrical Engineering, Computer Engineering, Material Science or Semiconductor Physics with a minimum of 0-2 years of relevant experience
- ▶ Master's Degree with a minimum of 0-2 years of relevant experience
- ▶ 1 year of experience using Cadence Virtuoso with DRC or LVS or an equivalent layout tool
- ▶ Knowledge of Cadence K2 Mask Compose commercial software
- ▶ Knowledge of coding software (C++), populating databases (Oracle, DB2) and familiarity with LINUX operating system
- ▶ Knowledge of tape-out, new product introduction and semiconductor fab setup in an area such as mask data preparation, inline metrology, reticle construction and manufacturing, testchips, reticle frame building, OPC or mask manufacturing
- ▶ If you need a reasonable accommodation for any part of the employment process, please contact us by email at usaccommodations@globalfoundries.com and let us know the nature of your request and your contact information. Requests for accommodation will be considered on a case-by-case basis. Please note that only inquiries concerning a request for reasonable accommodation will be responded to from this email address

38 **Senior Asic Mask / Layout Engineer**

Resume Examples & Samples

- ▶ Responsible for mask design (layout) of cell level circuits, including drivers, buffers, custom standard cells, some mixed signal blocks
- ▶ Responsible for some amount of mixed signal layout (as needed)
- ▶ Responsible for chip level integration tasks, including pad ring creation, ESD install, top level block integration and routing, top level clock routing, layout database management and archiving, final chip metal dummy fill, final DRC / LVS checks, chip release tasks, including GDS2 file creation and release

39 Serdes Layout Engineer

Resume Examples & Samples

- ▶ Responsible for the layout of high speed SerDes blocks
- ▶ Need to work closely with layout leads and deliver the layout in scheduled time
- ▶ Should be willing to put extra effort in learning the ever increasing layout complexities
- ▶ Quick and smart execution is key
- ▶ Need to come up with ideas to improve the flow and introduce automation techniques
- ▶ 3+ years experienced in SerDes, or Analog and Mixed Signal Layouts -Should be experienced in 28nm and lower nodes -Should be very strong in debugging and logical thinking -Need to be very thorough in analog layout techniques like device matching, shielding, differential pair matching, current mirrors etc - Good to be familiar with SKILL

40 IC Layout Engineer

Resume Examples & Samples

- ▶ Design(i.e. create) the Product Layout starting from electrical schematics within process technology specific design rules
- ▶ Identify best cost-effective and performance-effective solution working in team with design engineers
- ▶ Execute specific working packages according to the deadline interacting with Design Engineering and Project Management
- ▶ Guarantee compliance to technology design rules (DRC) and perform

41 RF Cmos Layout Engineer

Resume Examples & Samples

- ▶ Design the product layout starting from electrical schematics within process technology specific design rules
- ▶ Identify best cost-effective and performance-effective solution working in team with design engineers
- ▶ Execute specific working packages according to the deadline interacting with Design Engineering and Project Management
- ▶ Guarantee compliance to technology design rules (DRC) and perform Physical Verification (LVS) as well as support post-Layout verification
- ▶ Execute Layout Reviews and create proper documentation
- ▶ Execute Tape Out procedures and task, support or drive Mask Orders submissions
- ▶ Prepare packaging technical drawings and support feasibility analysis
- ▶ Cooperate with the development team on continuous improvement activities (methodologies, checklist, working instructions) and contribute to Technology and Design Methodology improvements

42 Senior Piping & Layout Engineer

Resume Examples & Samples

- ▶ To assist the Lead or Principal engineer in meeting project requirements and performing all technical duties in a highly competent and efficient manner
- ▶ Assist in the preparation of CTR's and man-hour estimates via the Aker Integrated Management System (AKIMS) where applicable
- ▶ Must be able to perform offshore surveys
- ▶ Execute technical duties in a competent and professional manner and in accordance with company procedures
- ▶ Ensure work is completed on Schedule and within budget
- ▶ Review and check the work of others
- ▶ Provide engineering and technical direction for drawing office personnel
- ▶ Overall responsibility for the delivery of multi-discipline and or single discipline engineering modifications / project scope of works within a contract or a project
- ▶ Manage the defined scopes of work provided by the contact / project management team ensuring that the discipline scopes of work are fully defined and in accordance with the client's requirements
- ▶ Familiar with the aspects of Pipe Stress Analysis
- ▶ Educated to HNC/HND/Degree level in engineering discipline
- ▶ Chartered or Incorporated Engineer
- ▶ Sound working knowledge of relevant industry codes and standards
- ▶ Conversant with appropriate technical software
- ▶ Aware of latest technical developments
- ▶ Current Offshore Survival and Medical Certificate essential
- ▶ Ability to direct and guide engineers and designers
- ▶ Effective written and verbal communication skills
- ▶ Good team working skills

43 Senior Analog / RF Layout Engineer

Resume Examples & Samples

- ▶ >15+ years of experience leading Analog/RF layout activities in complex ICs
- ▶ Strong expertise in Analog and RF layouts, device physics and IC ESD protection strategies
- ▶ Expert in advanced silicon technologies like 40nm, 28nm and/or beyond
- ▶ Expert in layout design tools like Cadence Virtuoso (PVS) and Mentor Graphics (Calibre)
- ▶ Experience in physical implementation in Analog/RF blocks at IPs and/or SOC level
- ▶ Experience with cross functional teams and good communication skills to operate in a global environment with multiple partners in design, test, program management, quality department

44 Analog IC Layout Engineer

Resume Examples & Samples

- ▶ 5+ years' experience in analog integrated circuit layout
- ▶ Solid knowledge of industry standard layout conventions and rules for reducing layout risk
- ▶ Proficiency with Cadence layout as well as Cadence and Mentor Graphics verification and extraction
- ▶ Analog circuit layout
- ▶ Analog circuit design knowledge is a plus
- ▶ Experience in the layout of ADCs, DACs, RF, PLLs, LDOs, Bandgaps
- ▶ Experience in isolated processes for high-voltage and switching power regulators
- ▶ Mixed-signal chip assembly

45 Senior Analog Layout Engineer

Resume Examples & Samples

- ▶ >10+ years of experience leading Analog layout activities in complex ICs
- ▶ Strong expertise in Analog layouts, device physics and IC ESD protection strategies
- ▶ Expert in advanced silicon technologies like 90nm and/or beyond
- ▶ Expert in layout design tools such as Cadence Virtuoso (OA, PVS) and Mentor Graphics (Calibre)
- ▶ Ability to drive and collaborate with experienced people having different technical profiles
- ▶ Ability to manage and drive a multisite layout team
- ▶ Experience in using the Mixed Signal on Top flow (MSoT)
- ▶ Experience in delivering advanced floorplan strategies
- ▶ Experience in physical implementation in Analog blocks at IPs and/or SOC level
- ▶ Ability to leverage his expertise to provide training, support and write guidelines focused on layout activities
- ▶ Experience with cross functional teams and excellent communication skills to operate in a global environment with multiple partners in design, test, program management, quality department

46 Layout Engineer

Resume Examples & Samples

- ▶ Leaf cell memory design for memory compilers with proper understanding of tiling requirements to assemble memory such as connection through abutment, pins connecting from leaf to leaf at boundary, DRC on any number of adjacent cell combinations to ensure no DRC violations in leaf cell usage in compiler
- ▶ Simple to complex Standard cell layout design, abutment checks, P & R compatibility
- ▶ Floor planning, architecture definition and physical layout implementation against the Schematic design

of Standard cells

- ▶ Validating the layout for DRC (design rule), LVS (Layout versus schematic), DFM (design for manufacturability) ERC (electrical rule) ORC (optical rule) EM /IR (electro migration and IR drop) checks
- ▶ Good understanding of usage of standard cells in P & R and proficiency in P & R flow is desirable
- ▶ Any scripting language proficiency is also desirable
- ▶ Provide reasonably accurate estimates of timescales for work

47 Principal Plant Layout Engineer

Resume Examples & Samples

- ▶ **Technical Design Ability** -Responsible for setting the project design basis for plant layout and piping design, influential in setting the layout concept and approving the developed design. Would be expected to be developing an interest in a specialist industry area (e.g. upstream, midstream, downstream, modularisation). In addition has thorough knowledge of all aspects of plant layout and piping design. Takes a hands-on and lead role with responsibility for plant layout and piping design in an assigned area including; setting plant layout concepts, assuring quality and consistency and ensuring that safety, operation, maintenance and construction requirements are incorporated. Maintain a cost focussed approach to plant layout and piping design such that installed and operational costs are minimised, whilst also ensuring that safety, operational, maintenance and constructability requirements are appropriately addressed supported with sound documented reasoning
- ▶ **Technical Expertise** -A respected member of the group, who is securely confident in their discipline. Experienced in setting a structured design basis, undertaking the conceptual plant layout and piping design, production of project standards and well-structured narrative. Proven track record in leading the conceptual phases of the plant layout, piping design and production effort. Confident in undertaking plant layout in critical and novel plant areas
- ▶ **Technical - Design Basis** - Sets project layout design basis, produces project standards and assures design basis is maintained through subsequent phases through well-structured narrative. Identifies, quantifies and produces project specific piping technical instructions for use by the piping and layout design team to achieve technical consistency and quality in plant layout and piping design

48 Layout Engineer

Resume Examples & Samples

- ▶ Experience: 5+ year in analog layout (full chip layout)
- ▶ Degree in electronics or electrical engineering
- ▶ Knowledge of design and verification tools (Cadence, Mentor, Calibre)
- ▶ Knowledge of tapeout procedures
- ▶ Knowledge in analog layout (matching structures), power routing, latch-up, ESD layout, area optimization
- ▶ Basic knowledge of circuit functionality (eq: comparators, bandgaps, amplifiers)

- ▶ Good communication skills, understand expectations and requirements of a project)
- ▶ Known Languages: English

49 Serdes Analog Integrated Circuit Layout Engineer

Resume Examples & Samples

- ▶ Interlock across the entire design team to drive solutions and resolve problems
- ▶ At least 8 years of ASIC analog layout design experience with a focus on analog and mixed signal designs
- ▶ Deep Experience with layout in the Cadence Design Environment
- ▶ Familiarity with Virtuoso XL
- ▶ Experience must include floor planning
- ▶ Experience includes ASIC Rule generation (GDS, LEF), and able to run checking such as LVS & DRC, YCD, & PIC
- ▶ Experienced with Electro migration and voltage drop analysis
- ▶ Ability to recognize critical signal nets and reduce parasitics by proper floor planning/placement
- ▶ Excellent communication skills and ability to work within a tightly-coupled team are a must

50 Senior Layout Engineer

Resume Examples & Samples

- ▶ Experience in analog IC layout skills, like bandgap voltage reference, devices matching and ESD/Latchup knowledge
- ▶ Experience in Cadence IC Layout tool set
- ▶ Team-based, cross-functional organizational structure experience preferred
- ▶ Experience in high current, high voltage circuit layout, high accuracy Opamp is a plus
- ▶ Chip Layout experience is a plus
- ▶ BS degree or equivalent experience

51 Plant Layout Engineer

Resume Examples & Samples

- ▶ Degree qualified in appropriate technical discipline
- ▶ Experience level: Engineer, Chartered Engineer
- ▶ Technical skills: Good knowledge and understanding of general layout rules for an industrial project. Knowledge of the general operation of a nuclear power station and the associated safety aspects (in particular, aspects relating to flooding, fire, radiological protection, high energy line ruptures, etc.)

- ▶ Software and tools: Microsoft Word/Excel. Good knowledge of PDMS (or any 3D design software), Autocad 2D and Navisworks software (consultation)
- ▶ Language(s):Fluent in English, French desirable

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