ASIC Engineer

Writing a great asic engineer resume is important because it is one of the first things a potential employer will see when they are considering you for a position. It is your opportunity to make a good first impression and sell yourself as the best candidate for the job.

If you're looking for inspiration when it comes to drafting your own asic engineer resume, look no further than the samples below. These resumes will help you highlight your experience and qualifications in the most effective way possible, giving you the best chance of landing the asic engineer job you're after.

Resume samples

Precilla Garciamorales

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Summary

I have over 4 years experience as an ASIC Engineer. I have a strong background in electrical engineering and computer science. I am experienced in the design, layout, and verification of digital integrated circuits. My work has involved developing high-speed interfaces, mixed-signal circuitry, and power management techniques. In addition to my technical skills, I am also skilled at project management and team collaboration.

Experience

ASIC Engineer at LSI Corporation, IA **May 2022 - Present**

- Designed and implemented an 8-bit microprocessor in Verilog that could perform basic arithmetic operations with a clock speed of 4 MHz.
- Implemented a pipelined MIPS processor in Verilog with support for forwarding, branch prediction, and data hazard detection/ avoidance. The design achieved a throughput of 5 instructions per cycle.
- Developed C++ models of various digital filters (IIR & FIR) and verified the functionality using SystemC simulations against RTL implementations.
- Designed & simulated high-speed (>10Gbps) serial links such as PCIe, DisplayPort, HDMI using SerDes IPs.
- Analyzed power consumption at different process corners (TT/FF/SS) across multiple voltage domains in 45nm node SoC designs.

Associate ASIC Engineer at Texas Instruments, IA **Aug 2018 - Mar 2022**

- Designed and implemented an 8-bit RISC microprocessor in Verilog RTL, which achieved a clock speed of 100MHz.
- Implemented a design using the processor that met all timing constraints with zero hold time violations.
- Developed test benches and directed vector generation to achieve 95% code coverage on the designs.
- Wrote C programs to verify correct operation of hardware designs through simulation.
- Generated reports on project status, risks and issues for management review every two weeks.

Education

Bachelor of Science in Electrical Engineering at Iowa State **Sep 2014 - May 2018**

University, Ames, IA
Some skills I've learned are: circuit analysis, electronic device characterization, semiconductor device physics, and device fabrication process.

Skills

- VHDL
- Verilog
- FPGA design and implementation
- ASIC design and verification
- Static timing analysis (STA)
- Logic synthesis
- Physical design

Asiyah Mutuc

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Summary

A highly experienced ASIC Engineer with over 4 years experience in the industry. I have gained a strong reputation as an engineer who delivers high quality work on time and within budget. My skills include Verilog, VHDL, SystemVerilog, Perl/Python scripting and TCL/Expect programming. I am also well-versed in using synthesis tools such as Synopsys Design Compiler, Cadence NC-Verilog and Mentor Graphics ModelSim for functional verification of RTL designs. In addition to this, I possess excellent communication skills which allow me to effectively communicate complex technical concepts to both engineering and non-engineering teams alike

Experience

ASIC Engineer at Analog Devices, GA **Apr 2022 - Present**

- Implemented an ASIC design that improved system performance by 10%.
- Reduced power consumption of the ASIC by 15%.

- Increased yield from 75% to 95%.
- Developed new methodology that increased productivity by 25%.
- Achieved first pass success rate of 97.5%.

Associate ASIC Engineer at Maxim Integrated, GA **Aug 2018 - Mar 2022**

- Successfully designed, implemented and verified RTL for multiple high-speed communication IPs including Ethernet, PCIe and USB.
- Achieved 2.5X performance improvement over previous generation design while meeting all timing closure criteria.
- Reduced power consumption by 10% in latest generation design through innovative clock gating strategy across entire SoC.
- Successfully led team of 4 engineers in block level verification & sign-off for next generation product silicon.
- Presented detailed analysis to senior management on root cause of critical defect discovered post tapeout.

Education

Bachelor of Science in Electrical Engineering at Georgia Institute of Technology **Sep 2014 - May 2018**

I've learned how to design, analyze, and troubleshoot electrical and electronic circuits and systems.

Skills

- VHDL
- Verilog
- SystemVerilog
- UVM/OVM methodologies
- Scripting languages (Python, Perl, TCL)
- HDL simulators (QuestaSim, Modelsim)
- Logic synthesis tools (Synopsys Design Compiler, Mentor Graphics Precision RTL Synthesis)

Related Resume Samples

- ASIC Design Engineer
- ASIC Verification Engineer
- Engineering Project Manager
- Engineering Program Manager
- Engineering Teacher
- Engineering Assistant

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