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Practical chip-centric electro-thermal simulations

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Abstract

Full-chip dynamic electro-thermal simulation is achieved by coupling a circuit simulator and a thermal solver. By letting both simulations run with their specific time-step, a higher computational efficiency is achieved. A scheduler synchronizes temperatures in the circuit simulator and dissipation patterns in the thermal solver on an 'as-necessary' basis. The 3D geometry for the thermal solver is generated automatically from the layout data-base and cross-referenced to the netlist to allow automatic extraction of power-dissipation from circuit simulations. In order to obtain realistic thermal responses for smart-power chips containing large driver transistors, it is essential to define the boundary conditions appropriately and account for package and PCB transients. To do so, the simulation domain is extended to cover the full package body, and uniform boundary conditions are defined to account for the thermal impedance of the PCB and for convection and radiation. Validation results are shown for the case of an SOIC package. Work is on-going on QFN and other power-packages.

Introduction

As the advancements in smart-power IC technology produce higher performance power transistors, the density of power dissipation on-chip is increasing pushing up junction termperatures to higher levels. This trend is further enhanced by increasing requirements for high ambient temperatures. As a result the temperature head-room between the peak junction temperatures reached on-chip and the maximum allowable temperatures dictated by reliability requirements is reducing, calling for ways to more accurately evaluate static and dynamic temperature distributions. Hence, electro-thermal simulation capability is becoming more and more necessary for the design of smart-power IC's.
Solutions enabling the electro-thermal simulation of IC's can be split in three categories as shown in Figure 1 : (a) those implementing a thermal network in an electrical circuit simulator, eg. [1]-[2], (b) those incorporating an electrical behavioral model in a thermal simulator, and finally, (c) those coupling an electrical and a thermal simulator, [3]-[5].

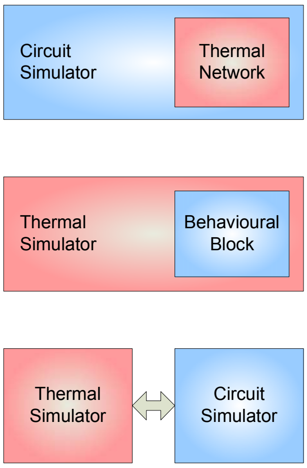

FIGURE 1 : ARCHITECTURES FOR ELECTRO-THERMAL SIMULATION SCHEMES

The main drawback of the inclusion of a thermal network in a circuit simulator is the fact that both networks will be solved with the same-time step, although the thermal network contains time-constants which are several order of magnitudes larger than the time-constants of the electrical part.
On the other hand, the generation of electrical behavioral models to be used as dissipation sources in a thermal simulator is a difficult task and currently still a field of research.
In this paper, the method used is therefore to achieve efficient electro-thermal simulation is the loosely coupling of a full-chip thermal solver (CircuitFire™ , [6]) and a circuit simulator (Spectre™ or Ultrasim™, [7]).

Electro-thermal Simulation Scheme

The dynamic electro-thermal simulation scheme we implemented is inspired from the early work of Van Peteghem et al, [4]. In order to interface with standard circuit simulators, the time-axis of the transient simulation is divided in critical intervals. The time-varying temperatures computed by the thermal solver for a given interval are approximated in the circuit simulator by equivalent constant values which are computed for every device in the layout, and passed to the

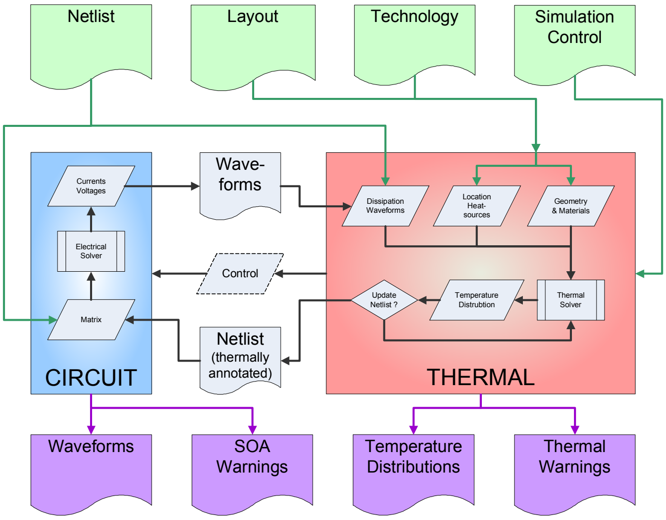

FIGURE 2 : FLOWCHART OF THE LOOSELY COUPLED ELECTRO-THERMAL SIMULATION SCHEME

device instances using the standard parameter 'TRISE'. The circuit simulation proceeds in segmented runs, one per critical time-interval, whilst temperature and power dissipation data are exchanged between the thermal solver and the circuit simulator at the end of each critical time interval. The length of the critical time-intervals is adapted automatically in order to keep the offset between the discretized temperatures in the circuit simulator and their continuous counter-parts in the thermal solver bounded below a user-defined value.

Figure 2 shows the general data-flow of our simulation scheme. The 3D model required by the thermal solver is built automatically from the layout data-base of the complete chip using a description of all layers, including packaging materials such as mould, die-paddle, bond-wires, etc. The layout-versus-schematic data-base can be used to extract the mapping between heat-source geometries and transistor instances in the netlist, such that automatic extraction of power dissipation from the circuit simulation is achieved.

Boundary Conditions for the Dynamic Case

In order to be able to realize accurate simulations for transients lasting longer than a few milliseconds, it is important to define good thermal boundary conditions on the simulation domain. In this work two approaches were compared : (a) one where the boundaries of the simulation domain are coinciding with the edges of the die, (b) one where the simulation domain is extended to include the package body (the mould compound and eventual exposed-pads).

Inside CircuitFire, the boundary conditions are formulated for each face S_i with uniform h_i and c_i parameters as shown in the following equation where ϕ is the flux density :

$$\varphi(\vec{r}_i)=h_i\cdot(T(\vec{r}_i)-T_A)+c_i\cdot\frac{dT(\vec{r}_i)}{dt} \quad \text{with } \vec{r}_i\in S_i \qquad (1)$$

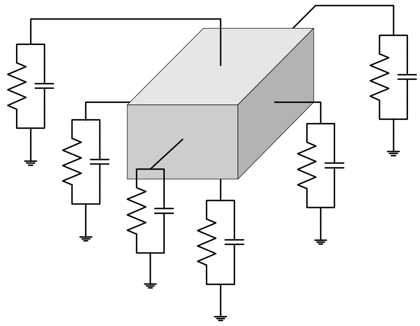

FIGURE 3 : THE BOUNDARY CONDITIONS SCHEME IN THE GRADIENT THERMAL SOLVER (CASE WHERE THEY COINCIDE WITH DIE EDGES)

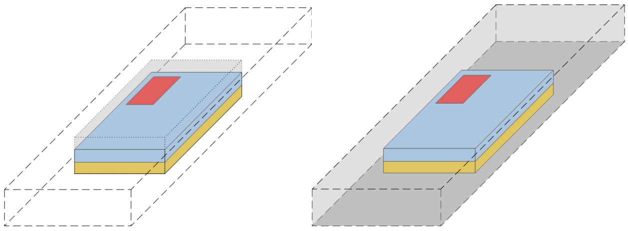

FIGURE 4 : ALTERNATIVE STRATEGIES TO LOCATE THE BOUNDARIES OF THE SIMULATION DOMAIN (SEMI-TRANSPARENT GRAY BOX)

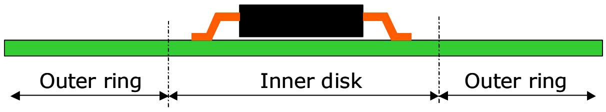

FIGURE 5 : PARTITIONING STRATEGY TO GENERAT THE PCB MODEL

During a transient simulation, when a strong power source is present close to the border of the die and one attempts to apply the boundary conditions at the edges of the die, it is not possible to a obtain satisfactory evolution of the temperature distribution over time. Indeed, the presence of the heat source close to the boundary causes on outward heat-flux into the mould compound which diffuses laterally and heats up that material in a way that can not be accounted by the uni-dimensional type of heat transfer model realized in equation (1). However applying the boundary conditions at the edge of the moulding compound, as shown on the right-hand side of Figure 4, yields much better results and allows to predict temperature distributions which are in much better agreement with measured result, as is shown in the next section.

In typical package configurations, the thermal paths leaving the die pass either via the PCB or go directly into the air. We are developing a compact modeling technique allowing to quickly generate boundary conditions for the PCB interface of our electro-thermal simulation framework from a small set of structural parameters. To do so the PCB is divided into an inner disk comprising the immediate vicinity of the package and an outer ring for which the cylindrical symmetry allows to build a simple analytical thermal resistance model, [8]. To build a model for the inner disk, a design-of-experiment was conducted varying PCB and package parameters in order to obtain thermal resistance values in function of structural parameters using the MSC.Mark™ thermal solver.

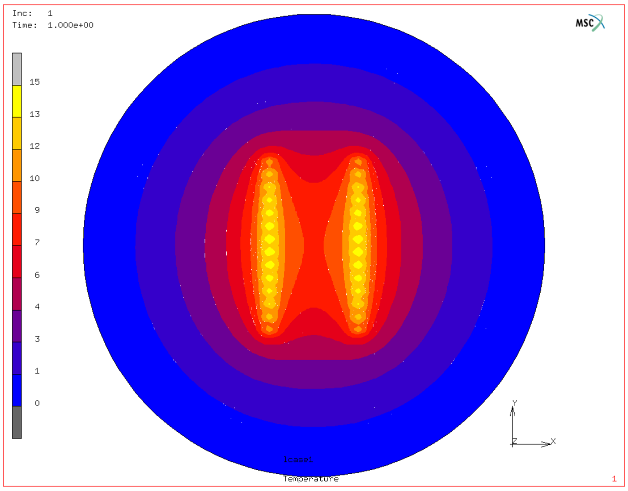

FIGURE 6 : TYPICAL TEMPERATURE DISTRIBUTION SIMULATED FOR THE FOOTPRINT OF A LEADED PACKAGE ON PCB

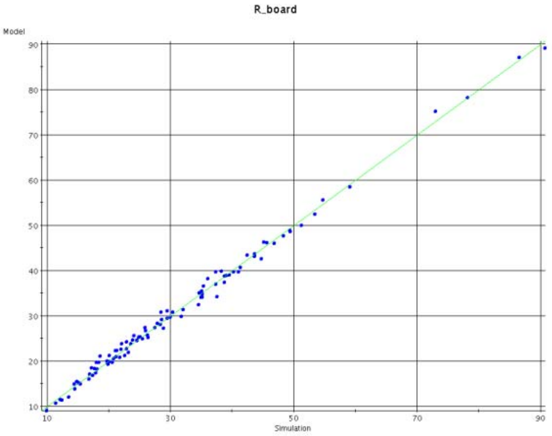

FIGURE 7 : VALIDATION OF THE RSM FOR THE RTH OF THE INNER DISK (X-AXIS : FEM RESULT, Y-AXIS : RSM RESULT)

The most significant parameters P_i (Table 1) were identified and used to build a 2^{nd}-order response surface model (RSM) to predict the transfer resistance R_{tfr} from the package to the outer ring using the generic equation shown below :

$$R_{tfr} = a_0 + \sum_k b_k P_k^{-1} + \sum_{i \neq j} c_{i,j} P_i^{-1} P_j^{-1} + \sum_l d_l P_l^{-2} \qquad (2)$$

Figure 7 shows the good fit of the RSM model to the simulated data. Combining the model proposed by R. Stout [8] and the transfer resistance computed using our RSM and a contribution for the convection on the back-side of the PCB, an equivalent thermal resistance value is obtained that can be plugged into the boundary conditions model of CircuitFire to account for the thermal paths running via the PCB.

To complete the thermal model, the thermal capacitance of the inner disk is computed and added to the boundary conditions model. This simple model is sufficient to cover static and dynamic electro-thermal simulations in the case of events which do not last longer than a couple of seconds.

Param. P_i	**Description**	**Range**
Kxy	Equivalent in-plane PCB conductivity	5 – 25 W/mK
Kz	Equivalent transversal PCB conductivity	0.25 – 0.7 W/mK
H	Convection coefficient	1 – 25 W/m²K
Heq	Interface conductivity coef. for outer ring	100 – 2500 W/m²K
T	PCB thickness	0.8 – 2.5 mm
P	Lead pitch	0.5 – 1.5mm
N	Number of leads	12 – 64

TABLE 1 : SIGNIFICANT PARAMETERS USED TO BUILD THE RESPONSE SURFACE MODEL

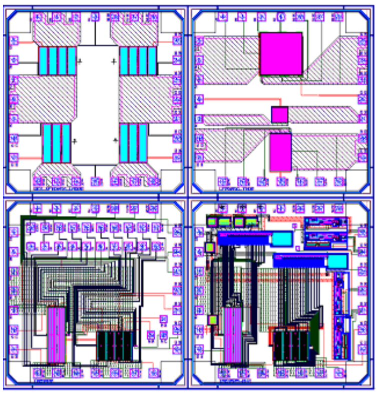

FIGURE 8 : LAYOUT OF THE TSENSOR TESTCHIP, SHOWING AT THE BOTTOM ON TH E LEFT THE POWER TRANSISTOR WIH EMBEDDED TEMPERATURE SENSING DIODES

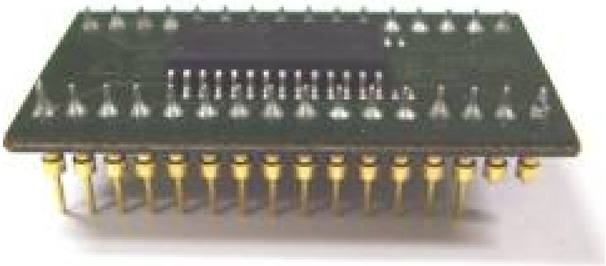

FIGURE 9 : IC AND TEST-BOARD USED FOR VALIDATION

Experimental Validation

In order to validate our electro-thermal simulation scheme, a test-chip containing several power transistors and temperature sensors was manufactured in assembled in several package confirgurations. Figure 8 shows a view of the testchip, consisting of four blocks to achieve a representative die-size, but where only the lower left-hand-side block was effectively used. The driver transistor is a 50V N-type vertical DMOS device fabricated in the I3T process of AMIS. 18 temperature sensing diodes are placed inside and around the area of the driver in order to record the temperature distribution. Figure 9 shows the device mounted in an SOIC package on the test-board.

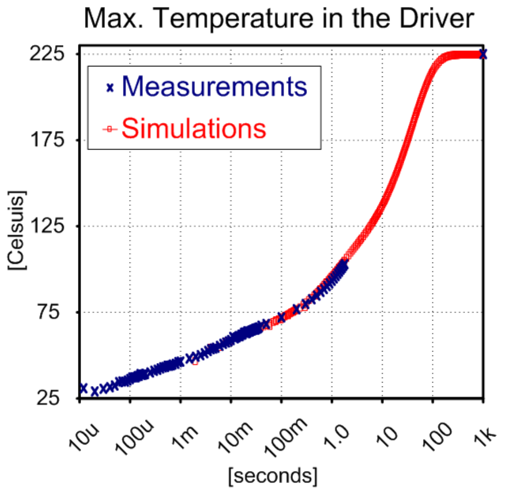

FIGURE 10 : MEASURED AND SIMULATED THERMAL IMPULSE RESPONSE

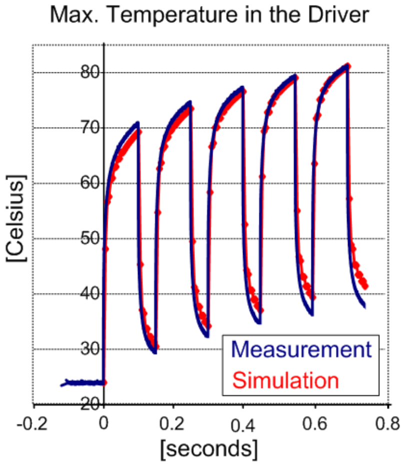

FIGURE 11 :

Two types of experiments were conducted : (a) thermal impulse responses were measured with a constant dissipation applied, (b) the response to a series of high-level pulses was measured, combining short-term and long-term heating trends. Figure 10 compares the measured and simulated thermal response measured at the centre of the driver. The data-points from 10us till 2s are measured with the oscilloscope on one single pulse. Note the last data-point measured separately in regime at 1000s. Figure 11 compares also measured and simulated temperatures at the centre of the driver but in pulsed mode .In all cases the simulation results agree well with the measured data.

Conclusion

We demonstrated a practical scheme to realize dynamic electro-thermal simulations at chip-level, and proposed a method allowing to easily generate a set of boundary conditions for the thermal solver. The validity of our approach is illustrated on a SOIC configuration in two different dissipation schemes. Work is on-going to extend the boundary conditions models and the validation to other package types.

Acknowledgements

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