Thermal Modeling of On-Chip Interconnects and 3D Packaging Using EM Tools

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ABSTRACT
The green (low power) chip design demands dramatic thermal and electrical simulation capabilities. In this paper, a novel thermal simulation approach for automatic thermal modeling of very large problems is introduced. This methodology can be fully integrated with existing solvers for electrical simulations, and make it possible to analyze practical on-chip and packaging thermal problems using the existing electromagnetic tools and geometry definitions, with very small additional effort. Its various applications to BEOL (on-chip wiring), thermal guideline design, and 3D integration (for multiple chip stacks) thermal modeling are investigated in this paper. We will demonstrate this capability with an automatic modeling framework, ChipJoule, for representative cases.

I. INTRODUCTION

Temperature rise due to the current carrying interconnects has tremendous impact upon the IC performance and reliability. Current flow in a VLSI interconnect causes a power dissipation of I^2R, which is referred to as Joule heating or self-heating. The Joule heating effects are becoming increasingly significant with the shrinking scale of Integrated Circuit technology because of increased on-chip power densities, inclusion of more metal layers with higher densities, and use of dielectric materials with lower thermal conductivities.

Joule heating is well-known for its impact on the interconnect lifetime through electromigration (EM) effect on reliability, that has a strong dependence on temperature [1]. In addition to the reliability, thermal effects also impact the electrical performance, and design optimization of interconnects [2-3]. Hence, accurate and efficient modeling of temperature rise in interconnects and packaging because of Joule heating is critical to the design of high performance semiconductor chips.

Temperature distribution simulation for IC interconnects and 3D packaging involves solving the three-dimensional (3D) or two-dimensional (2D) heat-conduction equation in a multi-level dielectric stack with interconnects, vias, and metal fills embedded in it. While some analytical thermal models are available for multi-level interconnects, the 2D/3D nature of heat-conduction in the presence of such complicated structures is either neglected or treated approximately [4-7]. Previous finite-element thermal simulation approaches have confined themselves to smaller problems with fewer metal layers or used assumptions of symmetry for worst-case structures [8-9] due to tool limitations. On the other hand, most methodologies were implemented by building tools dedicated to thermal analysis only, without interfaces to mask CAD layouts, and used mostly manually-created shapes.

In addition, these approaches are not readily integrated with on-chip CAD tools and design flows. Due to the extremely high integration density on chips, handling the resultant huge simulation structures becomes an intractable problem for most in-house and commercial tools, and traditionally people are forced to either look at small-sized problems or use approximate analytical models for thermal analysis.

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In this paper, we propose a novel methodology to use existing electromagnetic simulation tools for interconnect and packaging structures to simulate and model the temperature distribution and thermal resistances without any major modifications to these tools or the simulated structures.

II. Methodology of Thermal Analysis from Electrical Simulation

Poisson's Equation

$\nabla(\varepsilon\nabla\phi) = -\rho$

In the dielectric (Im. Part):

$\nabla(\sigma_{el}\nabla\phi) = 0$

Electrical Current Density:

$\frac{I}{A} = J = \sigma_{el}E = -\sigma_{el}\frac{\partial\phi}{\partial x}$

Heat Equation (Steady-State):

$\nabla(\kappa_{th}\nabla T) = -q_g$

In the dielectric (No heat generation):

$\nabla(\kappa_{th}\nabla T) = 0$

Thermal Flux:

$\frac{q}{A} = \Phi_{th} = -\kappa_{th}\frac{\partial T}{\partial x}$

Potential (ϕ) $\Leftrightarrow$ Temperature (T)

Current (I) $\Leftrightarrow$ Heat Flow (q)

Elec. Conductivity (σ_{el}) $\Leftrightarrow$ Thermal Conductivity (κ_{th})

Elec. Resistance (R_{el}) $\Leftrightarrow$ Thermal Resistance (R_{th})

Figure 1: Analogy between Electrical and Thermal Problems

The method of this work is based on the analogy between electrical and thermal conduction problems. As shown in Figure. 1, Poisson's equation for electrical charge can be transformed into the heat-equation, by transforming electric potential into temperature, electrical current into heat flow, electrical conductivity into thermal conductivity, and electrical resistance into thermal resistance. As to the resistance, a Laplace equation needs to be solved. Hence, any tool, which is capable of solving Laplace equation in a composite dielectric-stack with several metal layers, can be used to solve the temperature distribution in the same structure, by making the necessary transformations to the input and output variables of the tool.

An existing electrical resistive solver RGEN from the IBM Electrical Interconnect Packaging (EIP) Tool suite [10] has been used in this work. It has been successfully used for up to 64M resistive nodes. However, different thermal boundary conditions need to be emulated using electrical circuit components for the electrical resistance solver. There are three types of important conditions to be addressed: (1) *constant temperature*; (2) *constant heat density*; (3) *Joule heating*. Voltage sources and current sources with different source resistances are used to trick the electrical resistance solver into thinking it is still handling a classical electrical problem while its output is the temperature distribution or equivalent thermal resistance network. In addition, the thermal conductivity has to be converted into electrical conductivity with certain scales to guarantee a one-to-one mapping. It is found that this process is not trivial. Improper source setup can dramatically degrade the simulation accuracy provided by the resistance solver. During the conversion, all thermally conductive dielectrics have to be considered as electrical conductors. The thermal boundaries must be given very high thermal conductivity to obtain best approximation of different heating conditions.

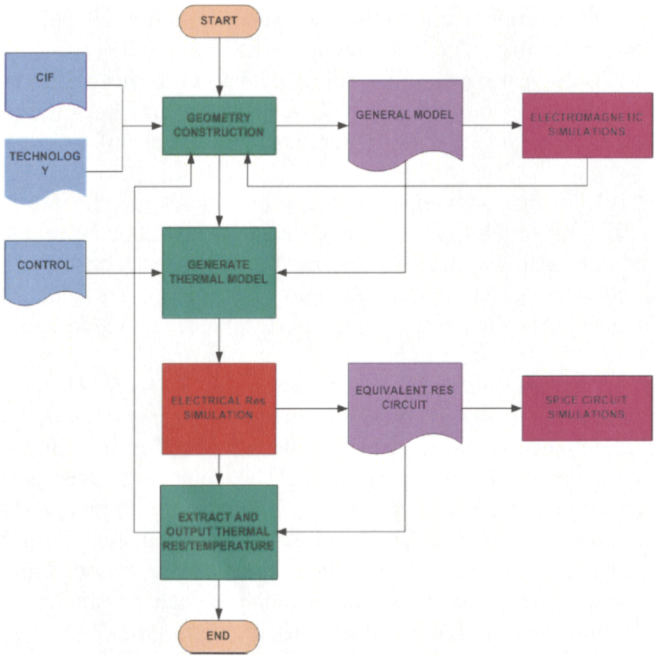

Figure 2: Flow-chart describing the implementation of the invented methodology

III. AUTOMATION

A complete and automatic simulation framework, *ChipJoule*, starting from the technology file to the temperature distribution, has been developed using this analogy methodology. A flow chart is show in Figure 2. It emphasizes the automation so that the layout data can be directly used for the geometry construction. It also highlights the coupling between thermal and electrical problems so that the EM and Thermal analyses and optimization could be done simultaneously. The outputs can be further sent into SPICE circuit simulators to deliver maximum flexibility for post data processing and closed-loop electro-thermal sensitivity analyses.

IV. NUMERICAL EXAMPLES FOR BEOL AND 3D PACKAGING

Many representative benchmarks for both 2D and 3D applications have been verified with this method by comparing *ChipJoule* and the popular commercial thermal tool *ANSYS*™. Perfect agreements have been

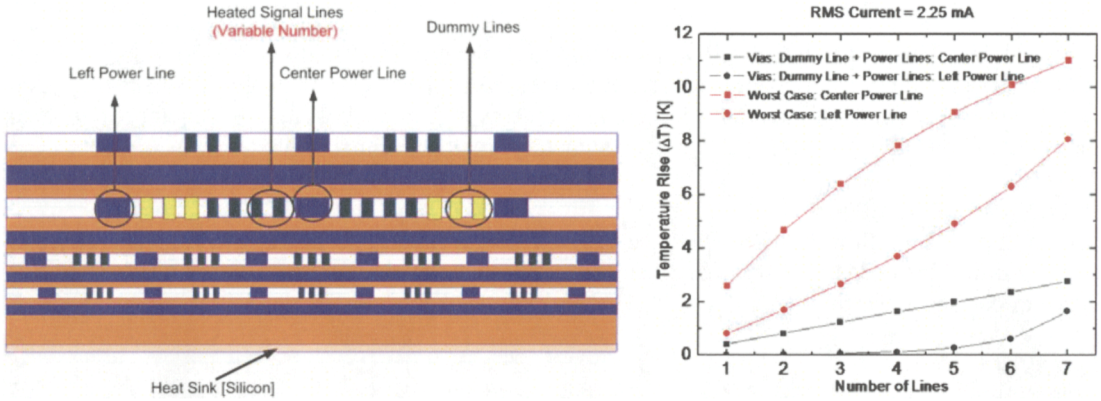

Figure 3: The full stack study of 45nm on-chip wiring for temperature rise on the power lines due to different Joule heating scenarios.

obtained. We also applied this method to many practical BEOL thermal guide-line design generations and 3D packaging analyses. The largest problem analyzed required close to 9M nodes. Figure 3 shows a full 45nm stack analyzed under different scenarios to understand the Joule heating effects in the power lines caused by the RMS current in the signal lines surrounding them. It demonstrates the influence of the other metal and via layers on the temperature rise of the target power lines. It shows that it is possible to use

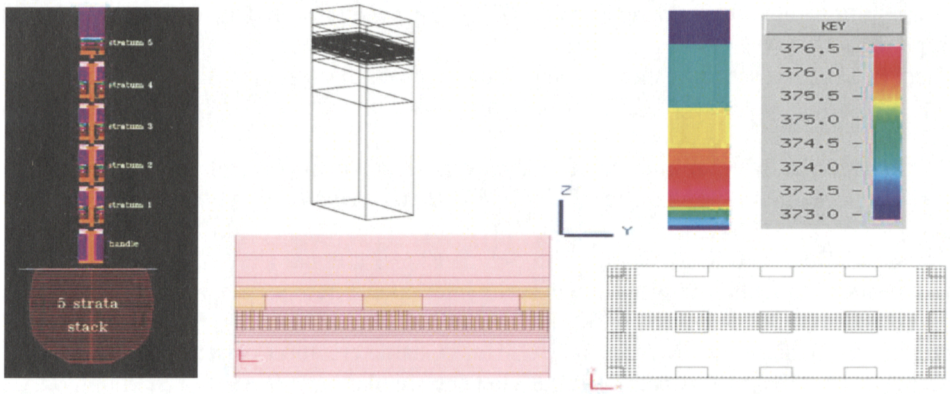

Figure 4: The study of an eDRAM 3D packaging for the temperature distribution due to the device heating in the eDRAM chip.

dummy metal lines and vias to constrain the temperature rise below 5 degrees.

An eDRAM chip 3D packaging model, part of a stack of several chips, is constructed using *ChipJoule* automatically in Figure 4. Chips above and below it are represented by blocks using relevant equivalent thermal conductivities. The device heating is emulated by heat density boundary condition within one

layer of the eDRAM. The vertical temperature distribution through a slice, shown in the upper right, is obtained directly from the simulation when both ends of the whole stack are set to be the heat sinks. All the details of the multi-layer eDRAM chip layout were considered in the simulation and Figure 4 also shows, in the bottom right, the different views of the heated region.

V. SUMMARY

This paper describes a novel methodology for thermal modeling of on-chip interconnects using electromagnetic simulation tools. It uses the analogy between electrical and thermal problems and calculates the temperature distribution in the on-chip interconnects that are embedded in a multi-layer dielectric stack, with vias and metal fills. Electrical resistance is used to obtain the thermal resistance by substituting the electrical resistivity with the material thermal conductivity. A fully automated tool named *ChipJoule* has been developed based on this methodology. The full stack BEOL structure and 3D chip stacks have been analyzed using this technique.

This methodology can be full integrated with existing tools for electrical analysis and does not require the users to construct additional simulation structures for thermal analysis. Our methodology makes it possible to analyze massively complex interconnect thermal problems, using the existing electromagnetic tools and geometry definitions directly from CAD layouts, with very small additional effort.

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