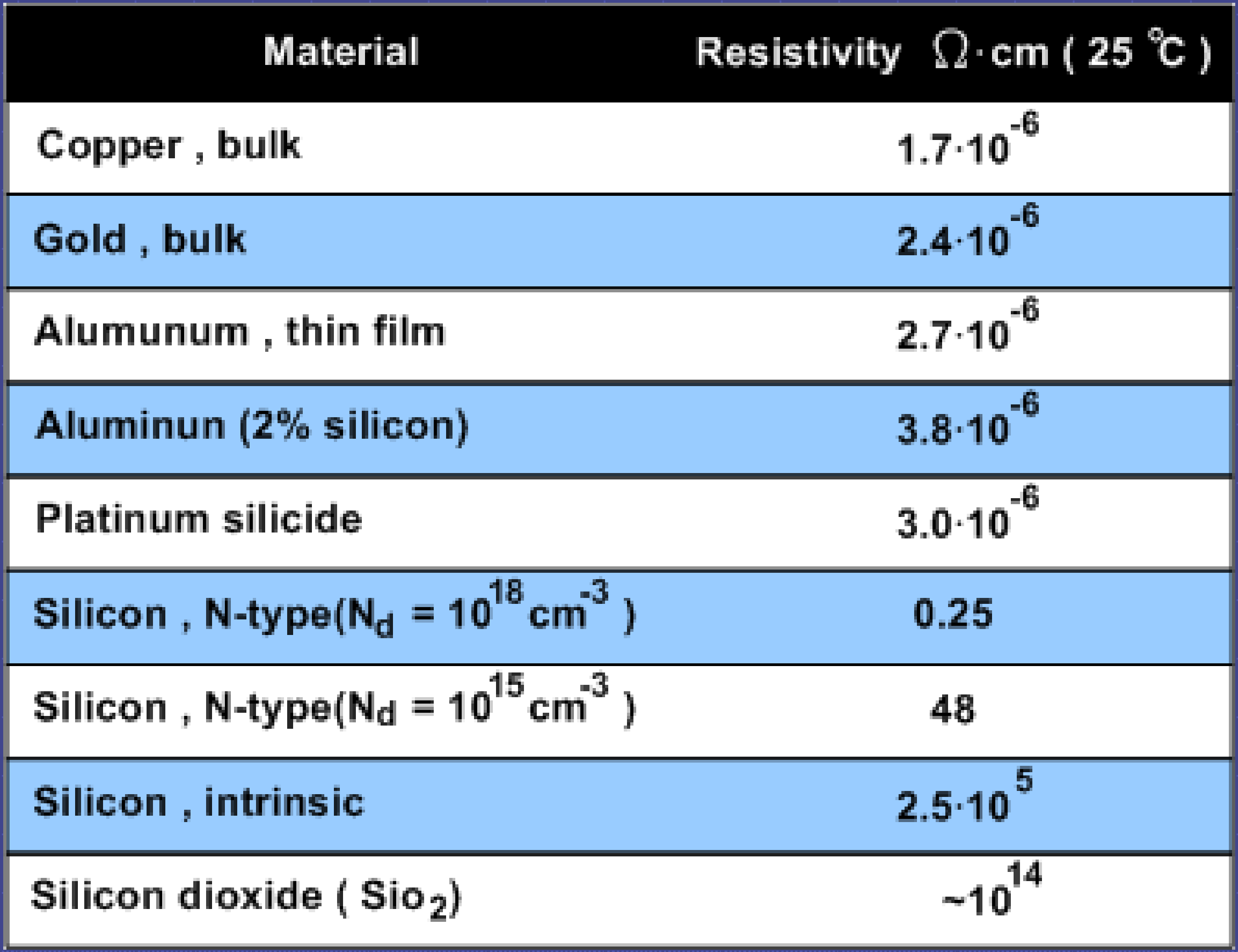
# Chapter 6  Layout of Resistor

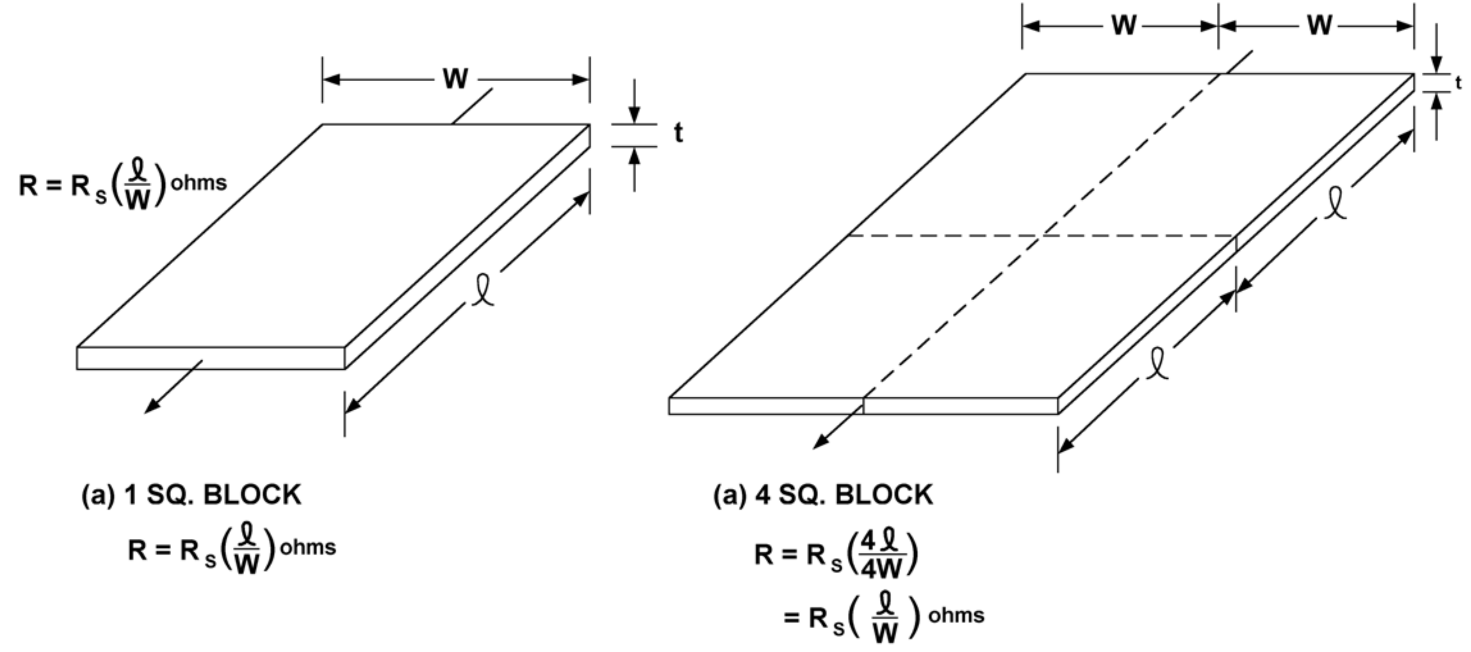
- Resistance Estimation
- Resistivity and Sheet Resistance
- Resistor Layout
- Resistor Variability
- Resistor Parasitics
- Comparison of Available Resistors
- Adjust Resistor Values

# Resistivities



| Material | Resistivity Ω·cm ( 25 ℃ ) |
|---|---|
| Copper , bulk | $1.7\cdot10^{-6}$ |
| Gold , bulk | $2.4\cdot10^{-6}$ |
| Alumunum , thin film | $2.7\cdot10^{-6}$ |
| Aluminun (2% silicon) | $3.8\cdot10^{-6}$ |
| Platinum silicide | $3.0\cdot10^{-6}$ |
| Silicon , N-type($N_d = 10^{18} cm^{-3}$ ) | 0.25 |
| Silicon , N-type($N_d = 10^{15} cm^{-3}$ ) | 48 |
| Silicon , intrinsic | $2.5\cdot10^{5}$ |
| Silicon dioxide ( $Sio_2$) | $\sim10^{14}$ |

# Resistance Estimation

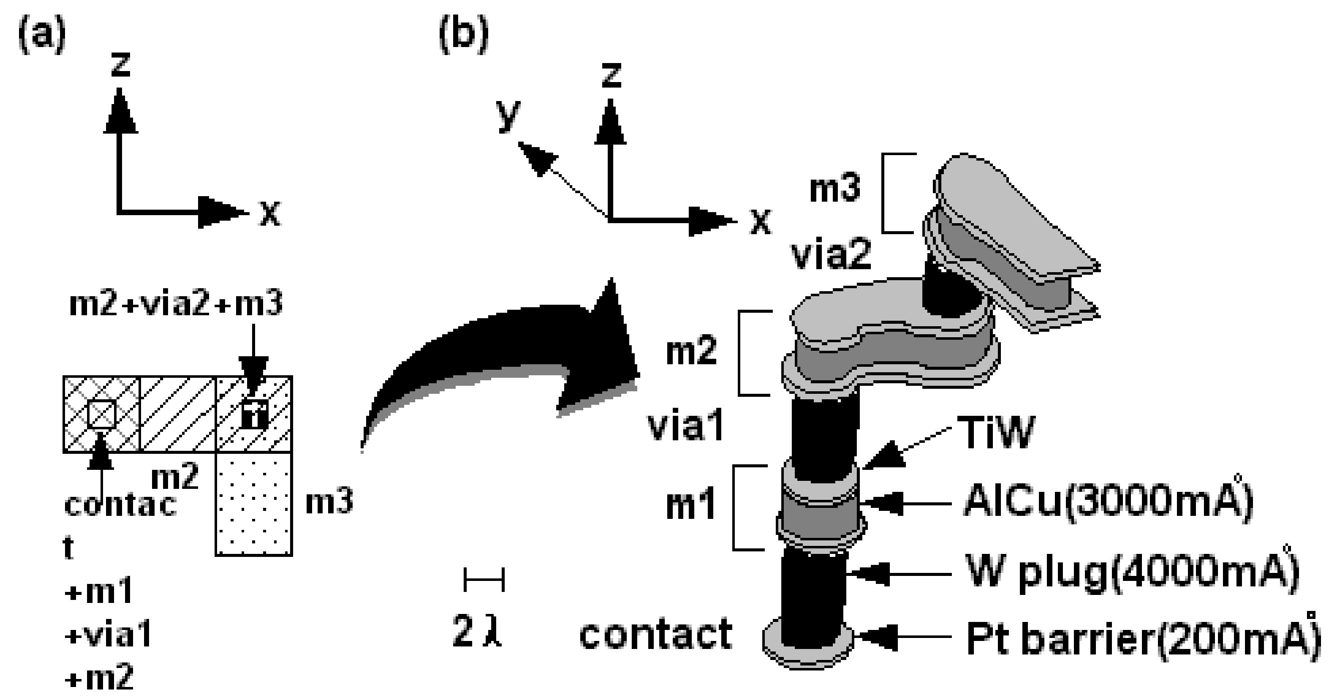


The resistance of a uniform slab of conducting material

$$R = \frac{\rho \ell}{A} = \frac{\rho \ell}{t\ w} = R_S \frac{\ell}{w}$$

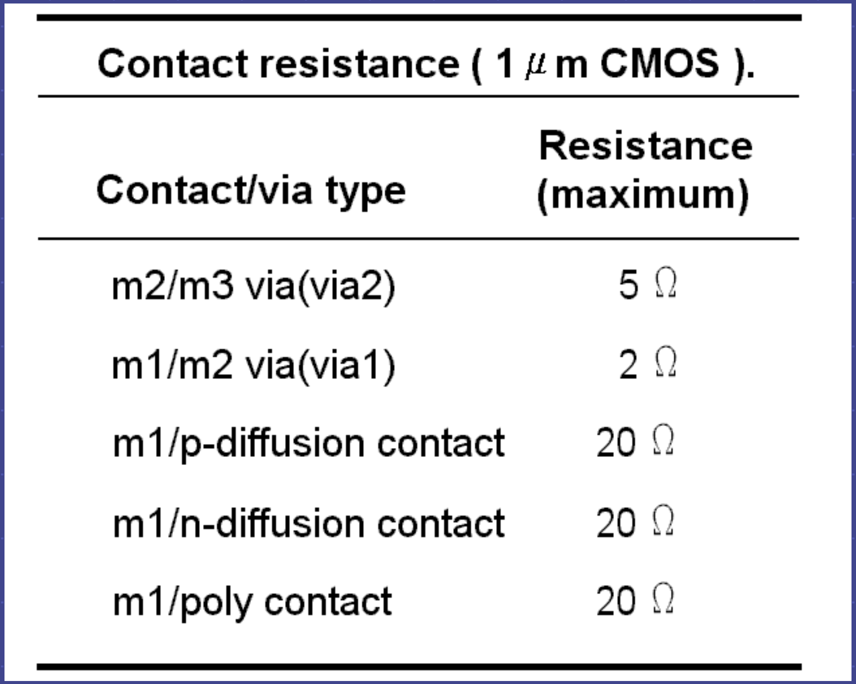
$\rho$ : resistivity
t : thickness
$\ell$ : conductor length
w : conductor width
Rs : sheet resistance

# Interconnections and Contacts/Vias



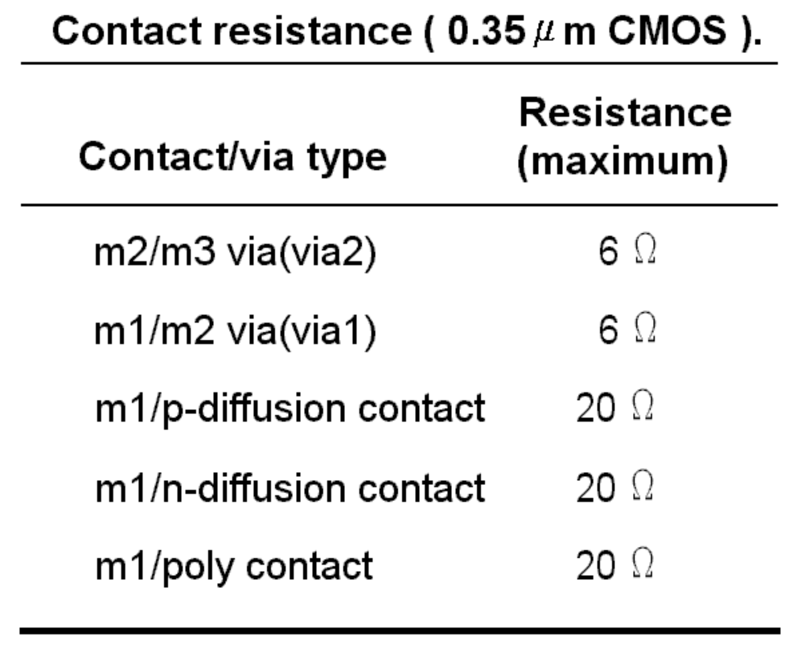
- Put barrier metal (typically platinum) to reduce the contact resistance and the likelihood of breaks in the contact.
- Use chemical-mechanical polishing (CMP) to smooth the wafers flat before each metal deposition step to help with step coverage.
- Insulator between layers – $SiO_2$

# Contact Resistance Parameters



Contact resistance ( 1 μm CMOS ).

| Contact/via type | Resistance (maximum) |
|---|---|
| m2/m3 via(via2) | 5 Ω |
| m1/m2 via(via1) | 2 Ω |
| m1/p-diffusion contact | 20 Ω |
| m1/n-diffusion contact | 20 Ω |
| m1/poly contact | 20 Ω |



Contact resistance ( 0.35 μm CMOS ).

| Contact/via type | Resistance (maximum) |
|---|---|
| m2/m3 via(via2) | 6 Ω |
| m1/m2 via(via1) | 6 Ω |
| m1/p-diffusion contact | 20 Ω |
| m1/n-diffusion contact | 20 Ω |
| m1/poly contact | 20 Ω |

# Silicide and Salicide

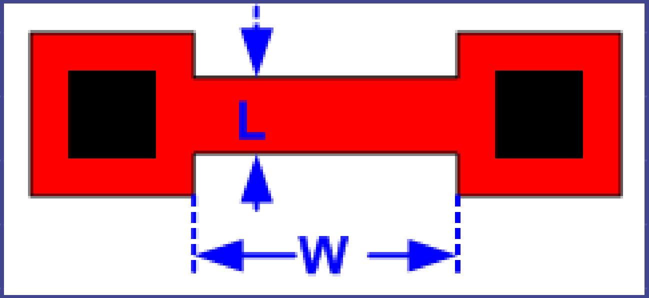
Diffusion – $n^+$ or $p^+$

Silicide poly gate – e.g. metalic compound of silicon
Tantalum silicide TaSi ,
Tungsten silicide WSi ,
or Titanium silicide TiSi

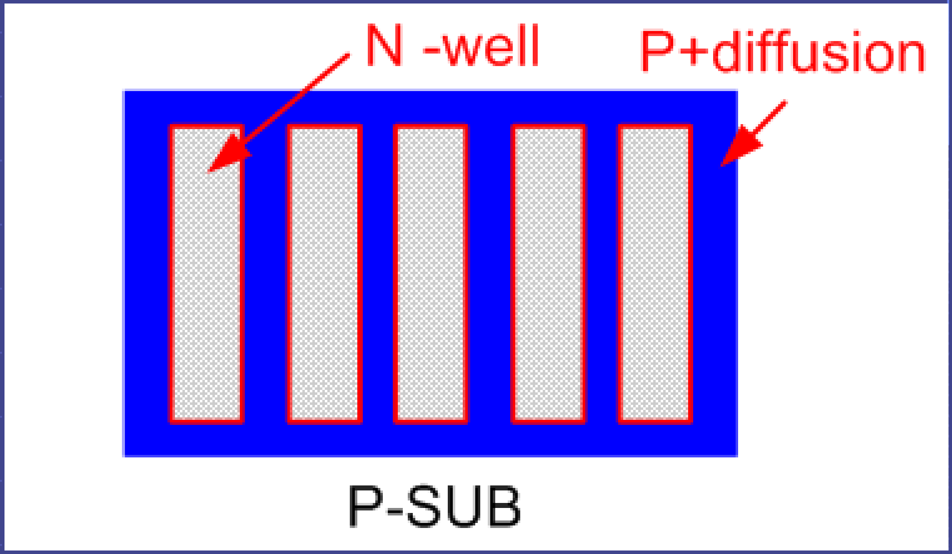
Salicide ( self-aligned silicide )
– both gate and sourse/drain regions are silicided

# Resistor Types

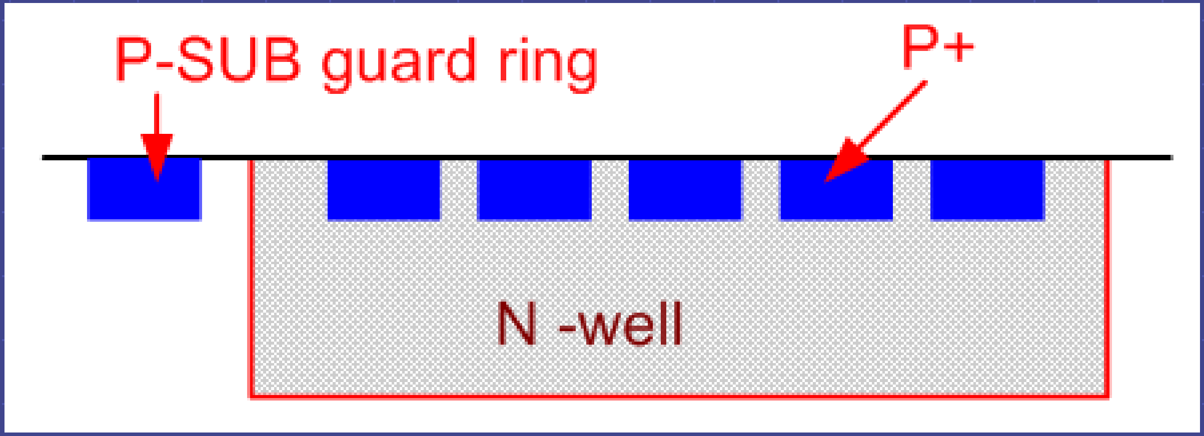
**Poly**



**well**

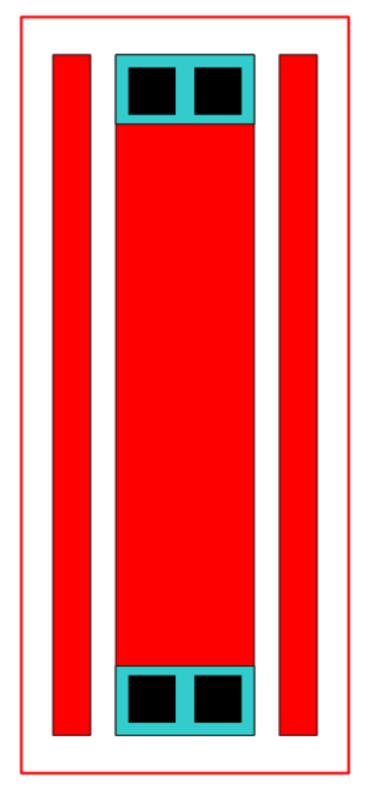


**diffusion**

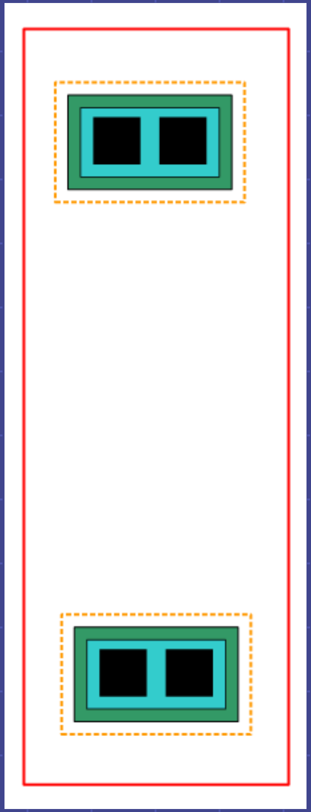


# Resistor Types

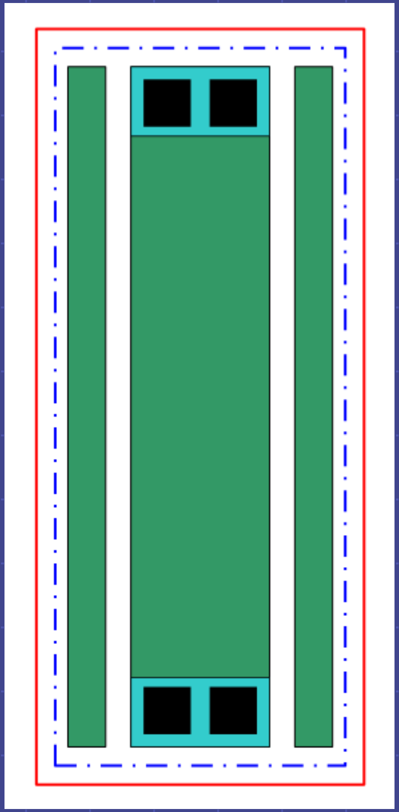
**Poly**



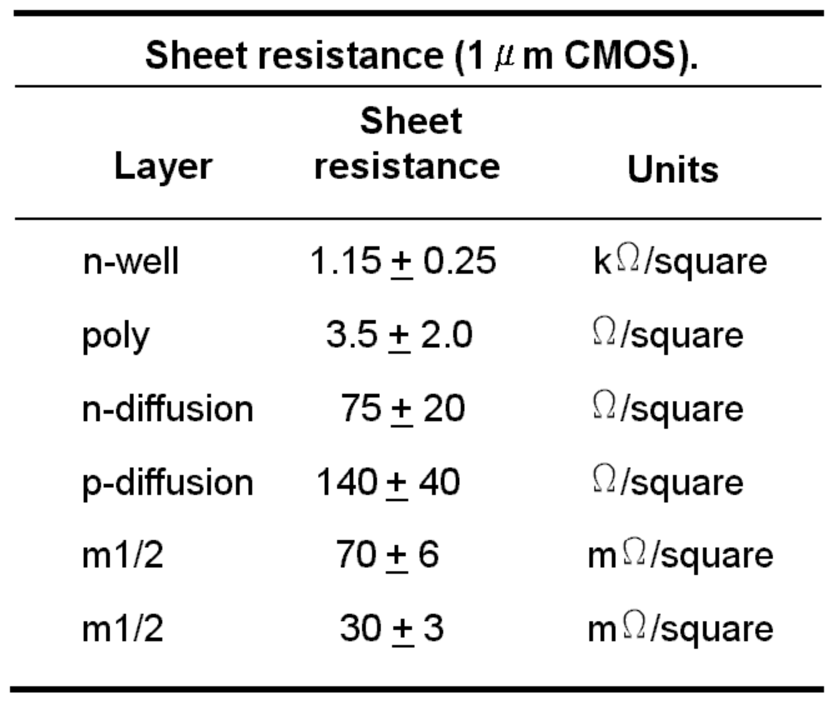
**well**



**diffusion**

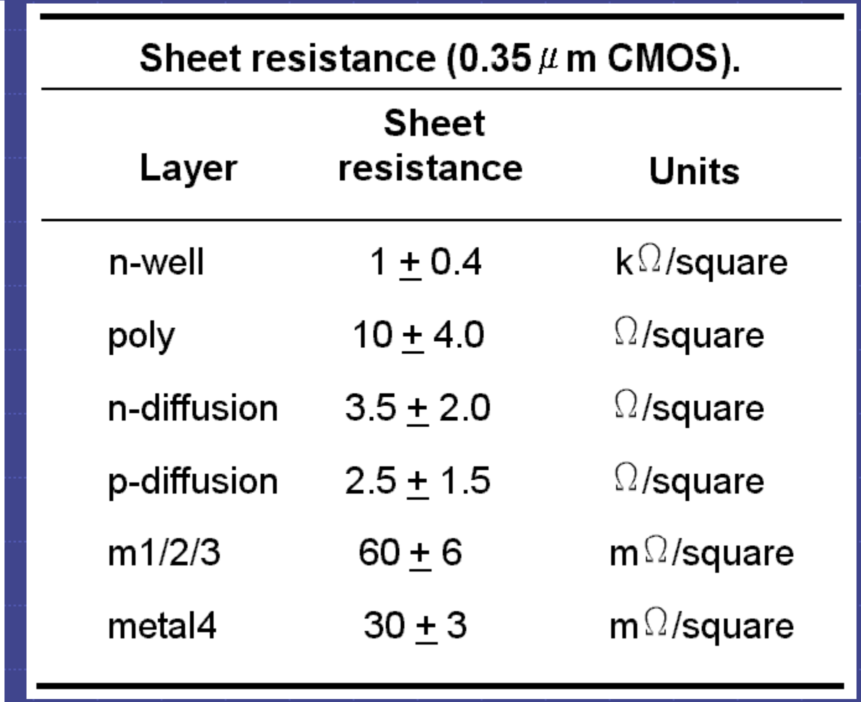


# Sheet Resistance Parameters



Sheet resistance (1 μm CMOS).

| Layer | Sheet resistance | Units |
|---|---|---|
| n-well | 1.15 ± 0.25 | kΩ/square |
| poly | 3.5 ± 2.0 | Ω/square |
| n-diffusion | 75 ± 20 | Ω/square |
| p-diffusion | 140 ± 40 | Ω/square |
| m1/2 | 70 ± 6 | mΩ/square |
| m1/2 | 30 ± 3 | mΩ/square |

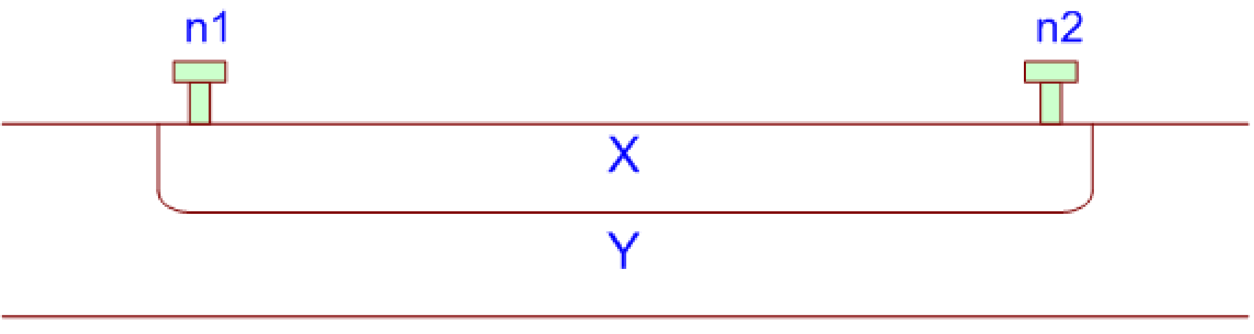


Sheet resistance (0.35 μm CMOS).

| Layer | Sheet resistance | Units |
|---|---|---|
| n-well | 1 ± 0.4 | kΩ/square |
| poly | 10 ± 4.0 | Ω/square |
| n-diffusion | 3.5 ± 2.0 | Ω/square |
| p-diffusion | 2.5 ± 1.5 | Ω/square |
| m1/2/3 | 60 ± 6 | mΩ/square |
| metal4 | 30 ± 3 | mΩ/square |

# Resistor Equivalent Circuit Model

## 1) Circuit Models for AC Effect of Diffused and Ion-Implanted Resistors



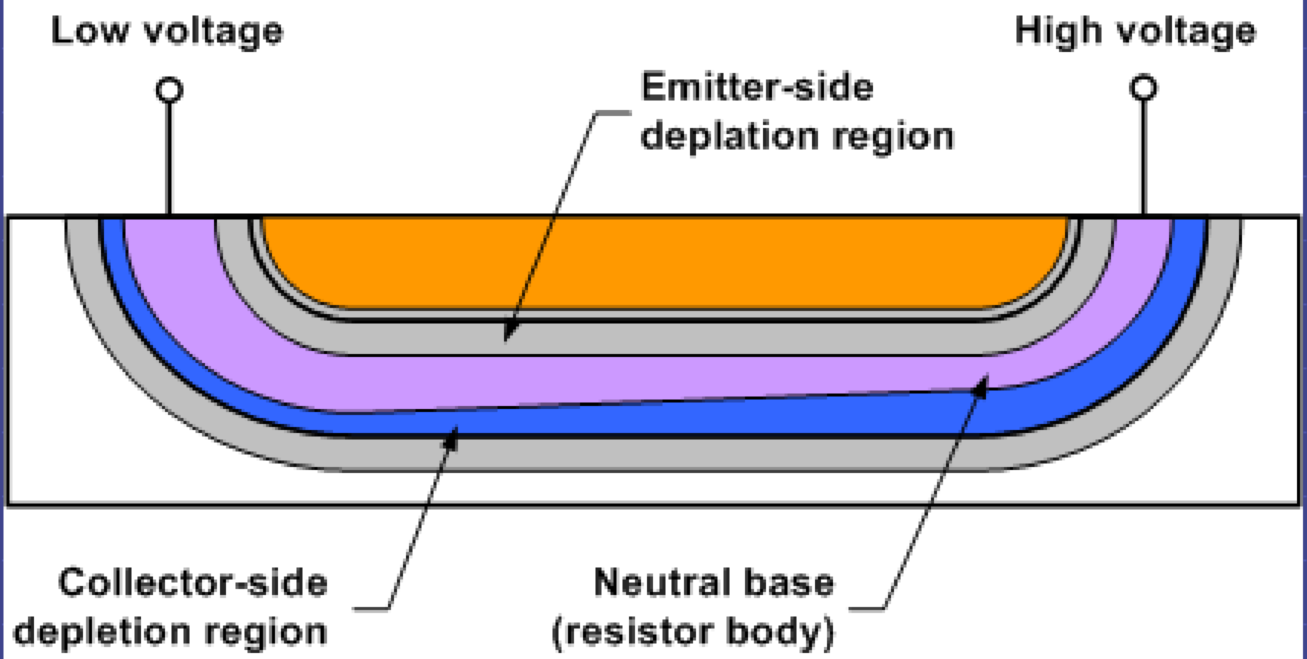
X , Y : N+ Pwell

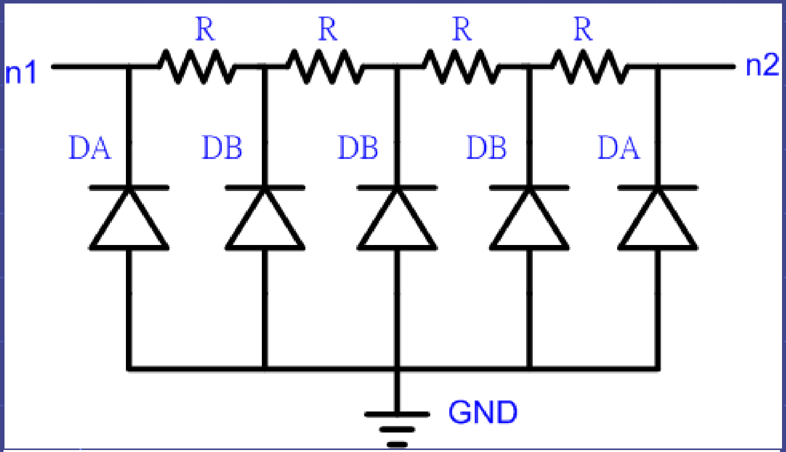
P+ Nwell

Nwell Psub

Cross section of Diffused and Ion-implanted Resistor

# Cross section of a base pinch resistor showing the intrusion of the depletion regions into the neutral base. Notice that the high-voltage end of the resistor narrows slightly





**Circuit model A**

The following functions have been implementted the model :

(1) resistor values are function of temperature :

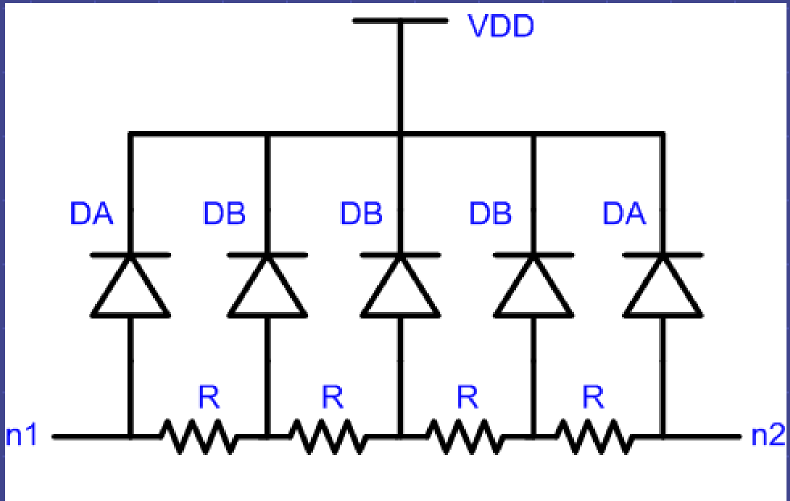
$R(t) = R0 * [\, 1 + TC1*dT + TC2 * (dt)^2 \,]$ ; where dT = T-Tnominal (25°C)

Valid range : 25°C ~ 125°C

(2) resistor values are function of temperature :

$R(V) = R0 * [\, 1 + VC1*dV + VC2 * (dv)^2 \,]$ ;

Valid range : 0 ~ 2V



Circuit model B : for P+ resistor

**Circuit model B**

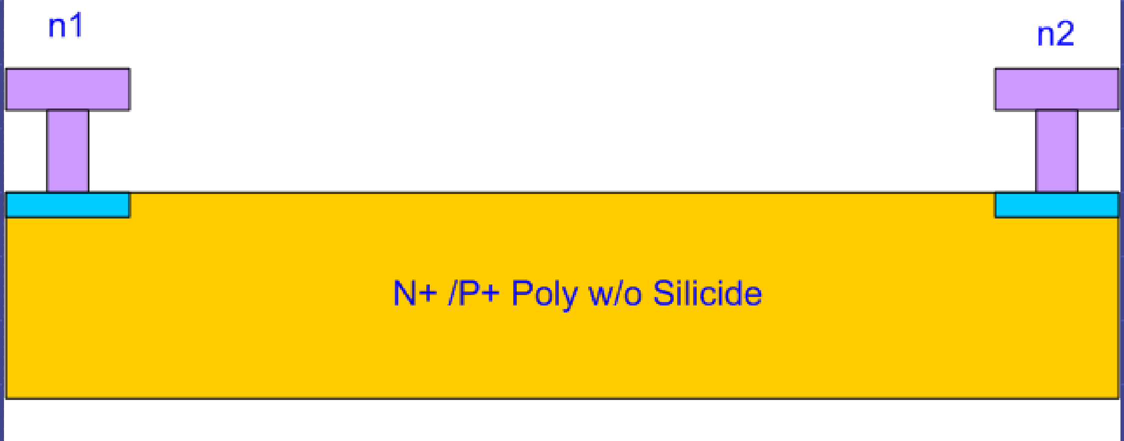
Resistor size (drawn) : L , W

DA : area = (W-deltaW) * L/5 pj = (W-deltaW) + 2*L/5

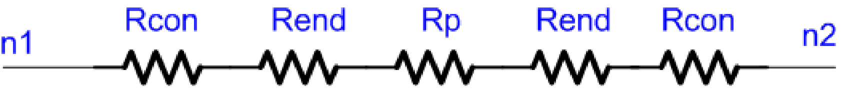
DB : area = (W-deltaW) * L/5 pj = 2*L/5

R : value = rsh*L/(4*(W-wdeltaW))

## 2) Circuit Models for N+ / P+ Poly w/o Silicide Resistor



Cross section of N+ /P+ poly w/o Silicide Resistor



circuit

Resistor Size (drawn) : L,W

R=2*Rcon+ 2*Rend+Rp

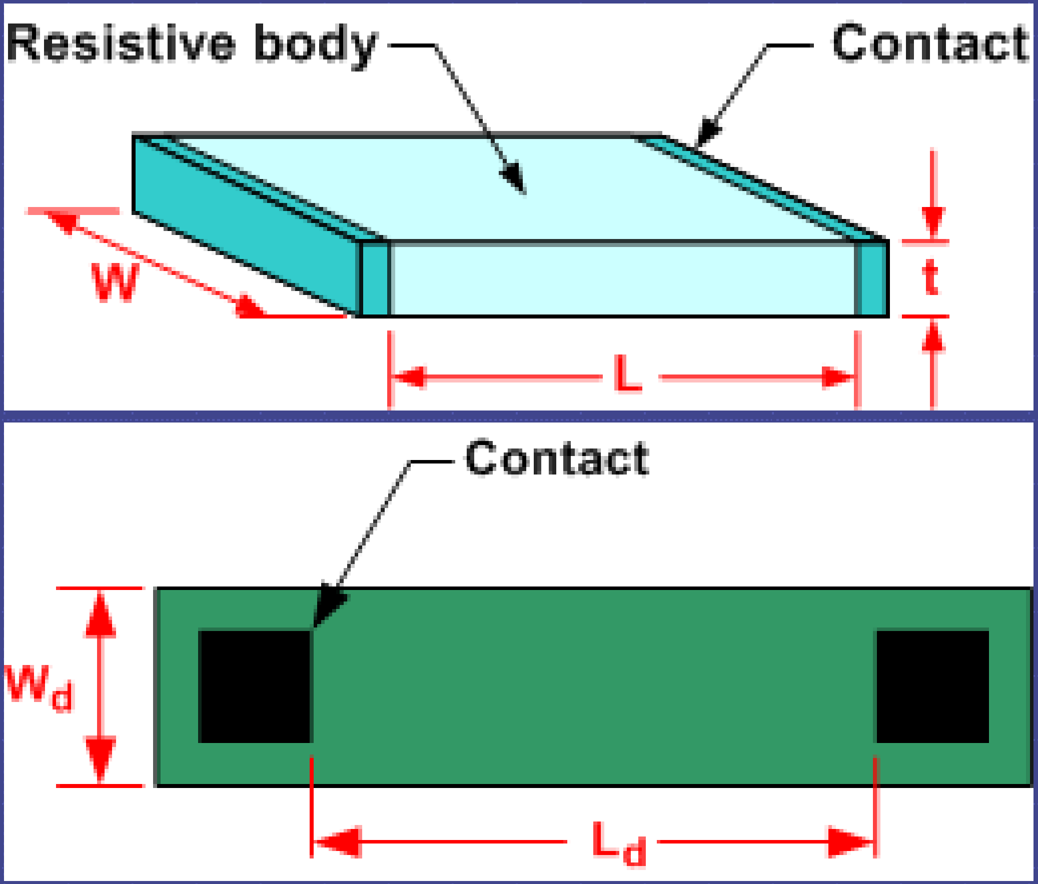
Rcon=Rc/nc$^{\text{(note)}}$

Rend=Rint / (W-DeltaW

Rp=Rsh*(L-DeltaL)/ (W-DeltaW)

Note : nc is Number of Contact, and its defaultvalue is 2

# Resistor consisting a rectangular Slab contacted by perfectly conducting terminations

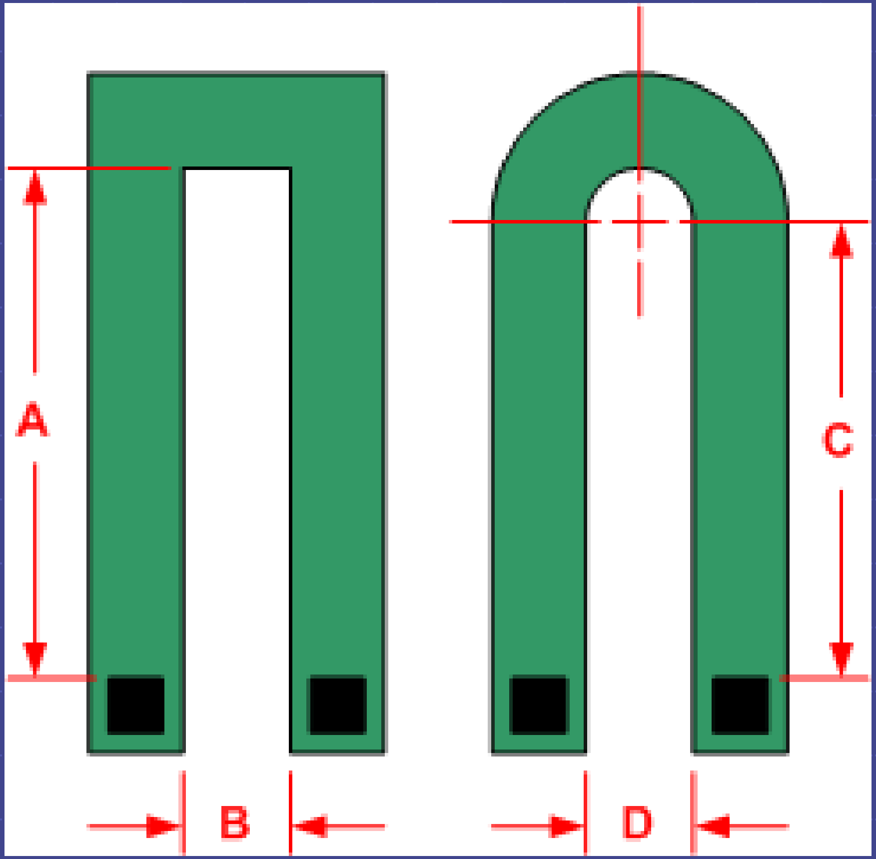


R = Rs[Ld/(Wd+Wb)]

Wb : width bias, difference between drawn width

and effective width

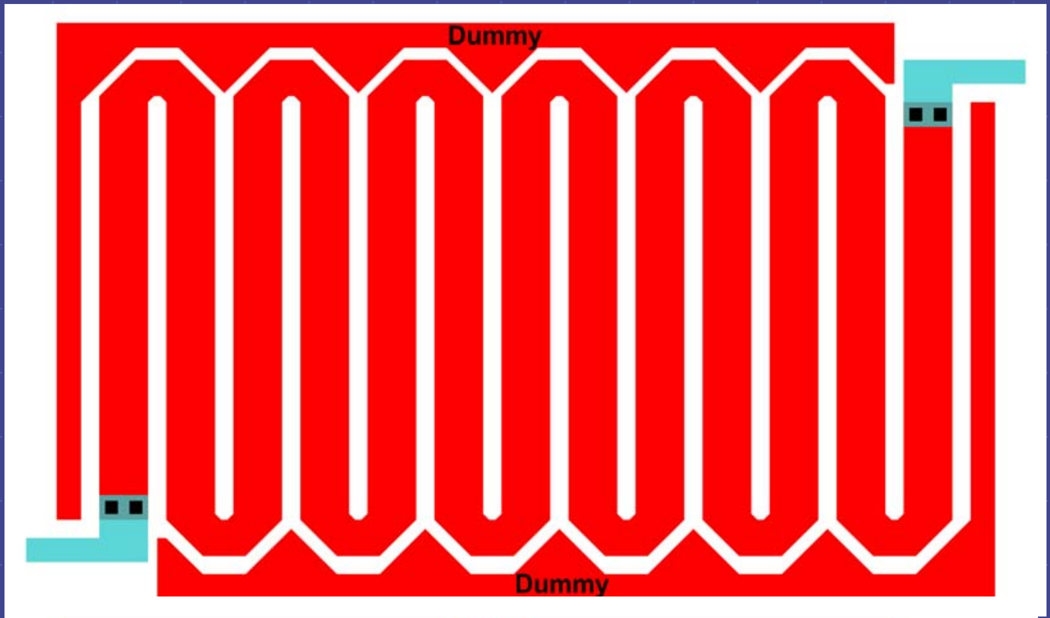
# Layout of serpentine resistors with rectangular turns and circular turns

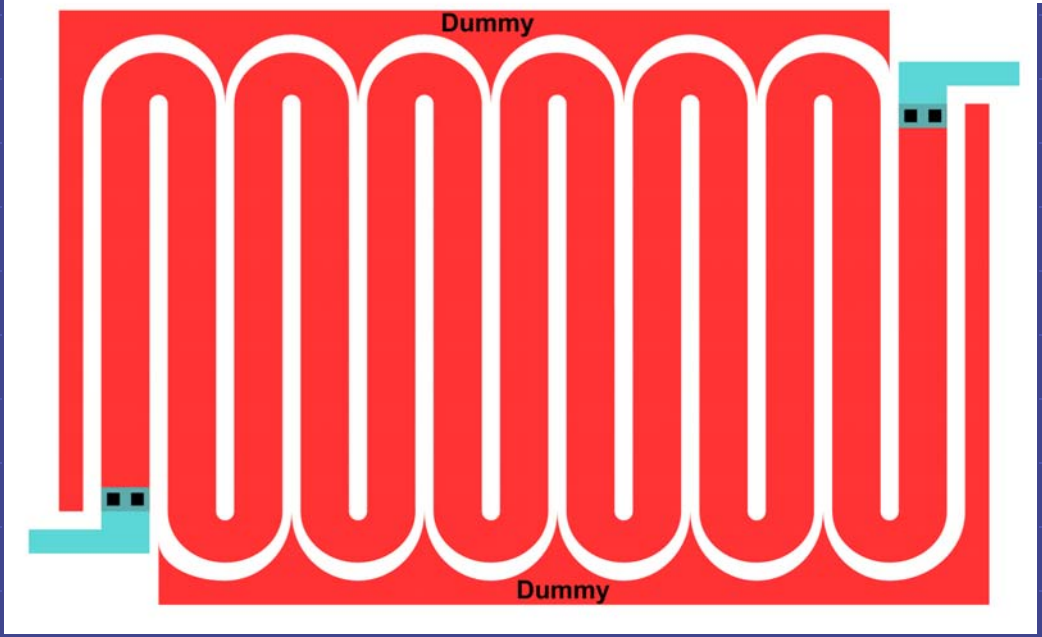


R = Rs[(2A+B)/W+1.12]

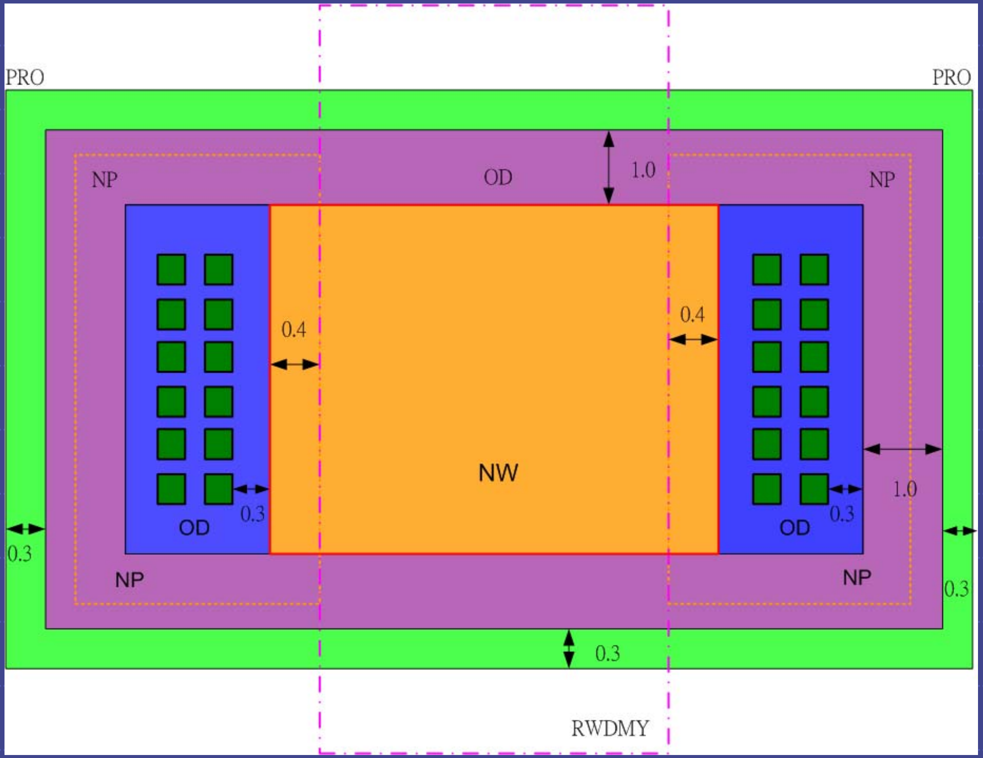
R = Rs(2C/W+2.96)

# Dummy



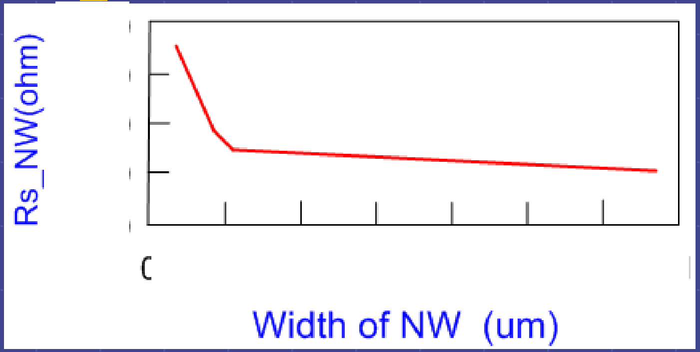


# NW resistance

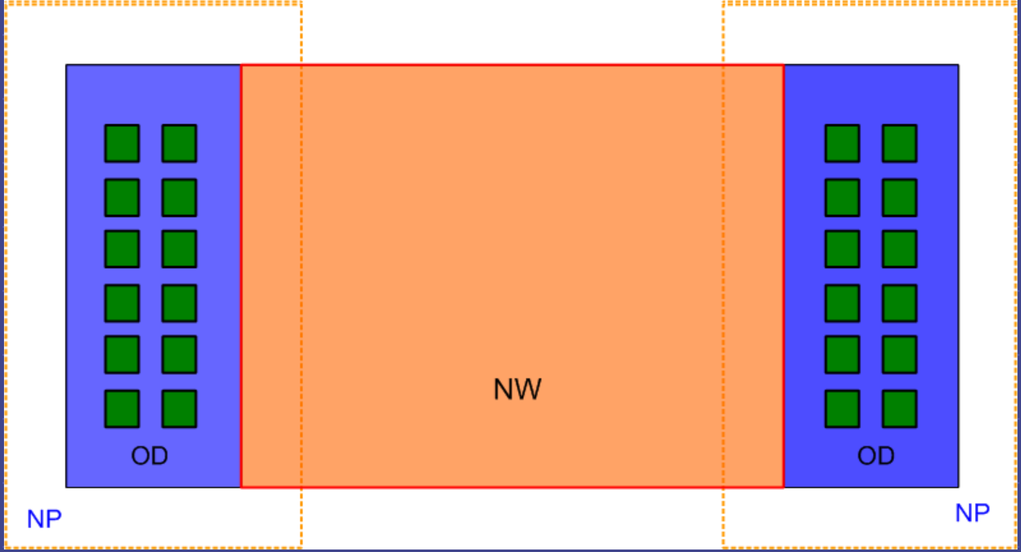


**NW within OD**

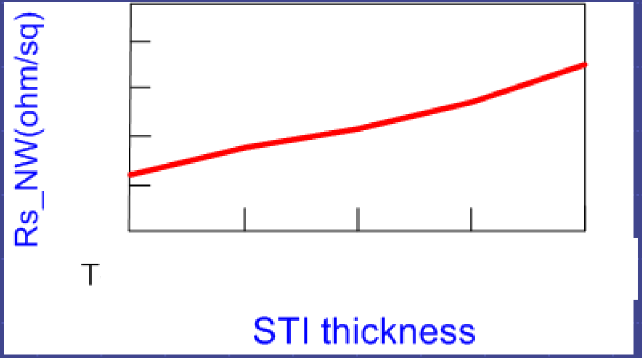
**Rs_NW under different NW dimension**



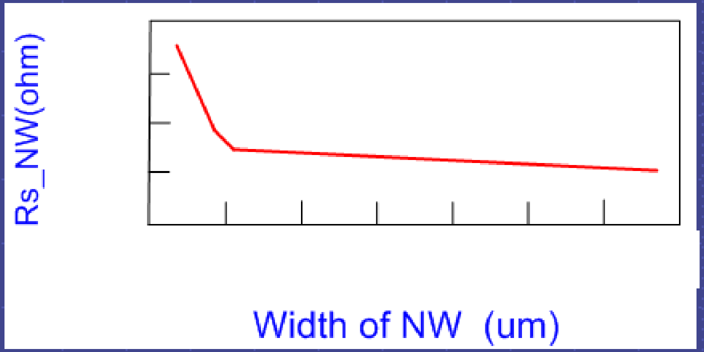
## NW under STI



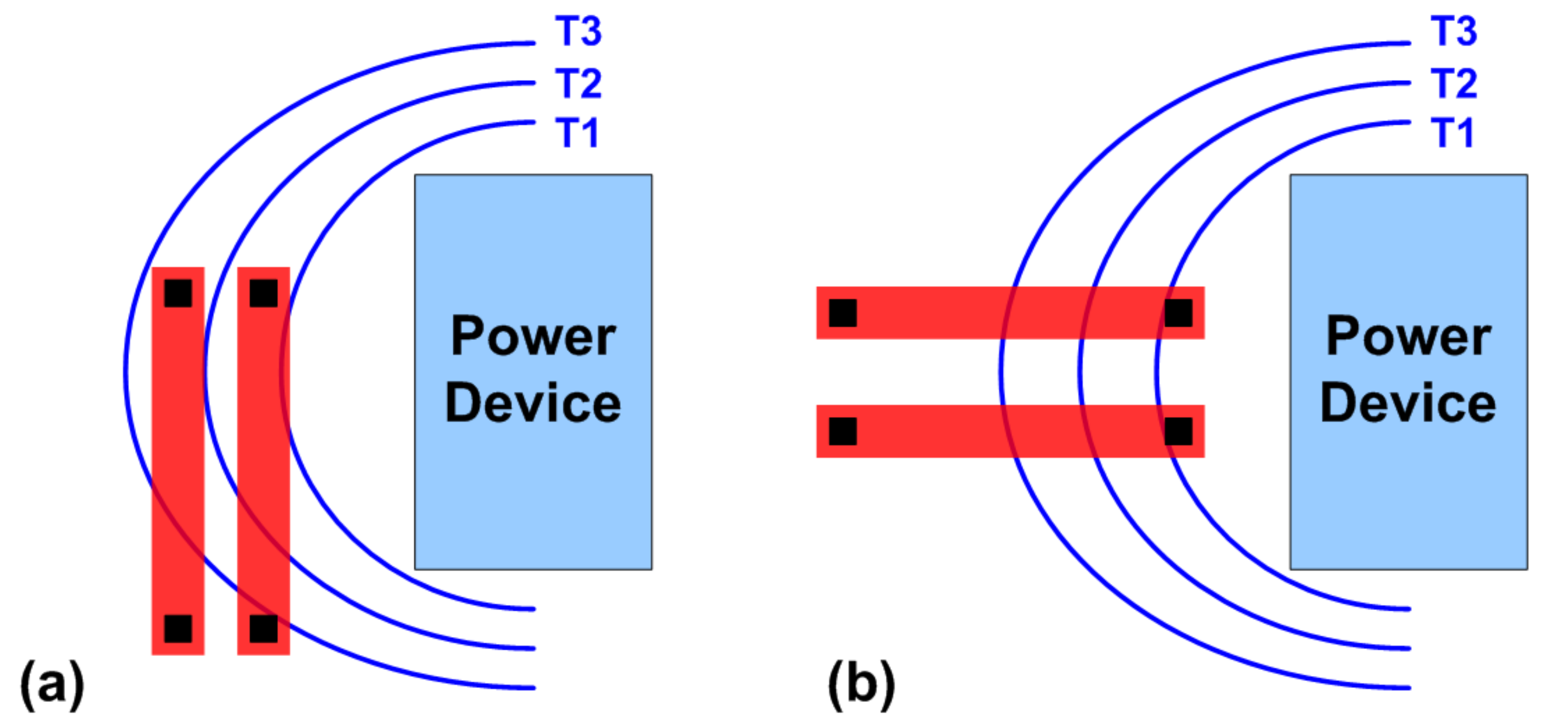
## Rs_NW under different STI thickness



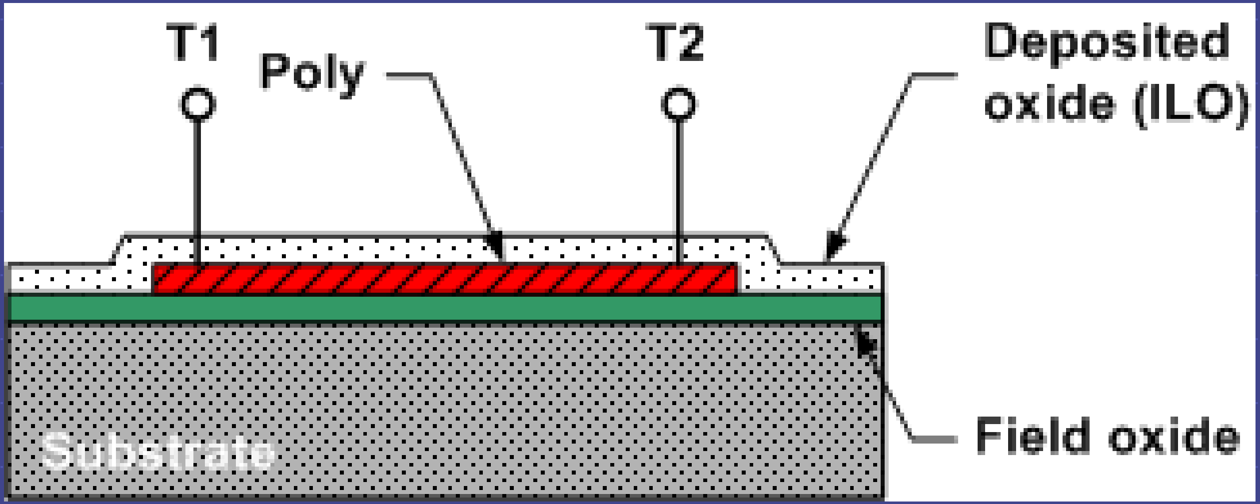
## Rs_NW v.s. NW width



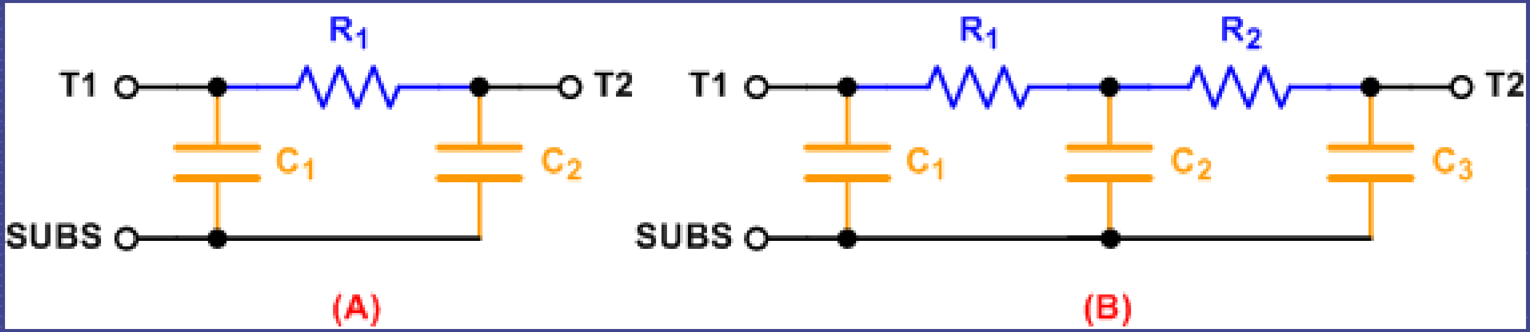
# Isothermal



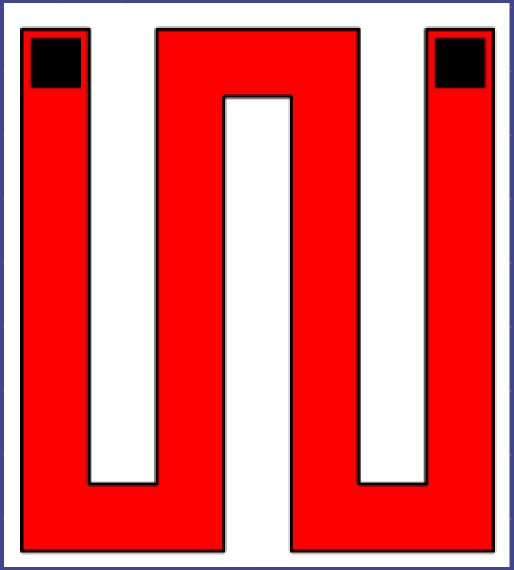
# Cross section of a polysilicon resistor.



Subcircuit models for polysilicon resistors that approximate distributed substrate capacitance using π-sections (a) single π-section and (b) dual π-section.



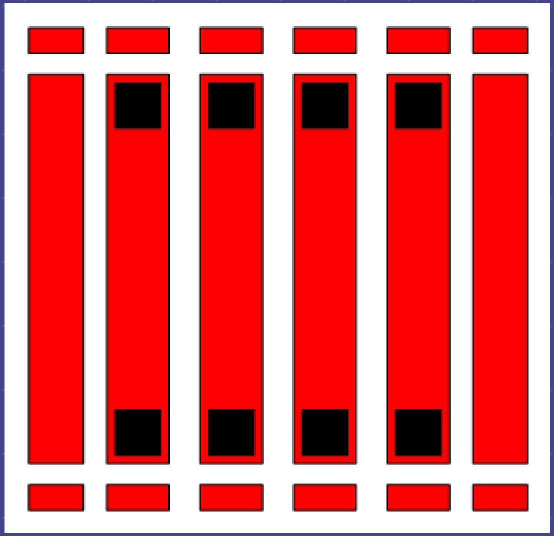
# Resistor layout

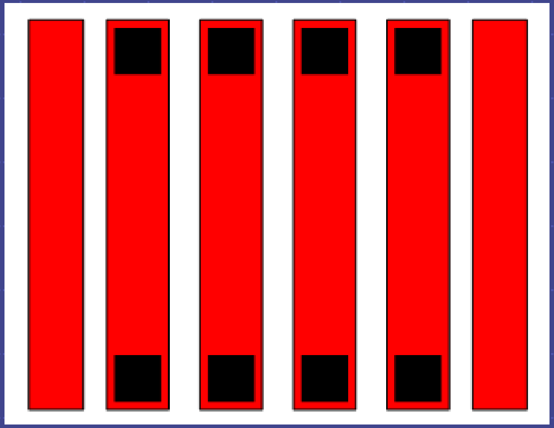


no matching issue

not care absolute value

small size

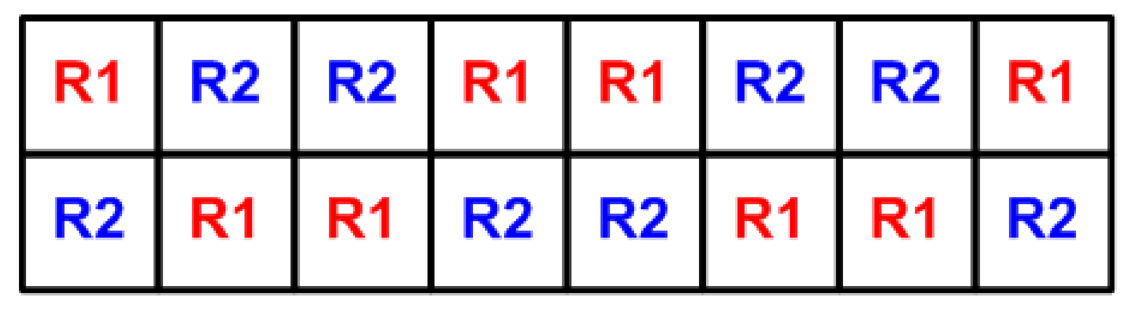




no matching issue

care absolute value

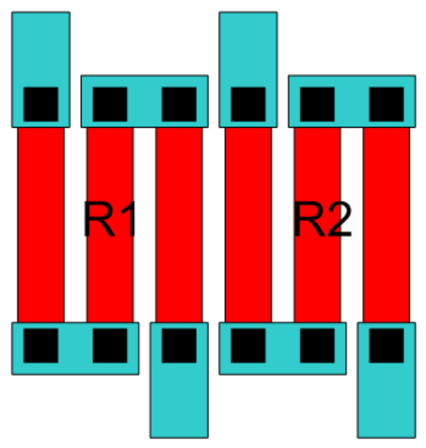
# Interdigitized Layout of Resistor

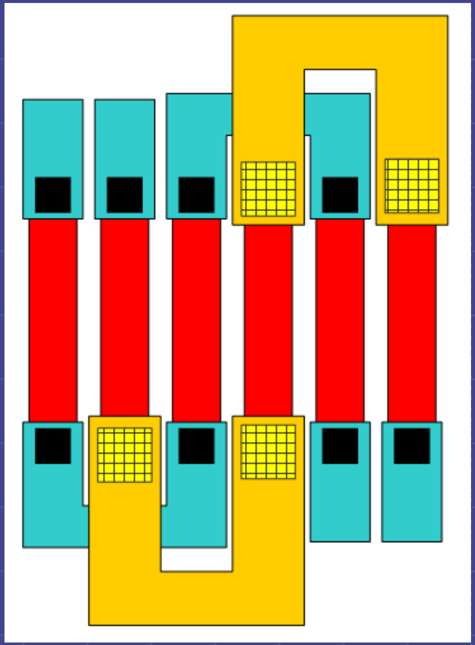


| | | | | | | | |
|---|---|---|---|---|---|---|---|
| R1 | R2 | R2 | R1 | R1 | R2 | R2 | R1 |
| R2 | R1 | R1 | R2 | R2 | R1 | R1 | R2 |

care matching

not care absolute value ↓





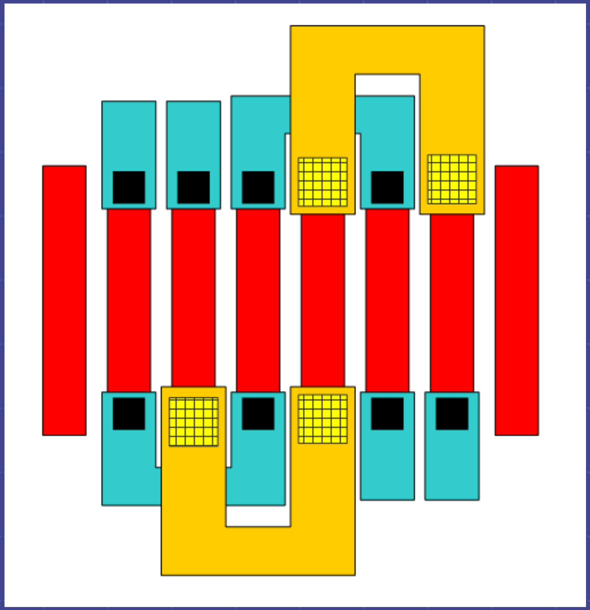
↑

finger layout

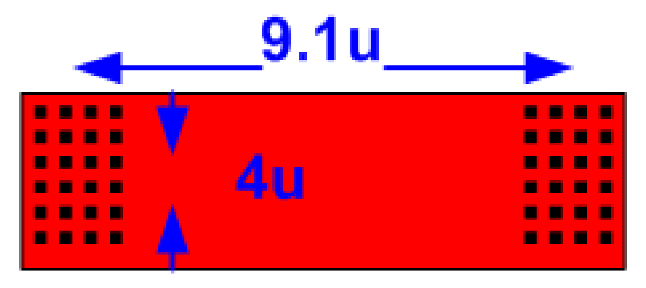
care matching

and absolute value

↓



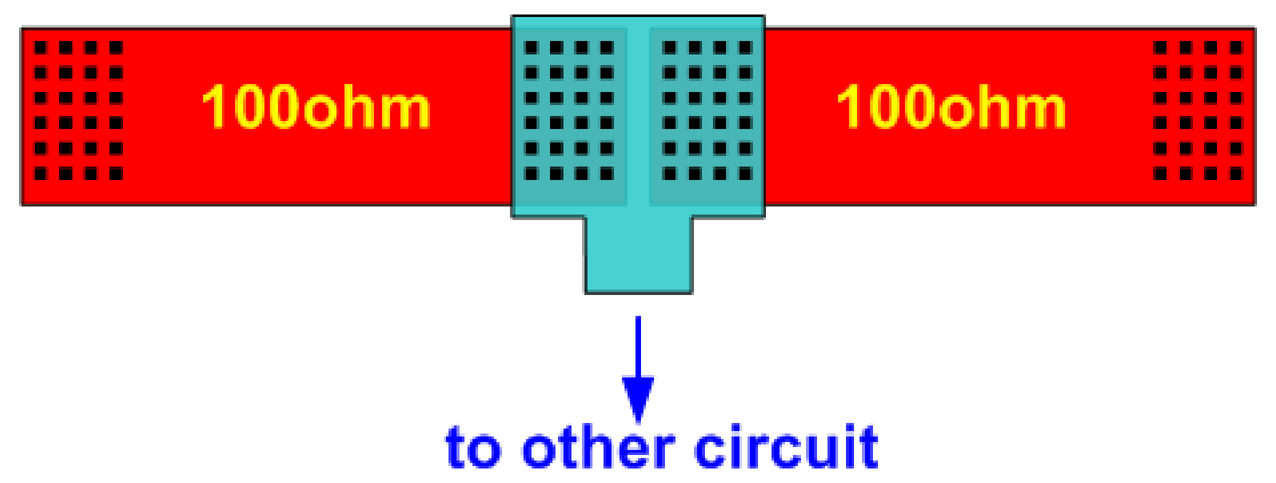
# Square

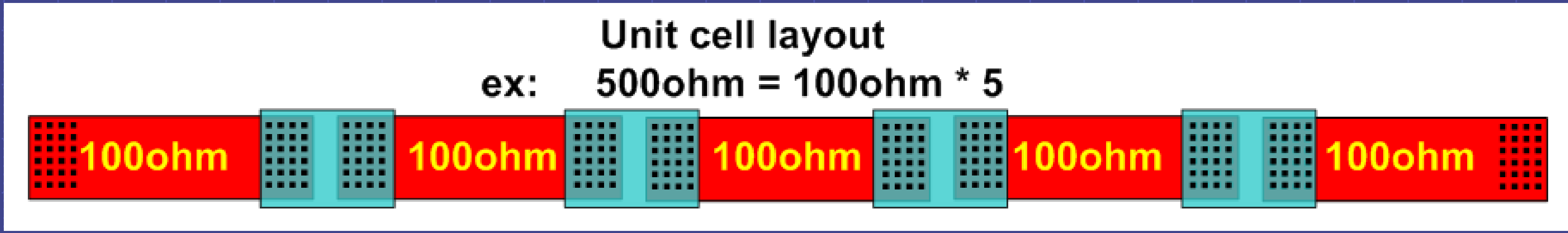


Poly 44 ohm/square

100/44 = 2.272 square

Length = 2.272*4 = 9.1u

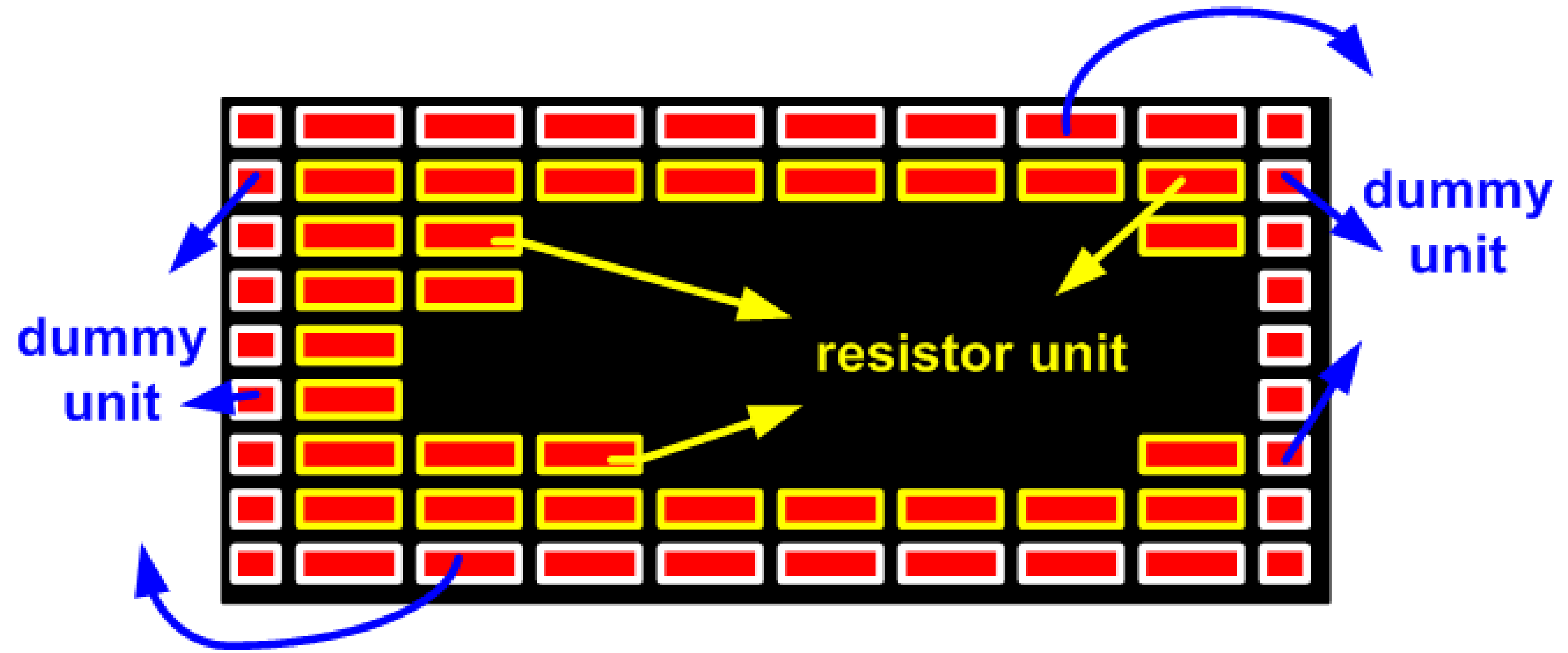




Unit cell layout

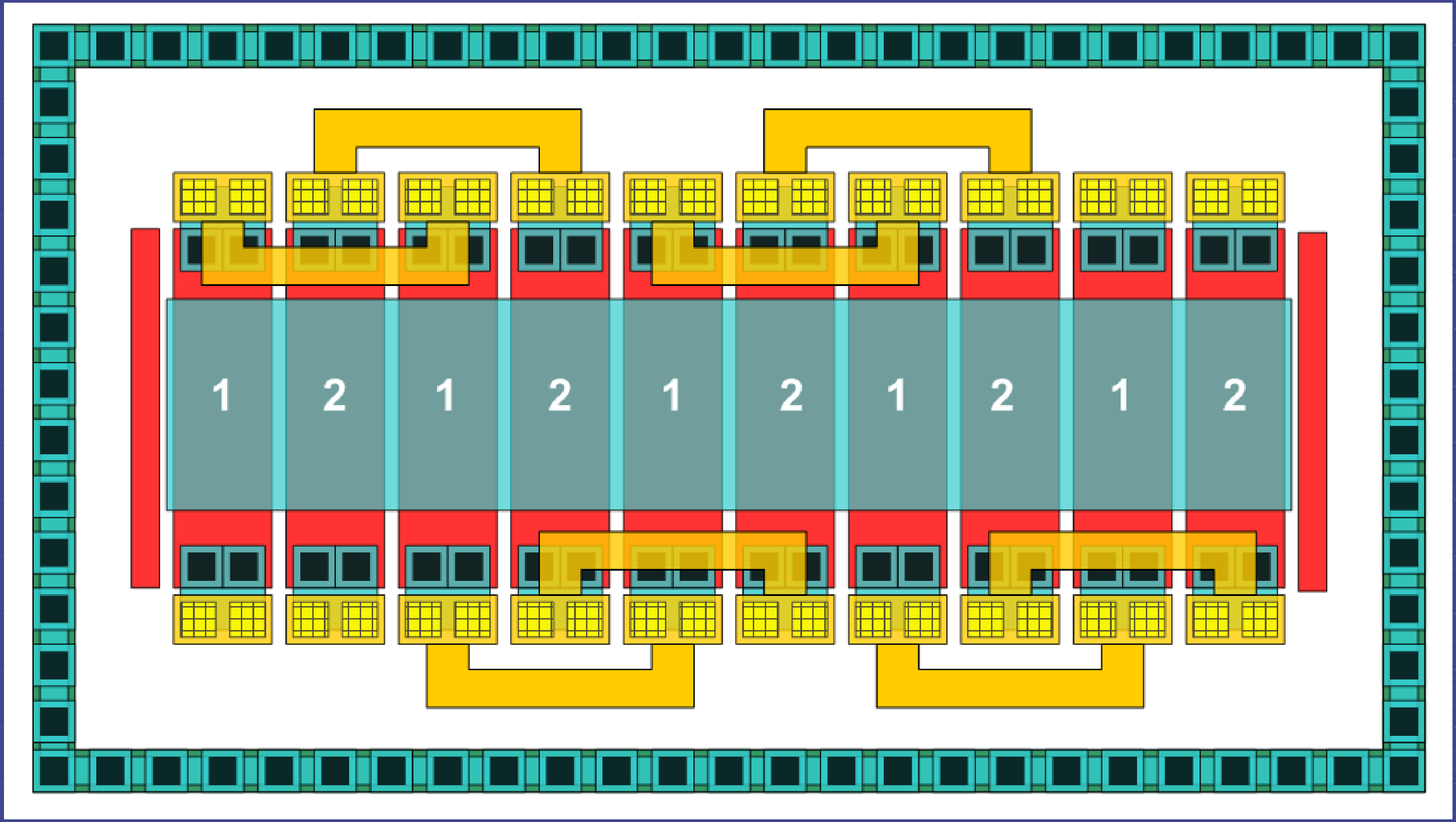
ex: 500ohm = 100ohm * 5

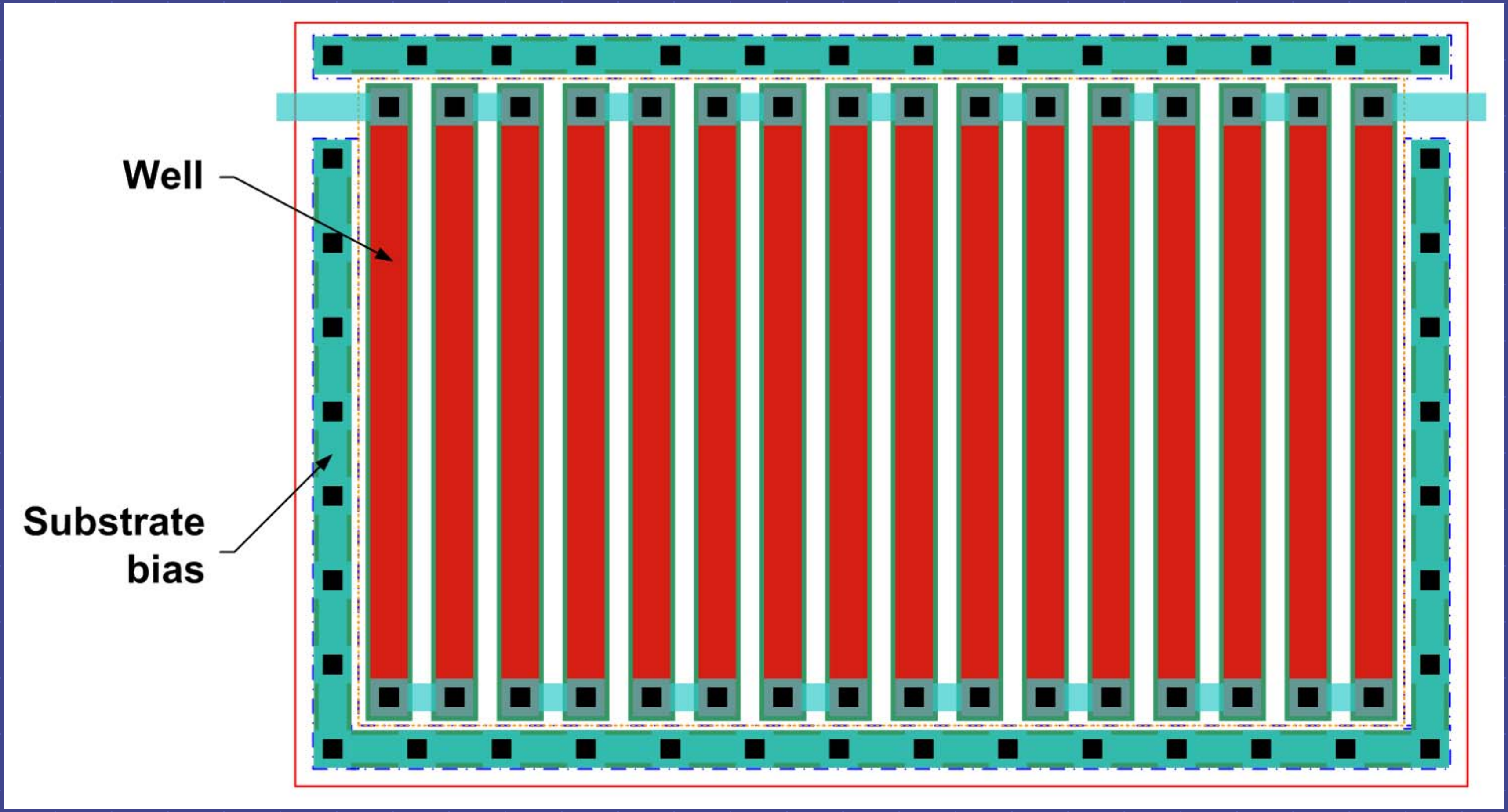
# Consideration of dummy



The resistor cells are layouted into square as possible add the dummy cells at four sides

# Crosses resistor




Well
Substrate bias

- Place shield under resistor that is connected to clean power supply

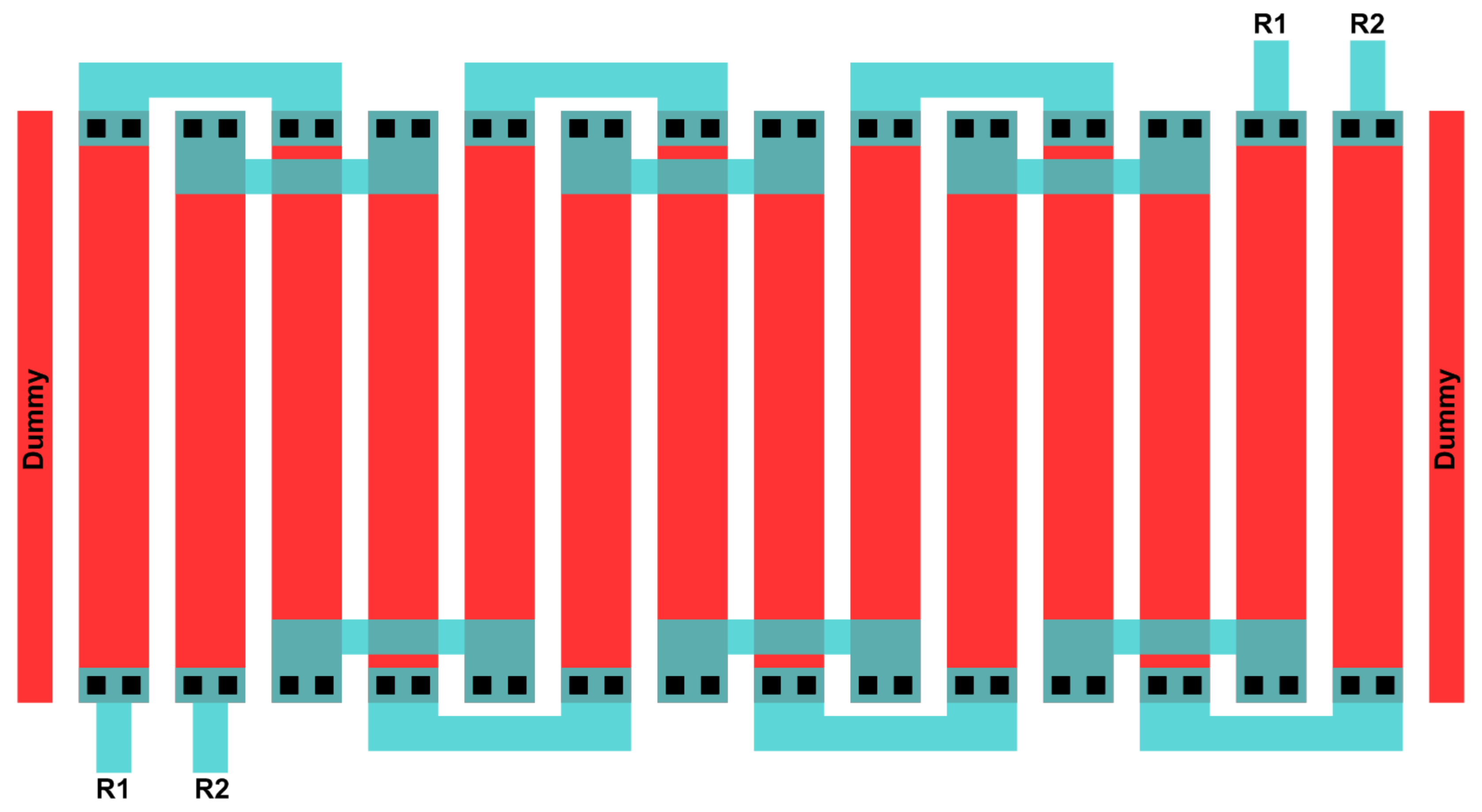
- N-well region to keep substrate noise from being injected into conductive layer

- Noise is due to capacitively coupling between substrate and a large resistor structure

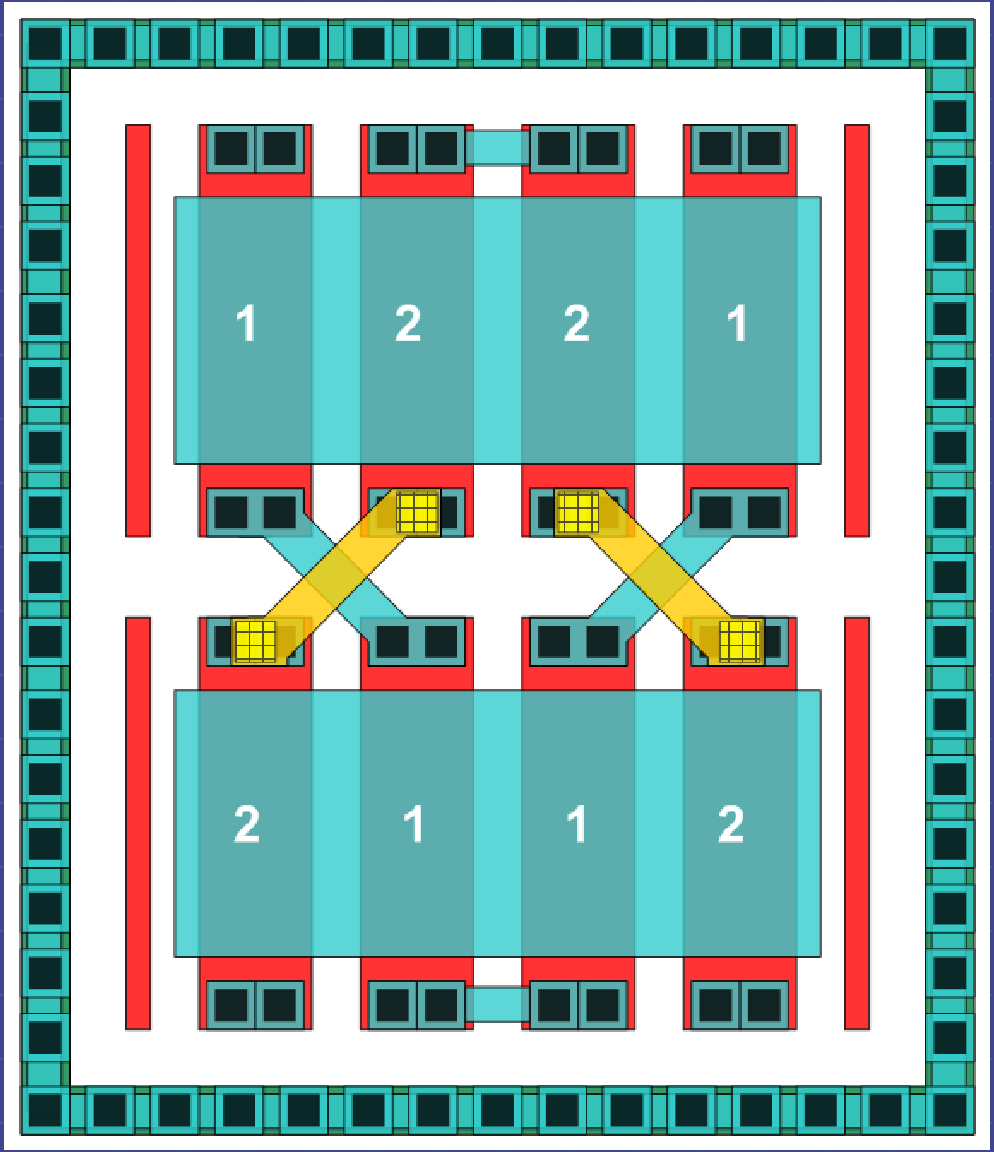
- The parasitic capacitor between resistor and the shield should be modeled during simulation

For low-noise design, a metal shield over the top maybe necessary

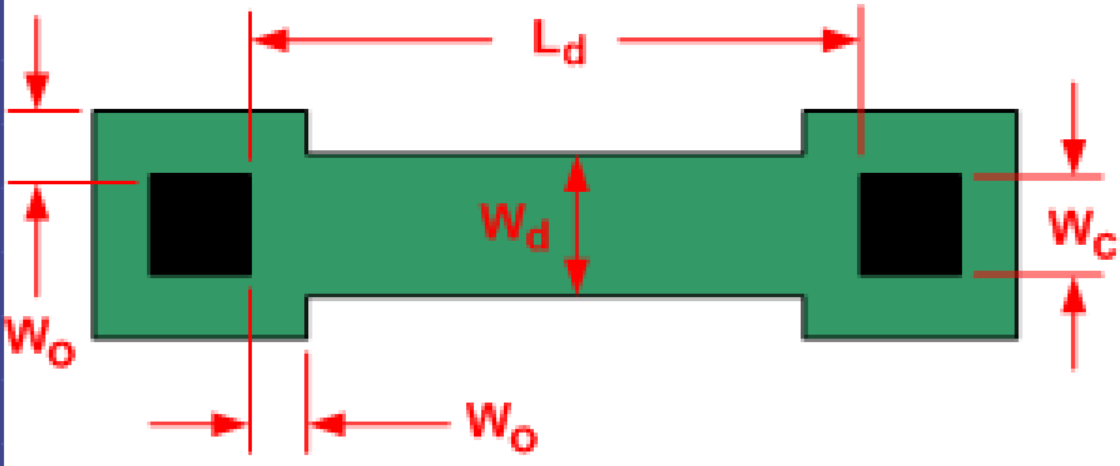
-- With resistor of high values ( KΩ or MΩ ), use n-well (or p-well)

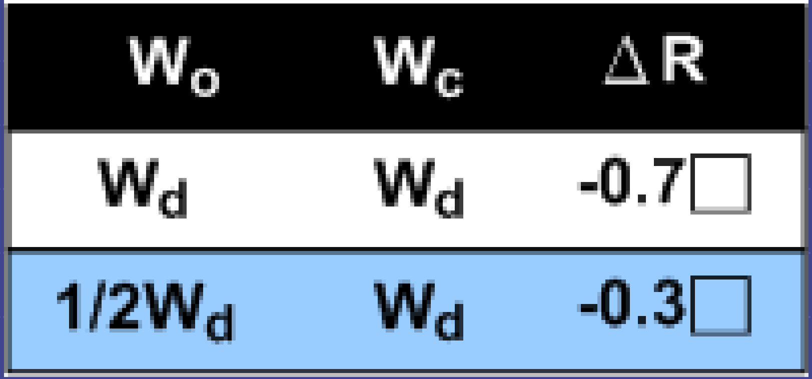

R1
R2
Dummy
Dummy
R1
R2

# Common Centroid



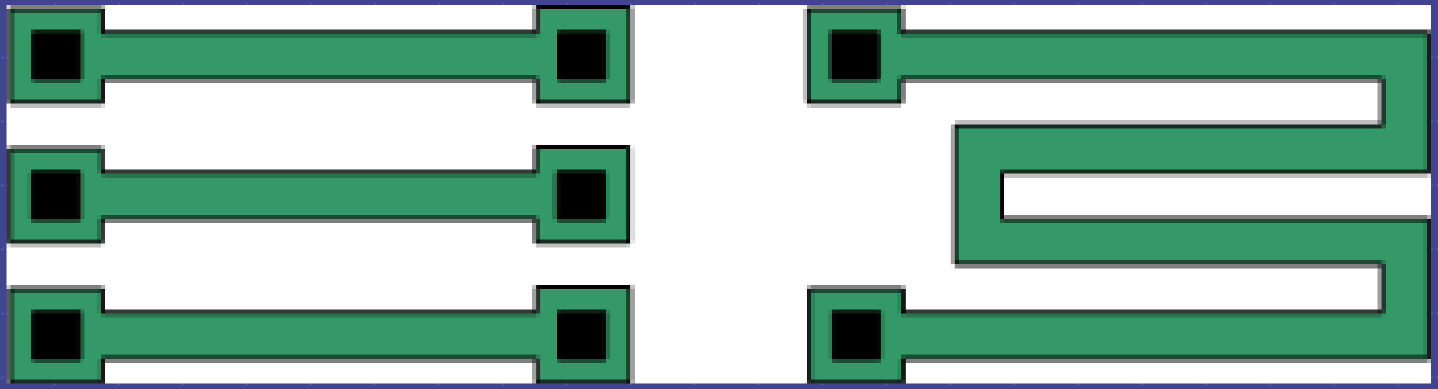
# Correction factors ΔR for dogbone resistors



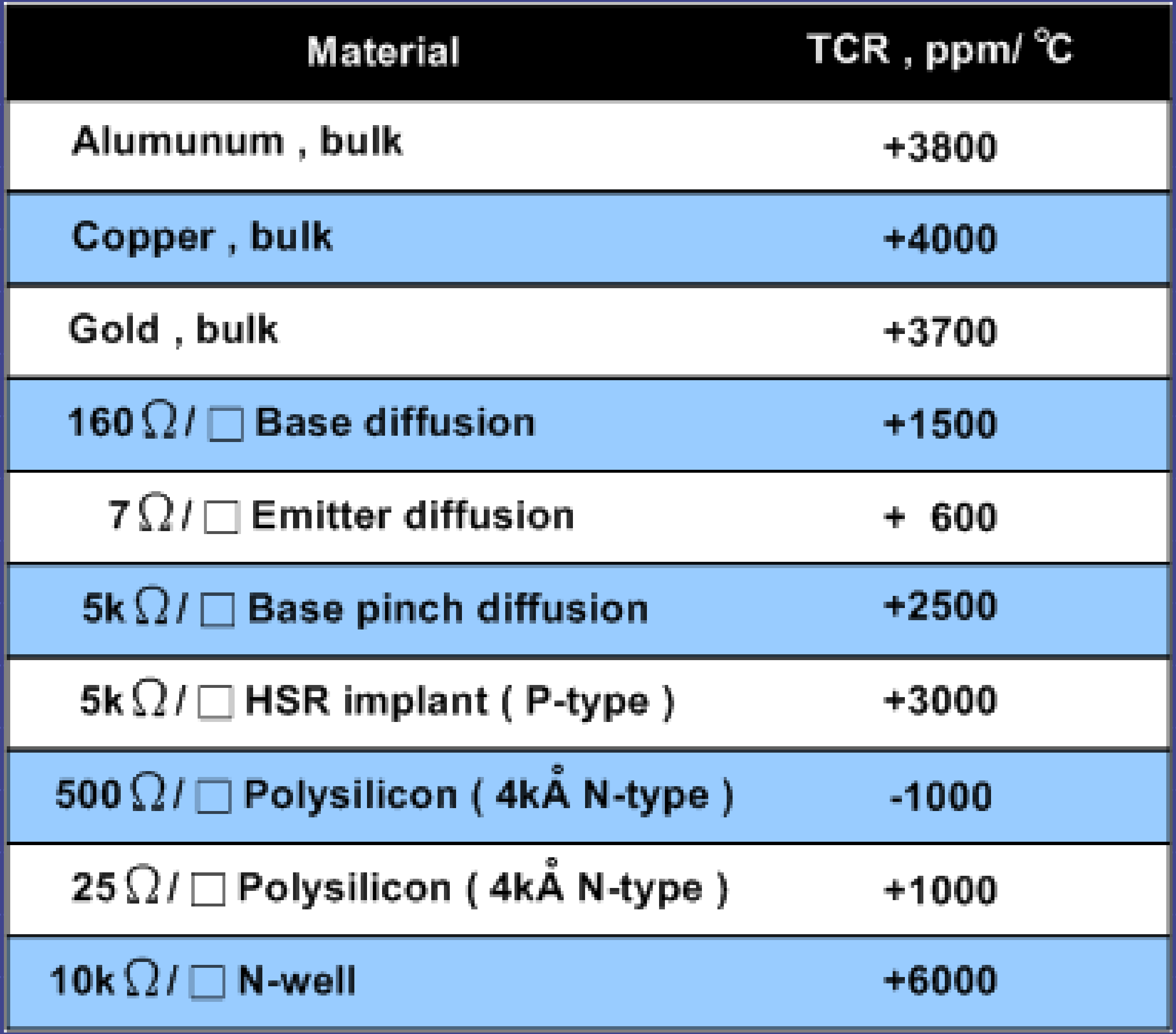


| $W_o$ | $W_c$ | ΔR |
|---|---|---|
| $W_d$ | $W_d$ | -0.7□ |
| 1/2$W_d$ | $W_d$ | -0.3□ |

# Sample dogbone and serpentine resistors,showing the poor packing density caused by the presence of enlarged heads

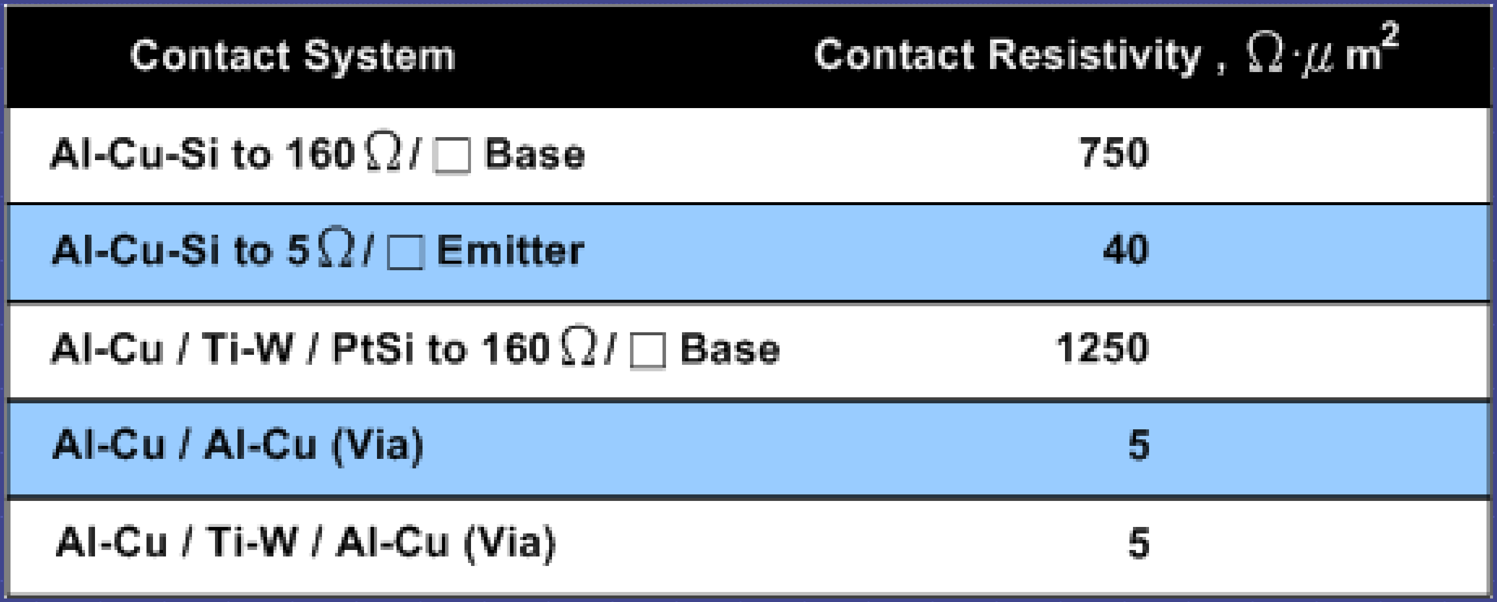


# Typical linear temperature coefficients of resistivity for selected materials at 25°C



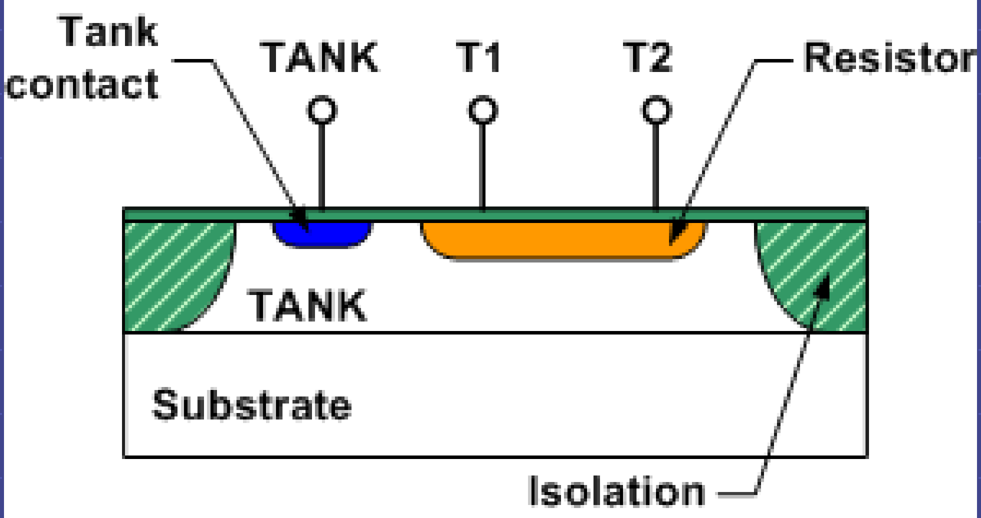
| Material | TCR , ppm/ ℃ |
|---|---|
| Alumunum , bulk | +3800 |
| Copper , bulk | +4000 |
| Gold , bulk | +3700 |
| 160 Ω/ □ Base diffusion | +1500 |
| 7 Ω/ □ Emitter diffusion | + 600 |
| 5k Ω/ □ Base pinch diffusion | +2500 |
| 5k Ω/ □ HSR implant ( P-type ) | +3000 |
| 500 Ω/ □ Polysilicon ( 4kÅ N-type ) | -1000 |
| 25 Ω/ □ Polysilicon ( 4kÅ N-type ) | +1000 |
| 10k Ω/ □ N-well | +6000 |

# Typical contact resistances for various contact systems.

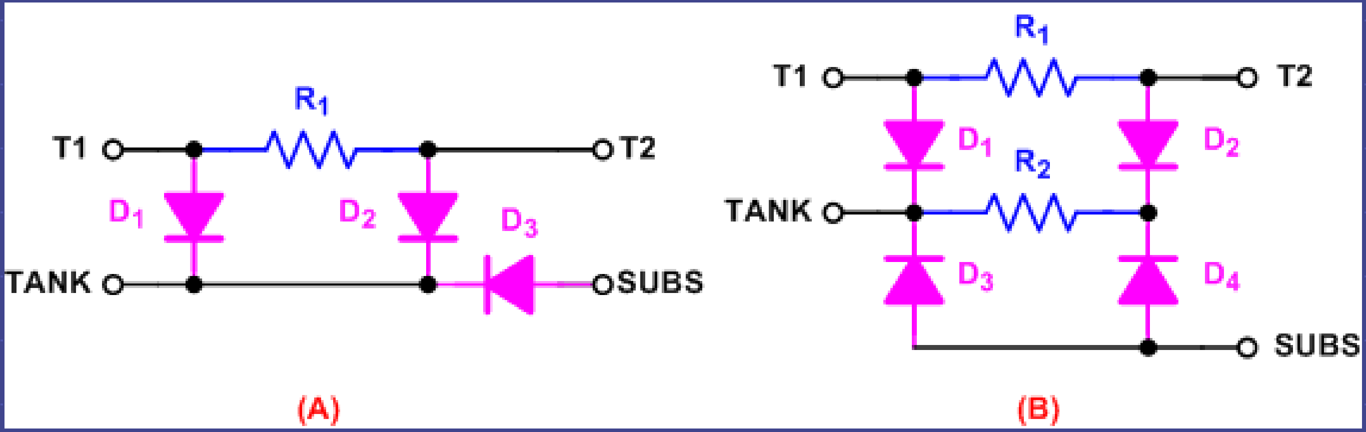


| Contact System | Contact Resistivity , $\Omega\cdot\mu m^2$ |
|---|---|
| Al-Cu-Si to 160 $\Omega$/□ Base | 750 |
| Al-Cu-Si to 5 $\Omega$/□ Emitter | 40 |
| Al-Cu / Ti-W / PtSi to 160 $\Omega$/□ Base | 1250 |
| Al-Cu / Al-Cu (Via) | 5 |
| Al-Cu / Ti-W / Al-Cu (Via) | 5 |

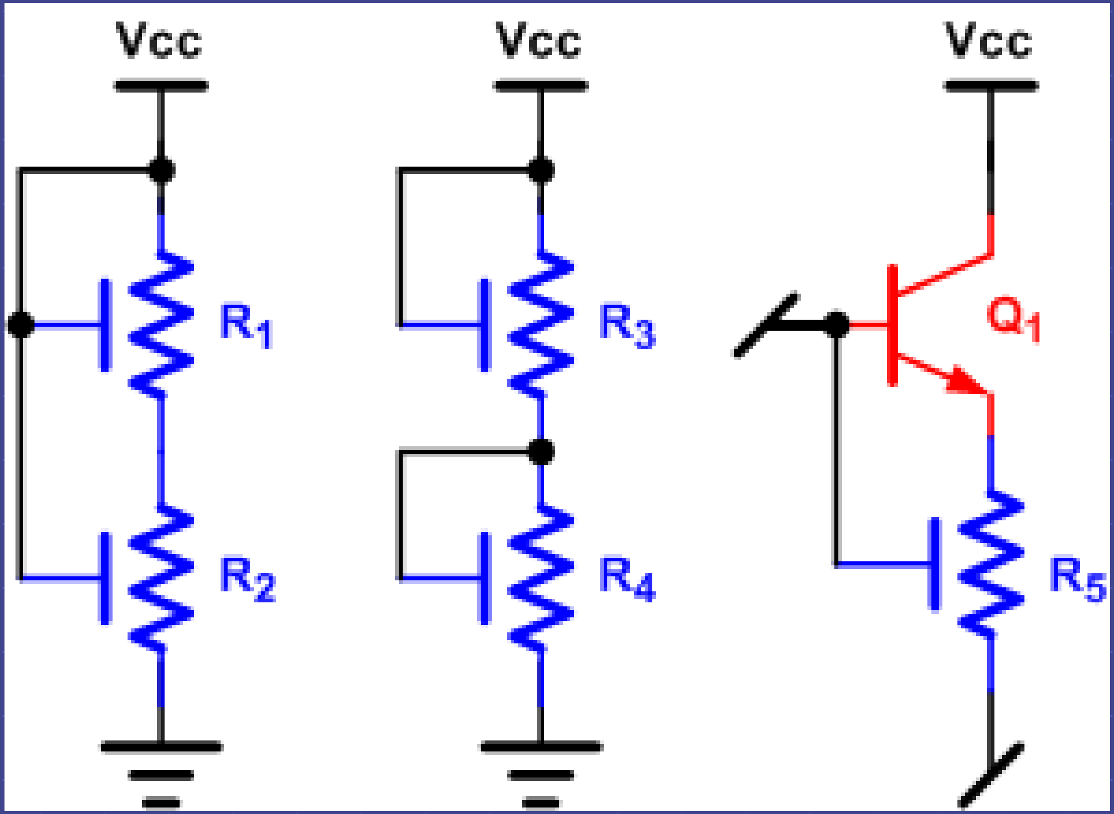
# Cross section of a typical diffused resistor.



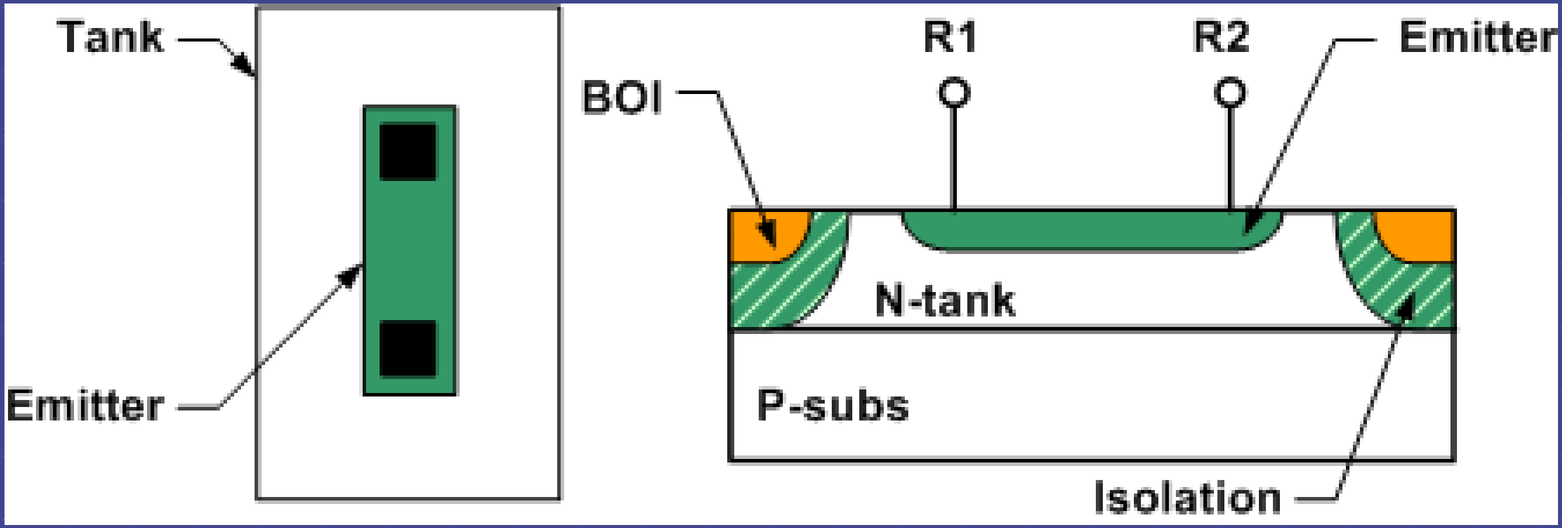
## Subcircuit models for diffused resistors (a) neglecting tank resistance and (b) including tank resistance



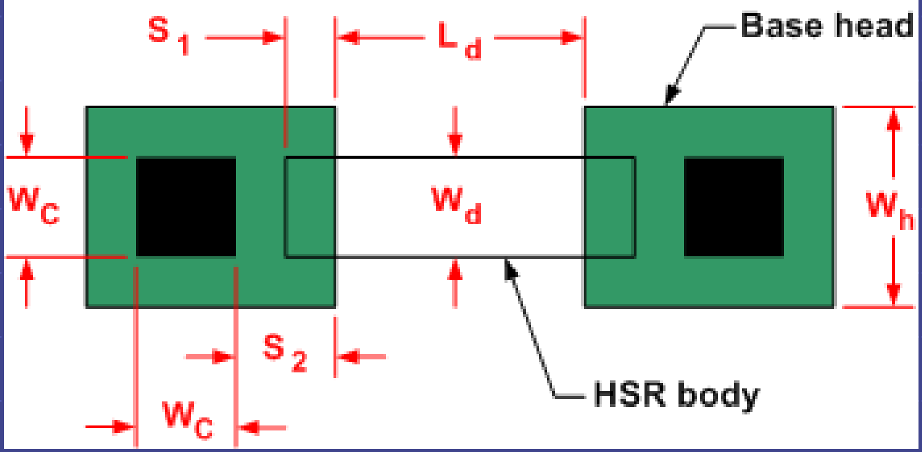
# Several methods of biasing the tank connections of diffused resistors.



# Layout and cross section of an alternate style of emitter resistor that eliminates the enclosing base diffusion to save space.

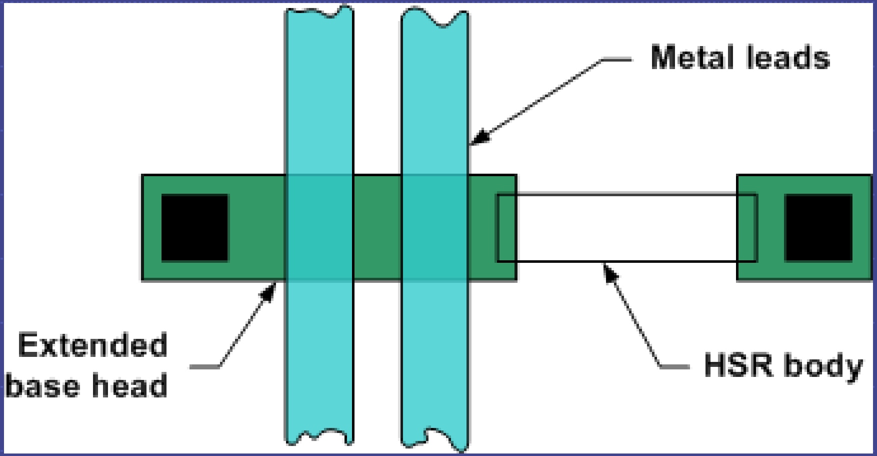


# Layout of an HSR(High-sheet-resistance) resistor, showing relevant dimensions.

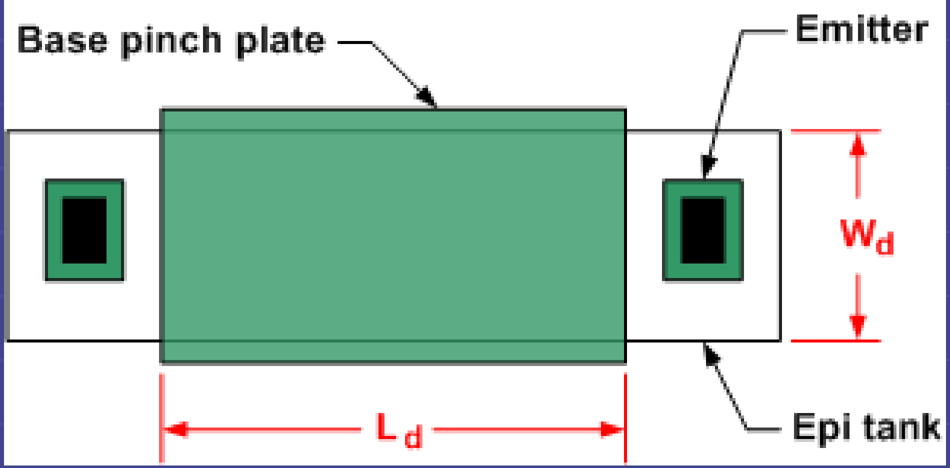


R = Rs[(Ld-Lb)/(Wd-Wb)+2Rh

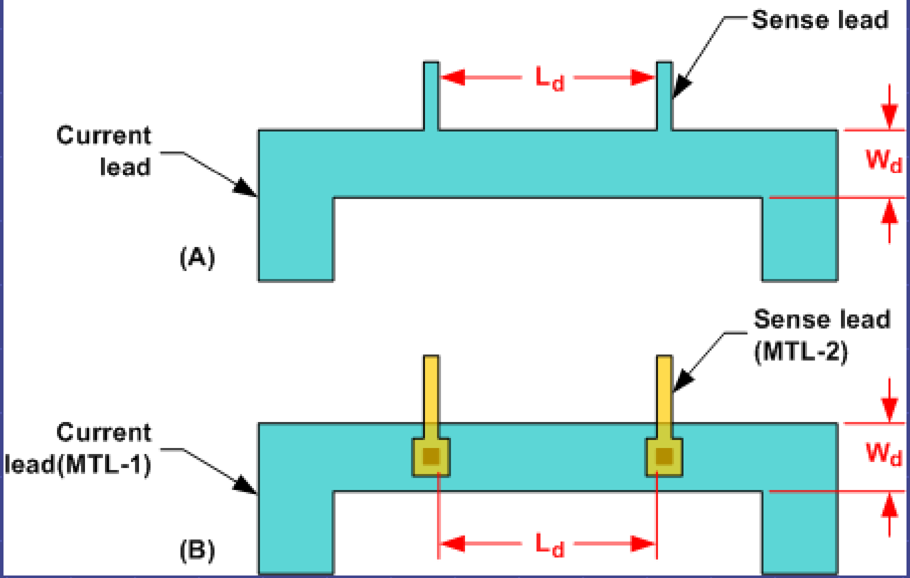
# Example of an HSR resistor with an extended head



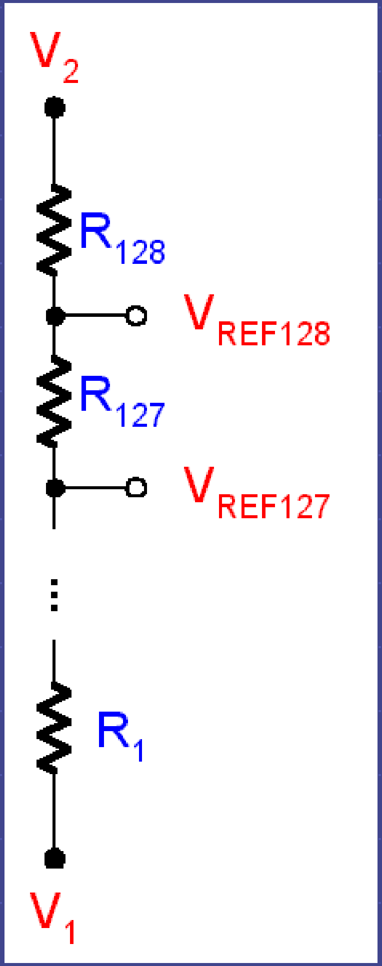
# Layout of an epi pinch resistor (epi-FET).



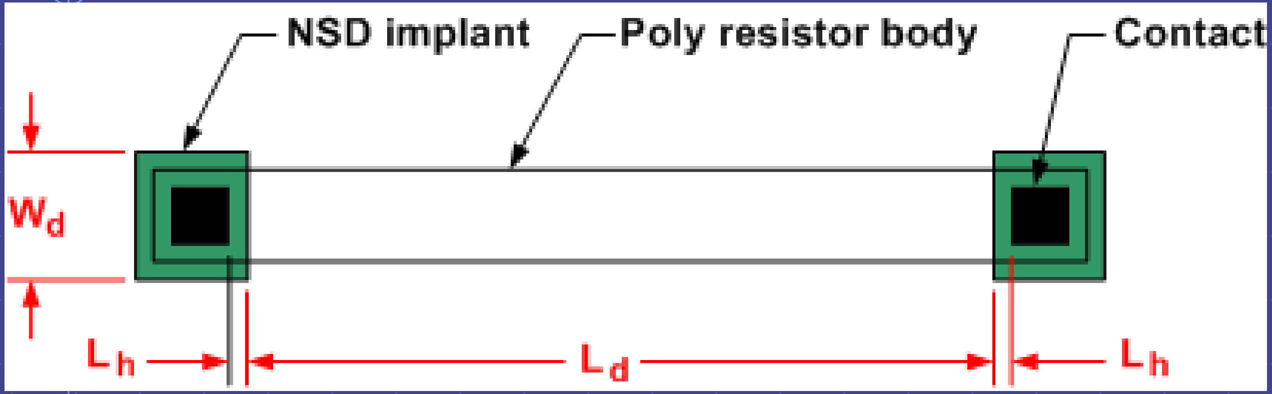
# Two styles of Kelvin-connected metal sense resistors (a) single-level-metal layout and (b) double-level-metal layout.



# Resistor ladder used in an A/D converter



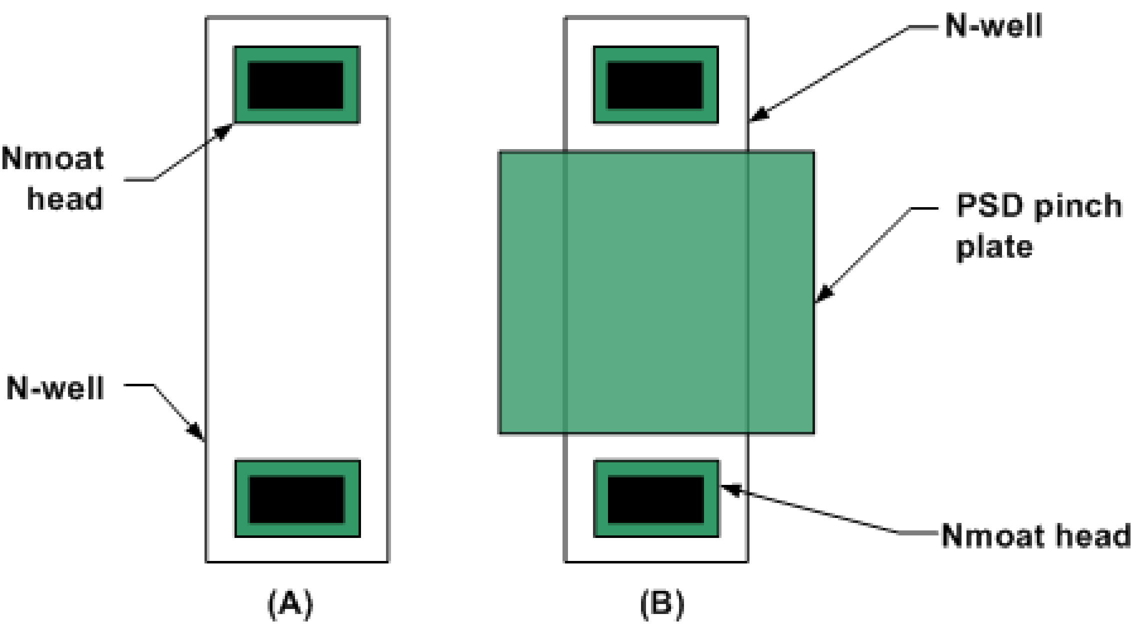
# High-sheet poly resistor with implanted heads.



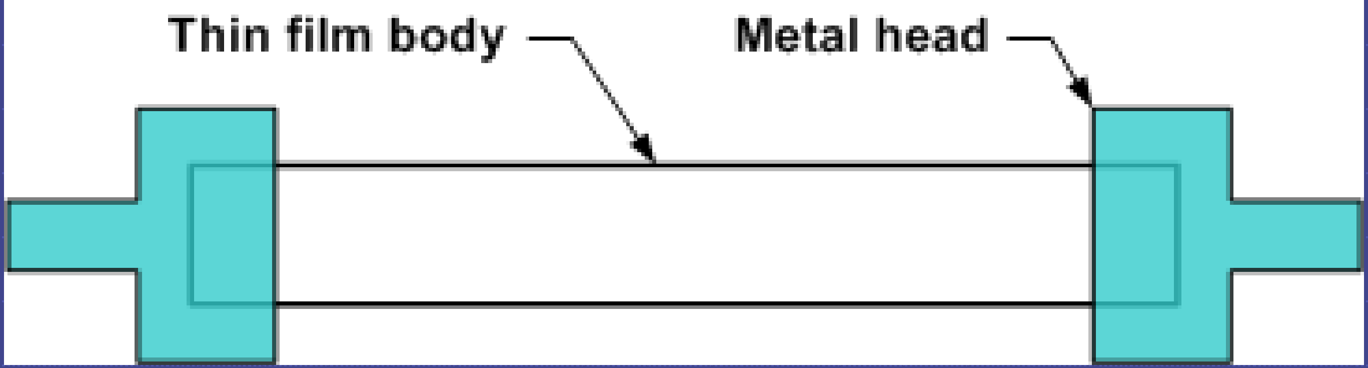
R = Rs[Ld/(Wd+Wb)

+2Rh[Lh/(Wd+Wb)]

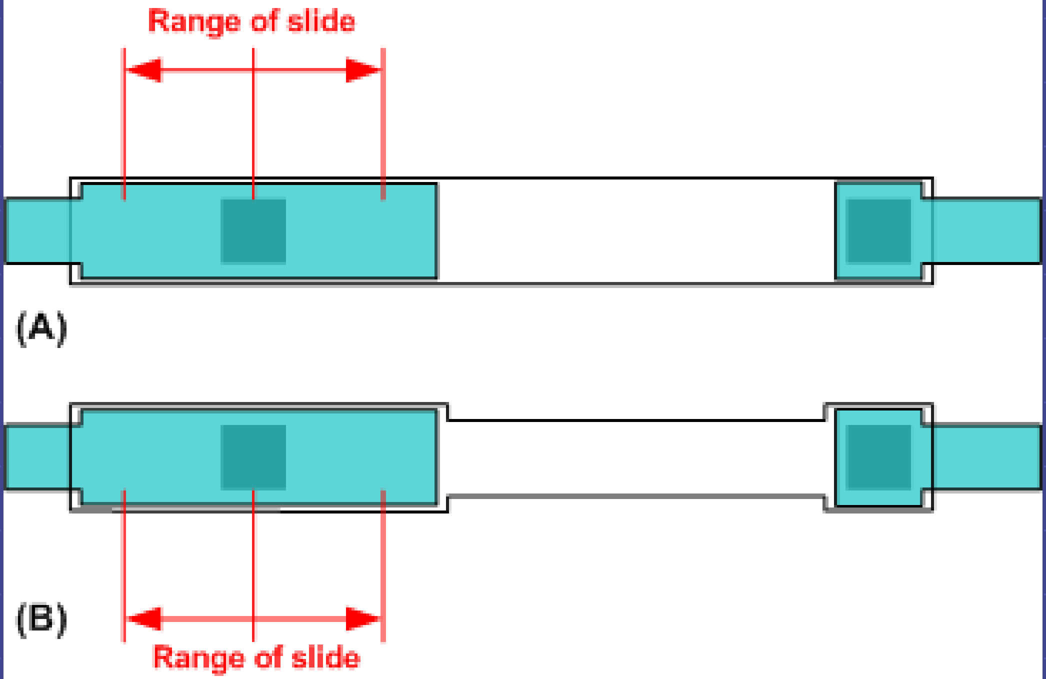
# (a) N-well resistor and (b) N-well resistor with PSD pinch plate (field plates not show.



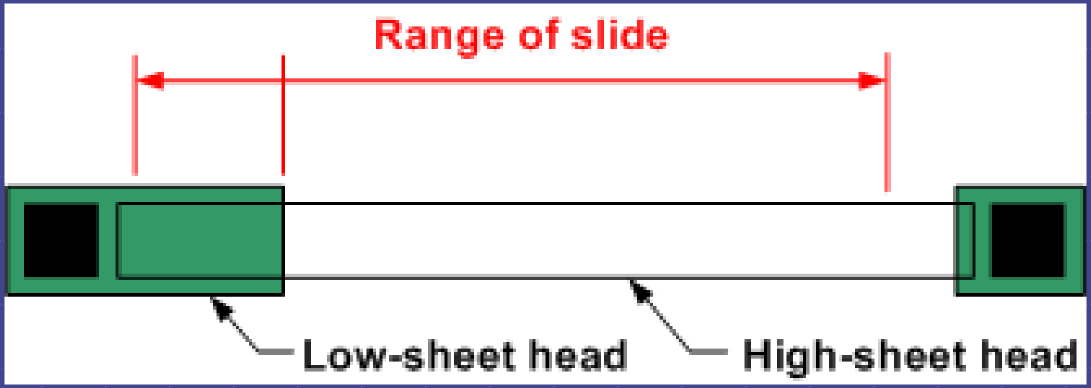
# Layout of a thin-film resistor.



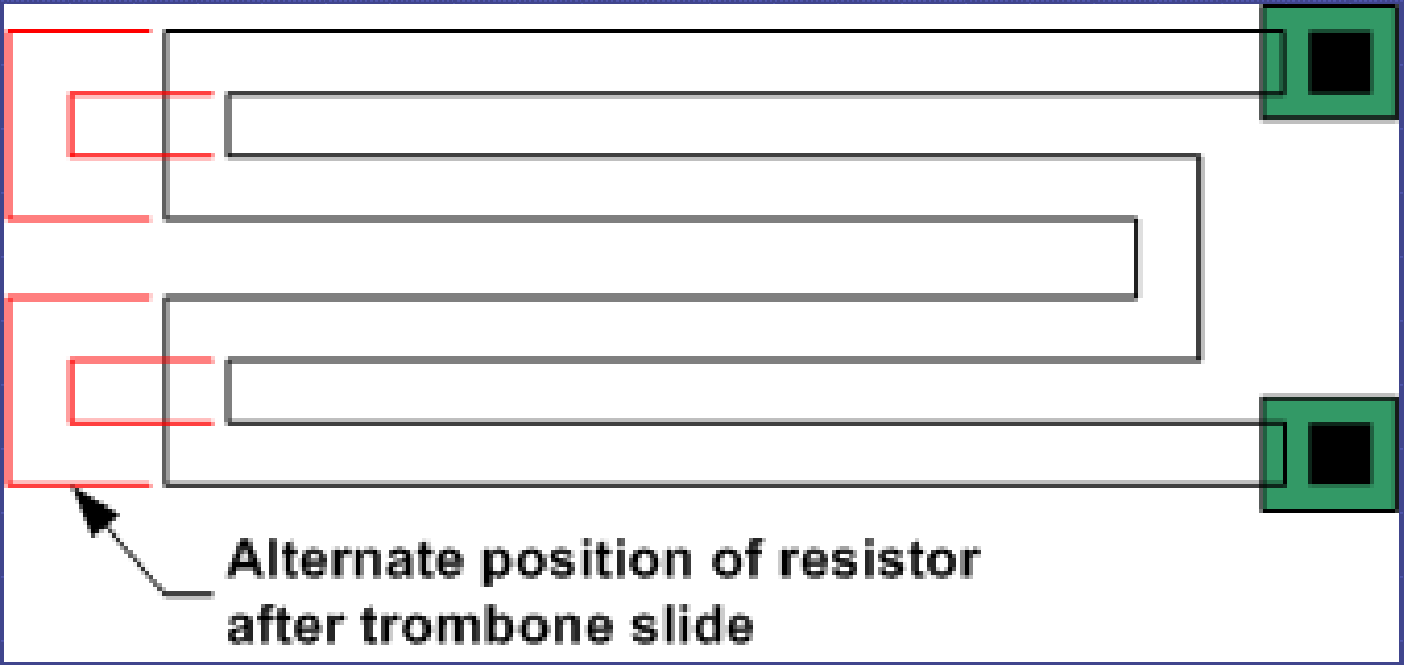
# Two styles of sliding contacts (a) without heads and (b) with heads.



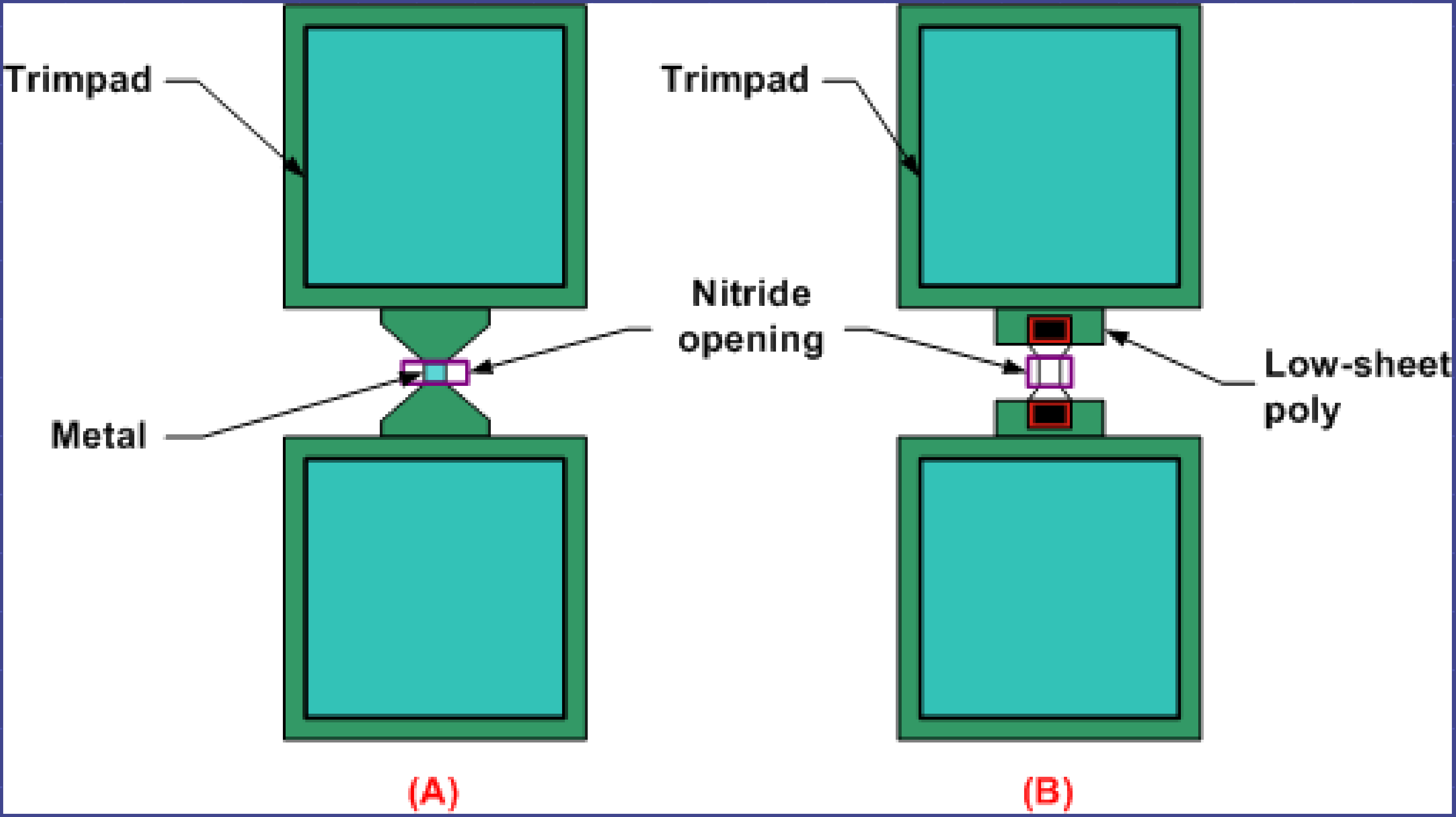
# Layout of a resistor with a sliding head.



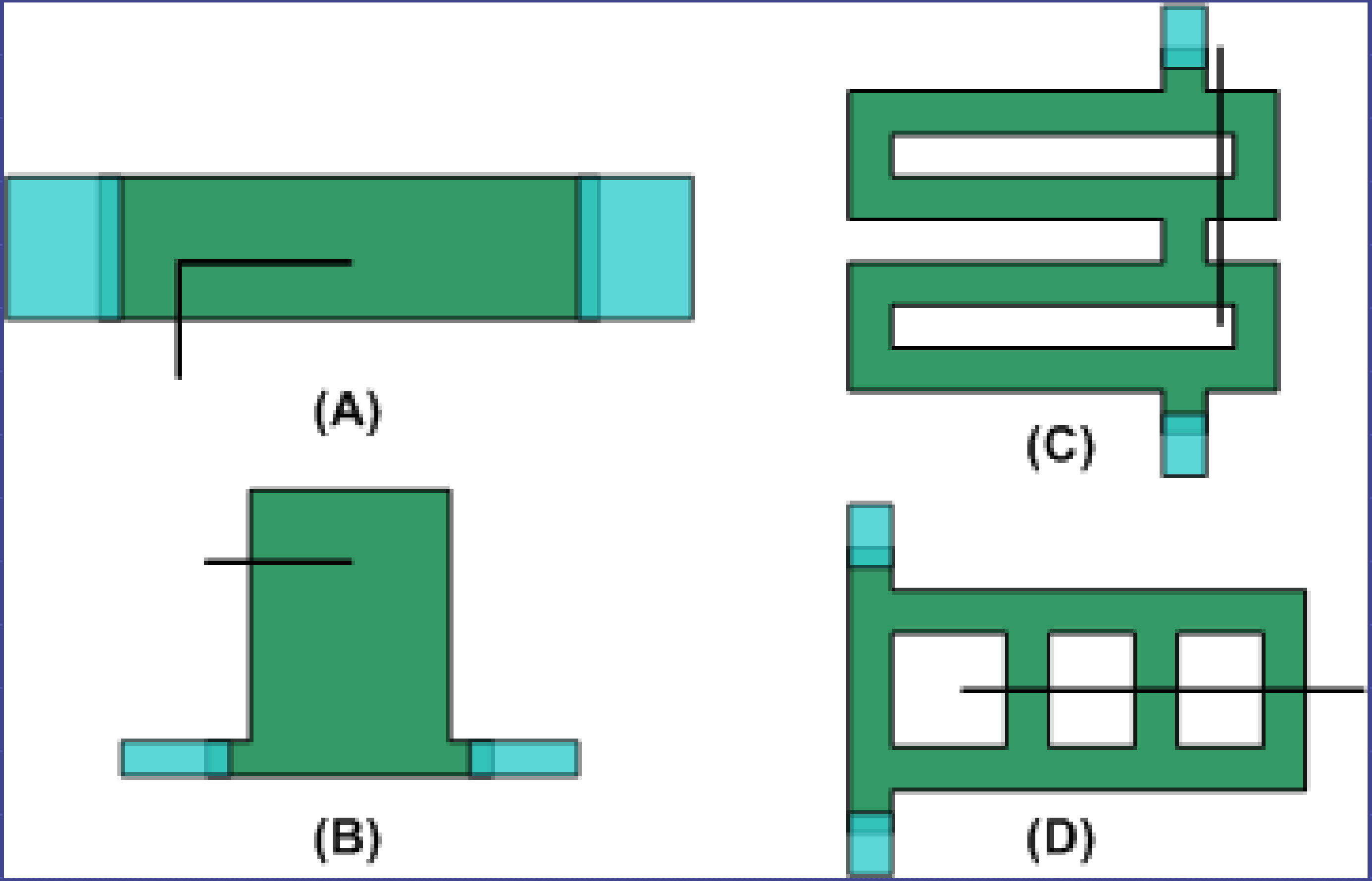
# Resistor adjustment by means of a trombone slide.



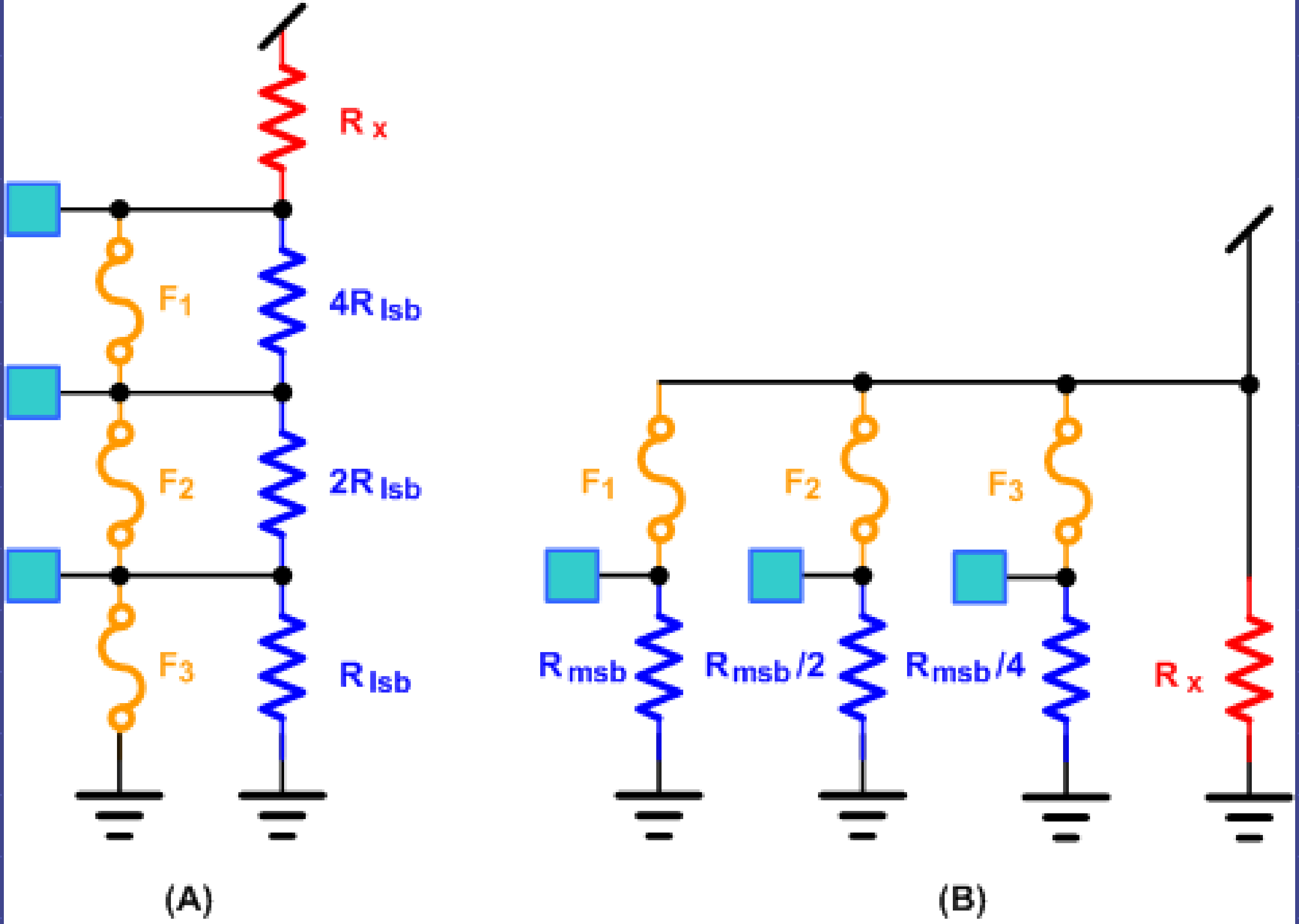
# Layouts of (a) a typical metal fuse and (b) a polysilicon fuse.



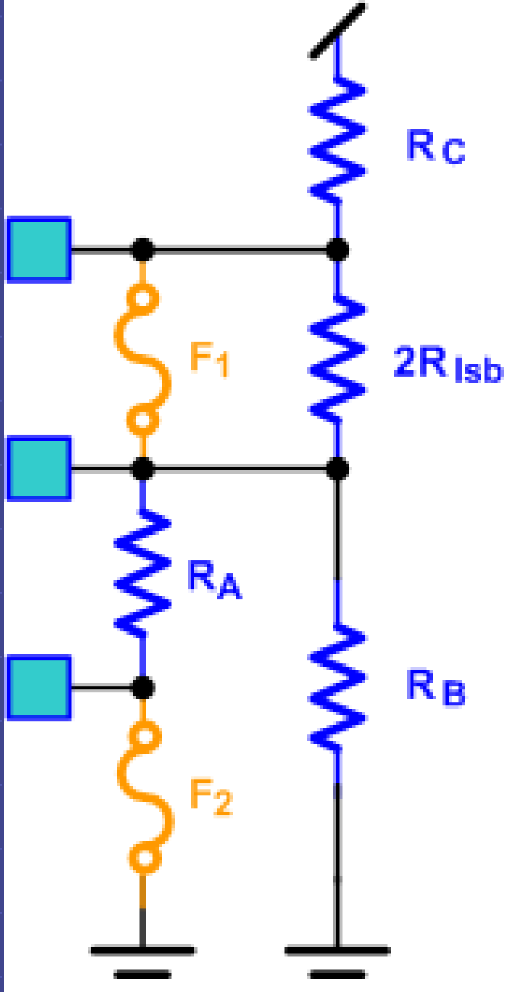
# Four different schemes for laser-trimming thin-film resistors (a) notched bar, (b) tophat, (c) looped layout, and (d) ladder layout. The heavy black lines show the path of the laser beam through the resistor.



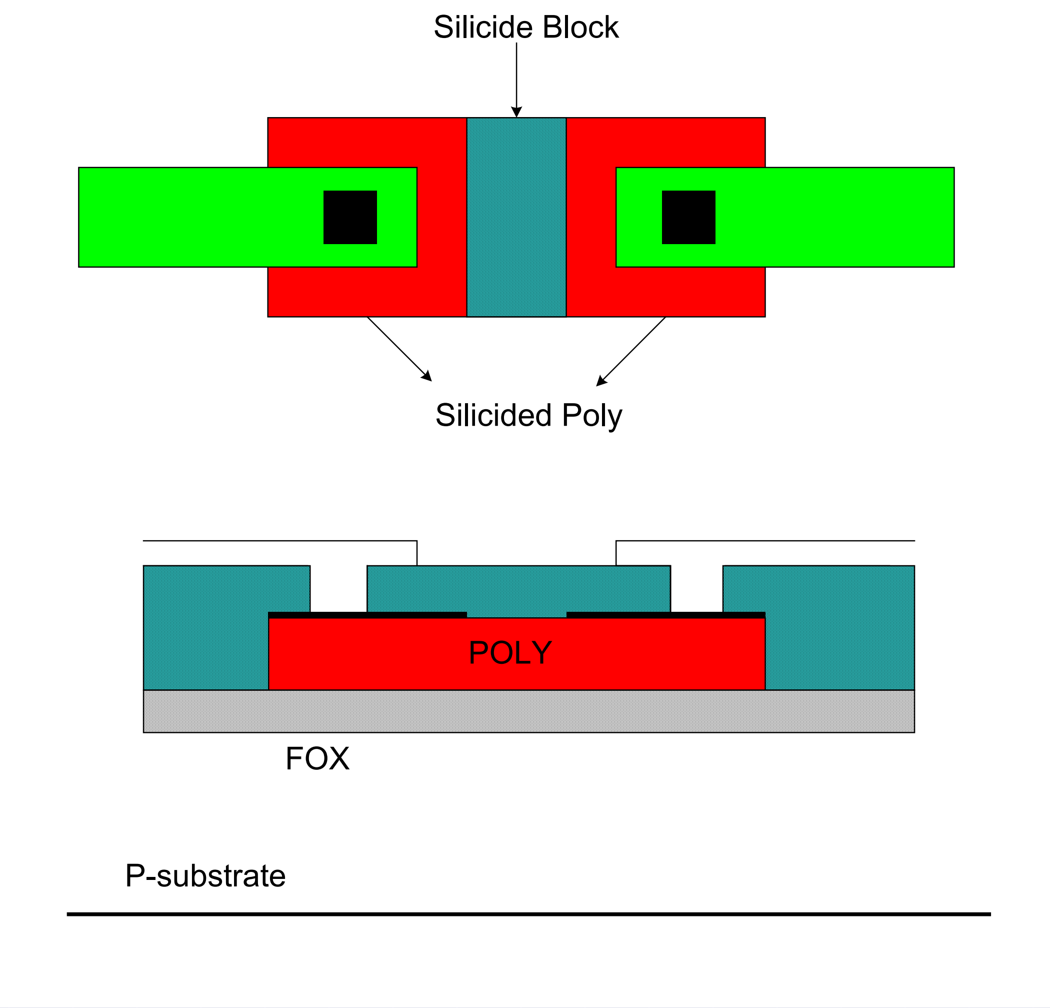
# Two different binary-weighted resistor trim schemes using fuses (a) series-connected and (b) parallel-connected. Both cases assume that the ground pad is used to program the fuses.



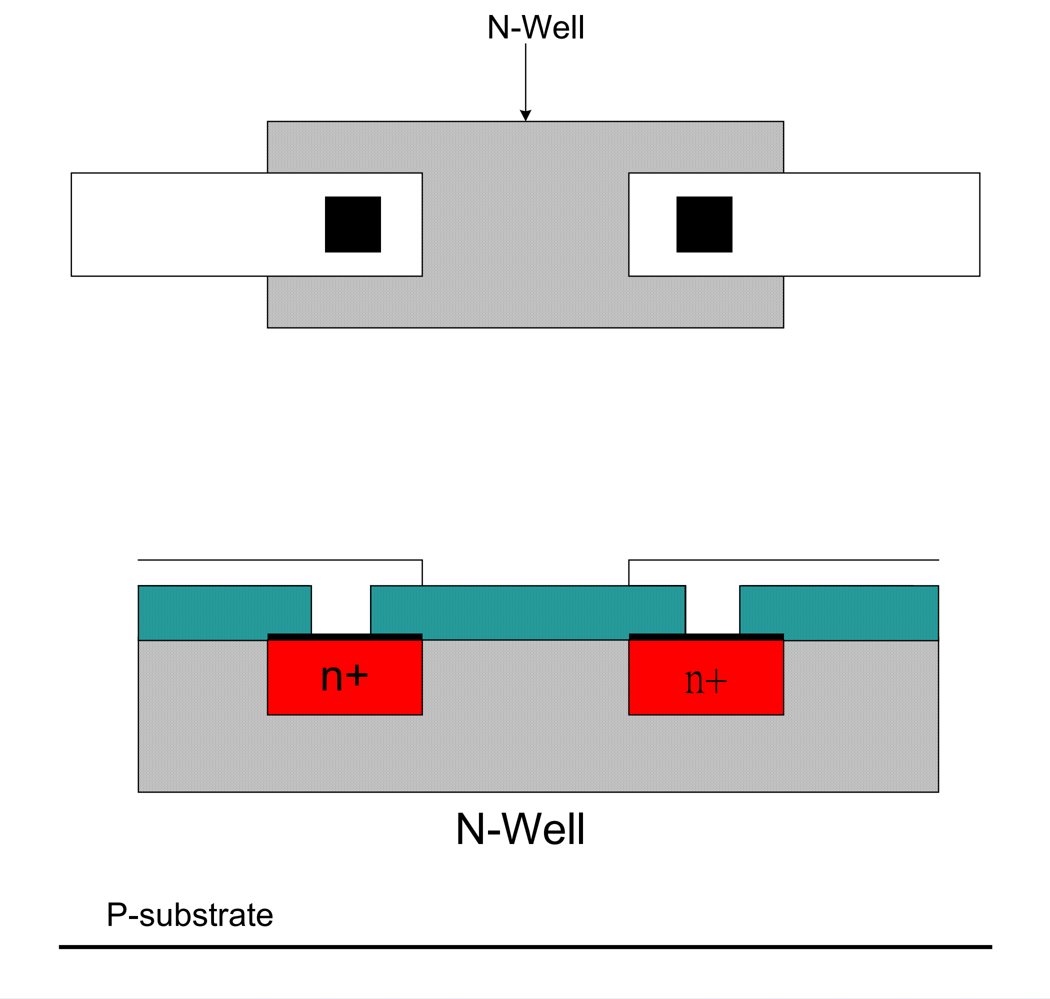
# Differential trim scheme applied to the LSB fuse, $F_2$, of a series-connected binary-weighted trim network.

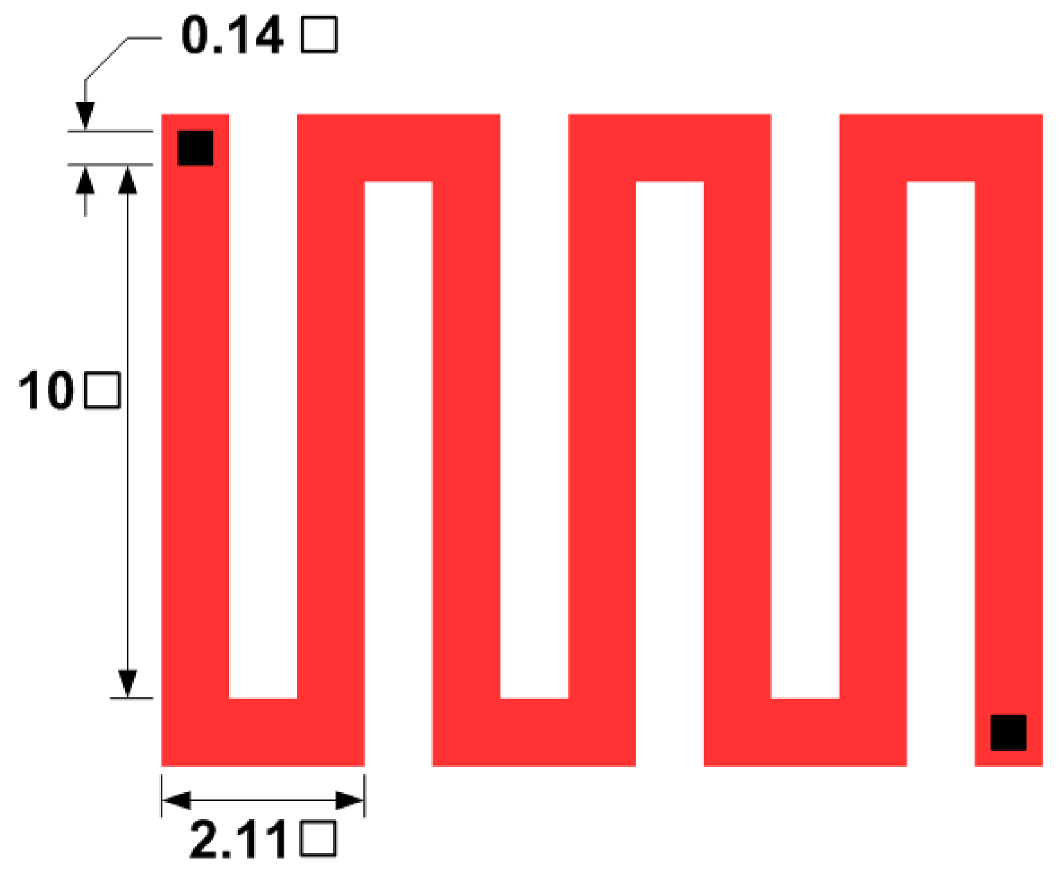


# The Silicide Block of Poly Resistor



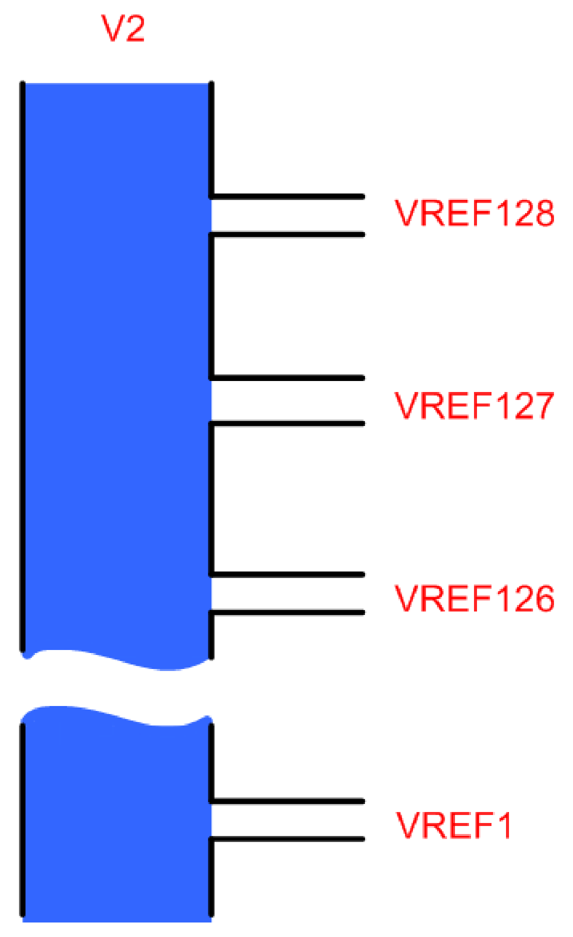
# N-Well Resistor

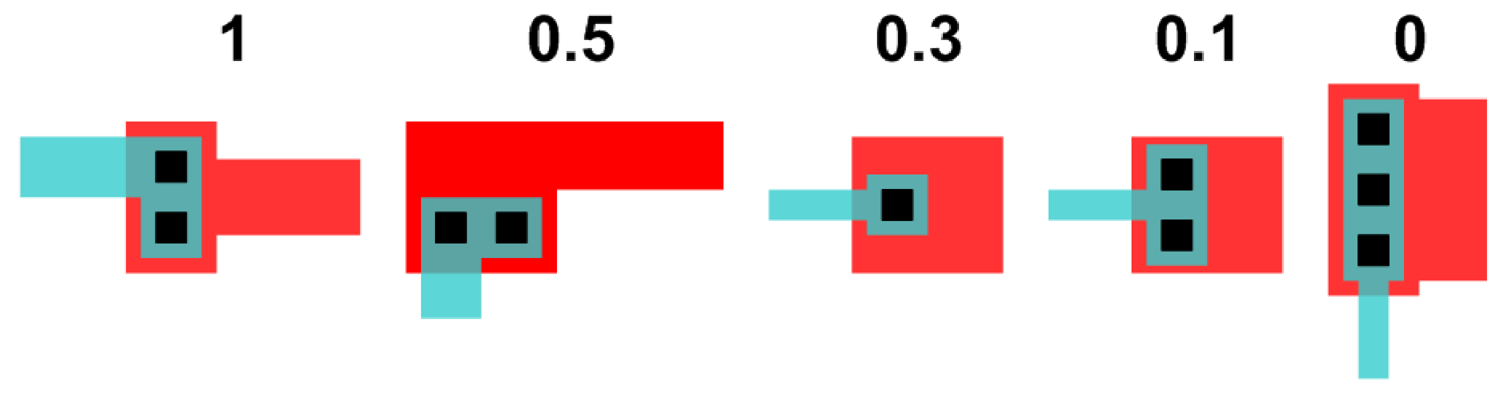




R = 82.94□ × 20Ω/□=1.659k Ω

# Resistor Ladder Made of Metal




1
0.5
0.3
0.1
0

## Minimal Matching

±1% three-sigma matching
6-7 bits of resolution
Degenerating current mirrors in biasing circuitry

## Moderate Matching

±0.1% three-sigma matching
9-10 bits of resolution
±1% bandgap references, op-amp and comparator input stage and most other analog applications

## Precise Matching

±0.01% three-sigma matching
13-14 bits of resolution
ADC DAC
Capacitors can more easily obtain this level of matching than resistors

# Rules for Resistor Matching

1. Construct matched resistors from a single material
- Process variations cause unpredictable shifts in the value of resistors relative to the other.
- Differing temperature coefficients of two materials prevent them from tracking over temperature.

2. Make matched resistors the same width
- Uncorrelated process bias cause systematic mismatches in resistor of different widths.
- If one resistor must be made wider than another, constructing wider resistor from a number of sections connected in parallel.
- Width effects are not entirely independent of temperature and stress, even if resistors are trimmed, they should still consist of sections of a uniform width.

## 3. Make matched resistors sufficiently wide

- Matching resistors > 30 squares (e.g. minimal allow width 2um)
  minimal matching, 150% minimal allowable width (3um)
  moderate matching, 200% minimal allowable width (4um)
  precise matching, 400% minimal allowable width (8um)
- Matching resistors 20-30 squares, consider increasing the width
- Matching resistors > 100 squares, consider reducing the width

## 4. Use identical geometry for resistors

- Corner and end effects prelude precise matching of resistor have different geometries.
- Same width, but different lengths or shapes, mismatches ± 0.1% or more.

## 5. Orient matched resistors in the same direction

- Resistor oriented in different directions may vary by several percentage.
- Diffused resistors show largest orientation mismatches.
- Most resistors should oriented vertically or horizontally.
- P-type poly diffused resistors on <100>-oriented experience less stress-induced variation if oriented 45º to X- and Y-axes.

## 6. Place matched resistors in close proximity.

- Minimal matched, spaced a few mils apart
- Moderate matched, placed adjacent
- Precise matched, interdigitated
- Dice area > 16mm$^2$, power > 250mW, heat-sunk package, junction-to-ambient temp. > 20ºC, mounted using solder or gold eutectics experience larger mismatches. Minimal matched, placed adjacent. Moderate and precise matched, arrayed or interdigitated.

## 7. Interdigitated arrayed resistors.

- Aspect ratio of array < 3:1
- Length of each segment should be at least 5X (preferable 10X) of its width
- Interdigitated patterns obeys the rules of common centroid.
- Even number of segments per resistor to obtain better rejection of thermoelectrics.
- Consider connecting some segments in parallel if this will reduce the total area.
- If the arrays requires a large number of segments, considering arranging these into multiple banks connected to form a two-dimensional arrays.

## 8. Place dummies on either end of a resistor array.

- Arrayed resistors should include dummies.
- Poly dummies need not have the same width.
- Diffused dummies should always have the same geometry as adjacent.
- Keep spacing between adjacent segments constant.
- Connect dummies to a quite low-impedance node.

## 9. Avoid short resistor segment.

- Very short resistor segments may introduce considerable variation due to contact resistance.
- Moderate matched > 5 squares
- Precise matched > 10 squares
- Precise matched poly resistor, total length > 50um, to minimize nonlinearities and granularity.

## 10. Connect matched resistors in order to cancel thermoelectrics.

- Arrayed resistors should be connected so that equal number of segments are oriented in either direction of X- and Y-axes.
- Serpentine resistors should be constructed so that their heads lie near one another.

## 11. If possible, place matched resistors in low stress areas.

- Minimal stress in the middle of die
- If precise matched resistor must reside to an edge, they should be placed near the middle of one side of the die, preferable the longer side.
- Maximum stress in the die corners.

## 12. Place matched resistors well away from power devices.

- Power device > 50mW, Major power devices > 250mW
- 200-300um away from major power devices, 100um from power devices.
- Optimum symmetry arrangement
- P-type diffused resistors exhibit less package shift on (100)-silicon, but this arrangement preludes placement on an axis of symmetry of power devices.
- If large thermal gradient, resistors arrayed vertically or horizontally.
- Thermal gradients produce more mismatch than stress gradients.
- Interdigitated as devices next to power devices.

## 13. Place precise matched resistors on axes of symmetry of die.

- On (100)-silicon, resistor aligns with one of the two axes.
- P-type diffused resistor benefits from diagonal orientation.
- If large amount of resistors exist, reserve the optimal location for the most critical devices.

## 14. Consider tank modulation effects.

- Significant for
  precise matched resistors with sheet resistor 100Ω/□
  moderate matched resistors with sheet resistor 500Ω/□
  minimal matched resistors with sheet resistor 1000Ω/□
- Substitute poly resistors for diffused resistors where possible
- If diffused resistors are employed, use low sheet resistor (e.g. 160 Ω/□) material will allow merging the matched resistors into a common tank

## 15. Sectioned resistors are superior to serpentine resistors.

- Serpentine resistors for larger, minimal matched only.

## 16. Use poly resistors in preference to diffused ones.

- Poly can be made much narrower which does not cause significant increase in mismatch
- Tank not requires, immunes to tank modulation.

17. Place deposited resistors over field oxide.

- Increased variation when crossing oxide steps or surface discontinuities

18. Choose p-type in preference to n-type poly resistors

- Empirical results, p-type matched better matching

19. Do not allow N+ buried layer to intersect matched diffused resistors

20. Avoid routing unconnected leads over matched resistors.

- Potential noise coupling
- Can run over minimal matched resistor with sheet resistor 500Ω/□, moderate matched resistor with sheet resistor 100Ω/□

## 22. If leads cross resistors, they should cross all resistor segments in the same manner.

- mechanical stress may alter the value of resistor
- cross the resistor array orthogonally,
- intersect each segment at the same point
- with the same area of intersection
- critical matched resistors remain uncovered.

## 23. Avoid excessive power dissipation in matched resistors.

- thermal gradients degrade matching
- avoid 1.5uW/um$^2$ in precise matched resistors
- resistors dissipating large power should be interdigitated
- high current in narrow resistors induces velocity saturation nonlinearity