Lab4
Scan Reorder in SOC Encounter

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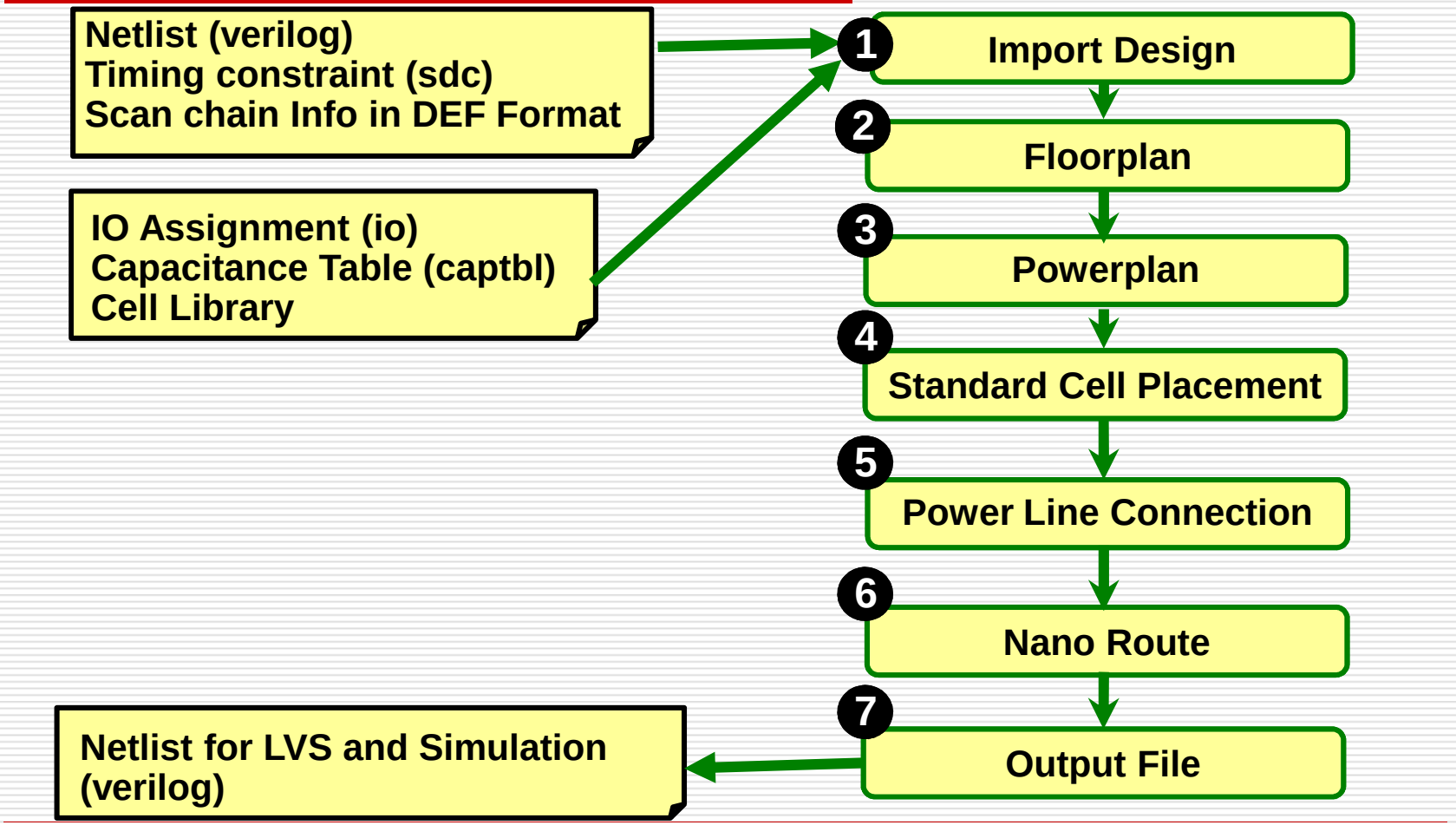
Outline

- Introduction
- SOC Encounter
  - Scan reorder after Nanoroute
  - Scan reorder during placement

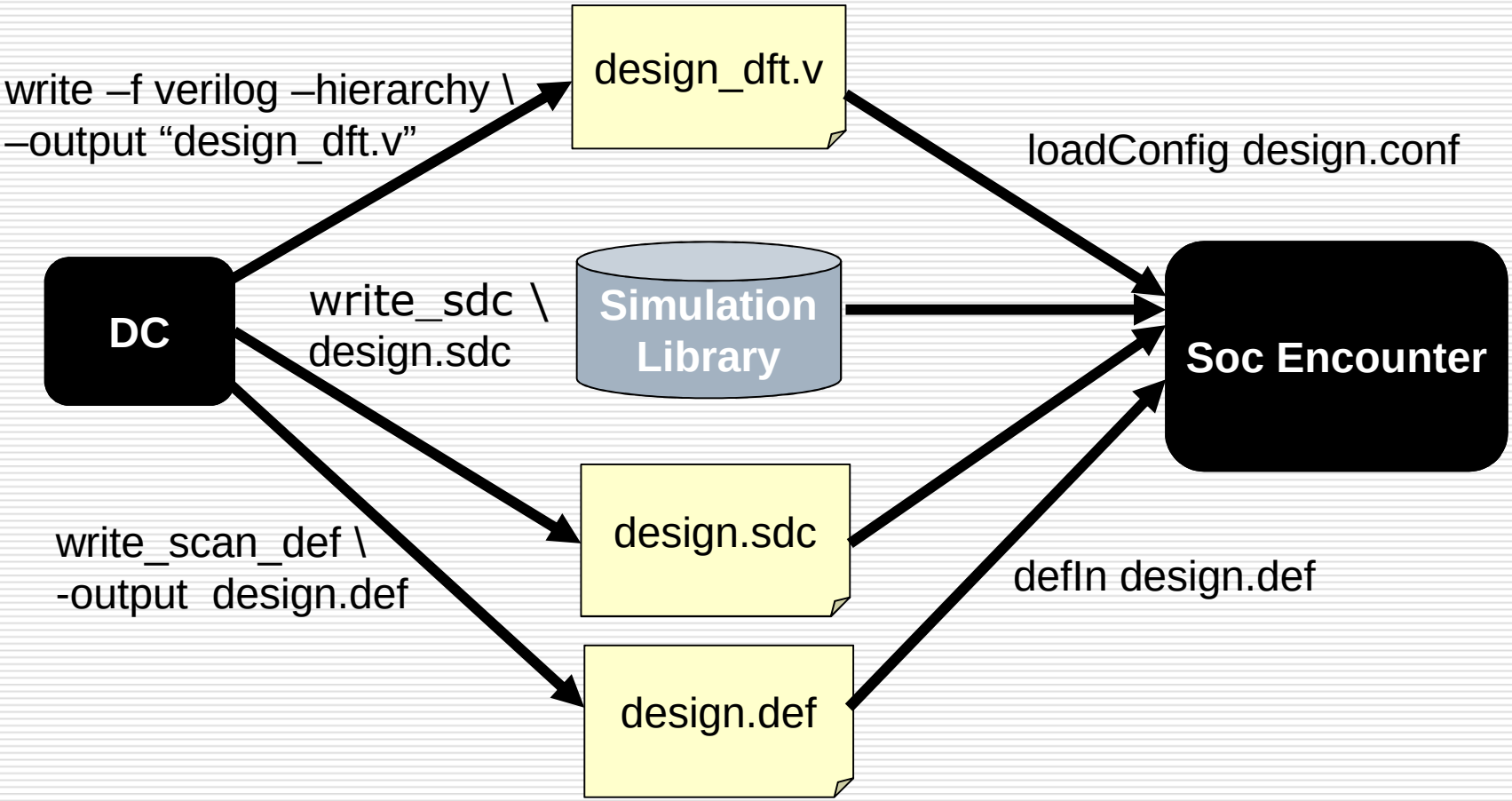
Introduction

- In this lab, we use SOC Encounter's build-in features to perform scan reorder either during placement or after placement.
- Cadence Soc Encounter is the most common Auto Placement & Route (APR) tool, which supports both interactive command input and GUI interface.

SoC Encounter Scan Design Flow



DFT compiler to SOC Encounter



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Invoke SOC Encounter

- $ source /CAD/scripts/default.csh
  - Just type above command for setting up all the tools.
- $ source /CAD/cadence/CIC/soc.cshrc
  - Just type above command for the first time invoke SOC encounter.
- $ cd lab4
- $ tar -zxvf lab4.tar.gz
- $ encounter

Import Design (1/2)

- View s38584_seq.conf to check the full included file list.
- Below is a snapshot:
  - set rda_Input(ui_netlist) "s38584_scan.v"
  - set rda_Input(ui_netlisttype) {Verilog}
  - set rda_Input(ui_topcell) {s38584_seq}
  - set rda_Input(ui_timelib,max) "lib/l90sprvt_bc.lib lib/uk90giosp25gpir_bc.lib"
  - set rda_Input(ui_timelib,min) "lib/l90sprvt_wc.lib lib/uk90giosp25gpir_wc.lib"

Import Design (2/2)

- Import the design configuration
  - encounter> loadConfig s38584_seq.conf
- Read Scan chain information
  - encounter > defIn s38584_scan.def
- Check Design
  - checks for missing or inconsistent library and design data at any stage of the design
  - encounter > checkDesign -all
- Check Unique
  - checks the uniqueness of the netlist; if the netlist is unique, the result is 1
  - encounter > checkUnique -verbose

Floor Plan

- Specify core width, height and core margin
  - encounter > floorPlan -site core
    -s 315.0 315.0 100 100 100 100
    - -s coreW coreH coreToLeft coreToBottom coreToRight coreToTop
- Connect Global Nets
  - encounter > globalNetConnect VDD -type tiehi -pin VDD
  - encounter > globalNetConnect GND -type tielo -pin GND

Power Plan (1/2)

- Create core power ring
  - encounter > addRing -center 1 -around core -nets {GND VDD } -width_left 9 -width_right 9 -width_bottom 9 -width_top 9 -spacing_bottom 0.34 -spacing_top 0.34 -spacing_right 0.34 -spacing_left 0.34 -layer_bottom metal3 -layer_top metal3 -layer_right metal2 -layer_left metal2

Power Plan (2/2)

- Create power stripes
  - encounter > addStripe -block_ring_top_layer_limit metal3 -padcore_ring_bottom_layer_limit metal1 -set_to_set_distance 100 -xleft_offset 40 -xright_offset 40 -padcore_ring_top_layer_limit metal3 -spacing 0.34 -merge_stripes_value 0.28 -direction vertical -layer metal2 -block_ring_bottom_layer_limit metal1 -width 9 -nets {GND VDD}
  - encounter > addStripe -block_ring_top_layer_limit metal4 -padcore_ring_bottom_layer_limit metal2 -set_to_set_distance 100 -ybottom_offset 40 -padcore_ring_top_layer_limit metal4 -spacing 0.34 -merge_stripes_value 0.28 -direction horizontal -layer metal3 -block_ring_bottom_layer_limit metal2 -ytop_offset 40 -width 9 -nets {GND VDD}

Standard Cell Placement(1/4)

- Connect core power pin
  - "sroute" : Connects the pad pin to rings
  - encounter > sroute -connect {padPin}
- Specify Placement Blockage
  - Choose M2, M3. Then there will be no cell placed under strip
  - encounter > setPrerouteAsObs {2 3}

Standard Cell Placement(2/4)

- Use command "placeDesign" to do standard cell placement
  - By default, "placeDesign" performs timing-driven placement with scan reordering.
  - Turning scan reorder off by
    - setPlaceMode -reorderScan false
  - Ignore scan connection by
    - setPlaceMode -ignoreScan true
  - Turning Pre-placement optimization off with -noPrePlaceOpt
  - encounter > placeDesign -noPrePlaceOpt

Standard Cell Placement(3/4)

- Connect standard cell power line from power rings or power stripes
  - encounter > sroute -connect { corePin }
- View scan chain
  - This command display each scan chain in GUI interface
  - encounter > displayScanChain

Nano Route(1/3)

- Runs routing via or wire optimization using the NanoRoute router.
  - Use command "getNanoRouteMode" to get the current setting
  - "-global | -detail | -globalDetail"
    - Specify routing types by parameter
    - Default: -globalDetail
  - Turing on Timing and SI driven feature by
    - encounter > setNanoRouteMode -routeWithTimingDriven true
    - encounter > setNanoRouteMode -routeWithSIDriven true

Nano Route(2/3)

- Default it runs placement check before route, turn it off by parameter "-noPlacementCheck"
- Taking care Process Antenna Issue
  - encounter > setNanoRouteMode -routeInsertAntennaDiode true
  - encounter > setNanoRouteMode -routeAntennaCellName ANTENNA
- encounter > routeDesign -globalDetail

Nano Route(3/3)

NanoRoute Summary

#Total wire length = 335292 um.
#Total half perimeter of net bounding box = 263026 um.
#Total wire length on LAYER metal1 = 8617 um.
#Total wire length on LAYER metal2 = 72822 um.
#Total wire length on LAYER metal3 = 95264 um.
#Total wire length on LAYER metal4 = 65180 um.
#Total wire length on LAYER metal5 = 50179 um.
#Total wire length on LAYER metal6 = 25147 um.
#Total wire length on LAYER metal7 = 9575 um.
#Total wire length on LAYER metal8 = 5345 um.
#Total wire length on LAYER metal9 = 3162 um.
#Total number of vias = 97514

Scan Reorder(1/3)

- Use command "scanReorder" to reorders the scan cells after running placement
  - "-allowSwapping"
    - Allows the software to swap scan elements between scan chains within the same partition.

      Default: No
  - "-lowEffort | -mediumEffort | -highEffort"
    - Specifies the effort level for reordering scan chains.

      Default: mediumEffort

Scan Reorder(2/3)

- "-preferH | -preferV"
  - Specifies the preferred direction for scan reordering connections.

    Default: No prefer.

- "-skipNone | -skipBuffer | -skipTwoPinCell"
  - Specifies how scan reordering handles buffers and inverters in the scan chain.

    Default: -skipNone

- encounter > scanReorder

Scan Reorder(3/3)

*** Summary: Scan Reorder

INFO: Finished reorder scan group 20.
*** Summary: Scan Reorder
INFO: Finished reorder 20 scan groups.
Initial total scan wire length: 36995.660
Final total scan wire length: 22411.860
Improvement: 14583.800 percent 39.42

Re-do Nano Route

- For connecting the Reordered scan cell.
- encounter > routeDesign -globalDetail

Verify Design(1/4)

- Use command "verifyConnectivity" to detects conditions such as opens, unconnected wires , unconnected pins, loops, etc. And generates violation markers in the design window.
  - encounter > verifyConnectivity -type all -error 100 -warning 50

Verify Design(2/4)

- Use command "verifyGeometry" to checks width, spacing, and internal geometry of objects and the wiring between them.
  - encounter > verifyGeometry -error 100 -warning 50

Verify Design(3/4)

- Use command "timeDesign" to runs Trial Route, extraction, and timing analysis, and generates detailed timing reports. The generated timing reports are saved in timingReports directory
  - encounter > timeDesign -postRoute -hold

Verify Design(4/4)

s38584_seq_postRoute_hold.summary

Top Cell: s38584_seq

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------


+--------------------+---------+---------+---------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | in2reg  | reg2out | in2out  | clkgate |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.036  |  0.170  |  0.036  |   N/A   |   N/A   |   N/A   |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |   N/A   |   N/A   |   N/A   |
|    Violating Paths:|    0    |    0    |    0    |   N/A   |   N/A   |   N/A   |
|          All Paths:|  5804   |  2880   |  4171   |   N/A   |   N/A   |   N/A   |
+--------------------+---------+---------+---------+---------+---------+---------+

Density: 83.781%
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```

Save Design

- Save current configuration
  - encounter > saveConfig s38584.conf
- Save current design
  - encounter > saveDesign s38584.enc

- Export Netlist for LVS and simulation
  - encounter > saveNetlist -includePhysicalInst -excludeLeafCell s38584_lvs.v
- Save sdf for post layout simulation
  - encounter > delayCal -sdf s38584.sdf

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Difference(1/3)

- Don't set command
  - encounter > scanReorder
  - encounter > routeDesign –globalDetail
    (Re-nano route for scan cell connection part)
- Turning scan reorder on and do the placement process
  - encounter > setPlaceMode -reorderScan true
  - encounter > placeDesign -noPrePlaceOpt

Difference(2/3)

*** Scan Sanity Check Summary:

INFO: Finished reorder scan group 20.
*** Summary: Scan Reorder
INFO: Finished reorder 20 scan groups.
Initial total scan wire length: 36995.660
Final total scan wire length: 22411.860
Improvement: 14583.800 percent 39.42

Difference(3/3)

NanoRoute Summary

#Total wire length = 336217 um.
#Total half perimeter of net bounding box = 263026 um.
#Total wire length on LAYER metal1 = 8459 um.
#Total wire length on LAYER metal2 = 73572 um.
#Total wire length on LAYER metal3 = 97306 um.
#Total wire length on LAYER metal4 = 64816 um.
#Total wire length on LAYER metal5 = 49125 um.
#Total wire length on LAYER metal6 = 25461 um.
#Total wire length on LAYER metal7 = 10090 um.
#Total wire length on LAYER metal8 = 5340 um.
#Total wire length on LAYER metal9 = 2047 um.
#Total number of vias = 95834

Reference

- [1] Cadence, “Encounter Menu Reference v8.1”, Nov. 2008
- [2] Cadence, “Encounter Text Command Reference v8.1”, Nov. 2008
- [3] Cadence , “Encounter User Guide v8.1”, Nov. 2008
- [4] IC Lab Course Slide, Chih-Lung Chen