Import design

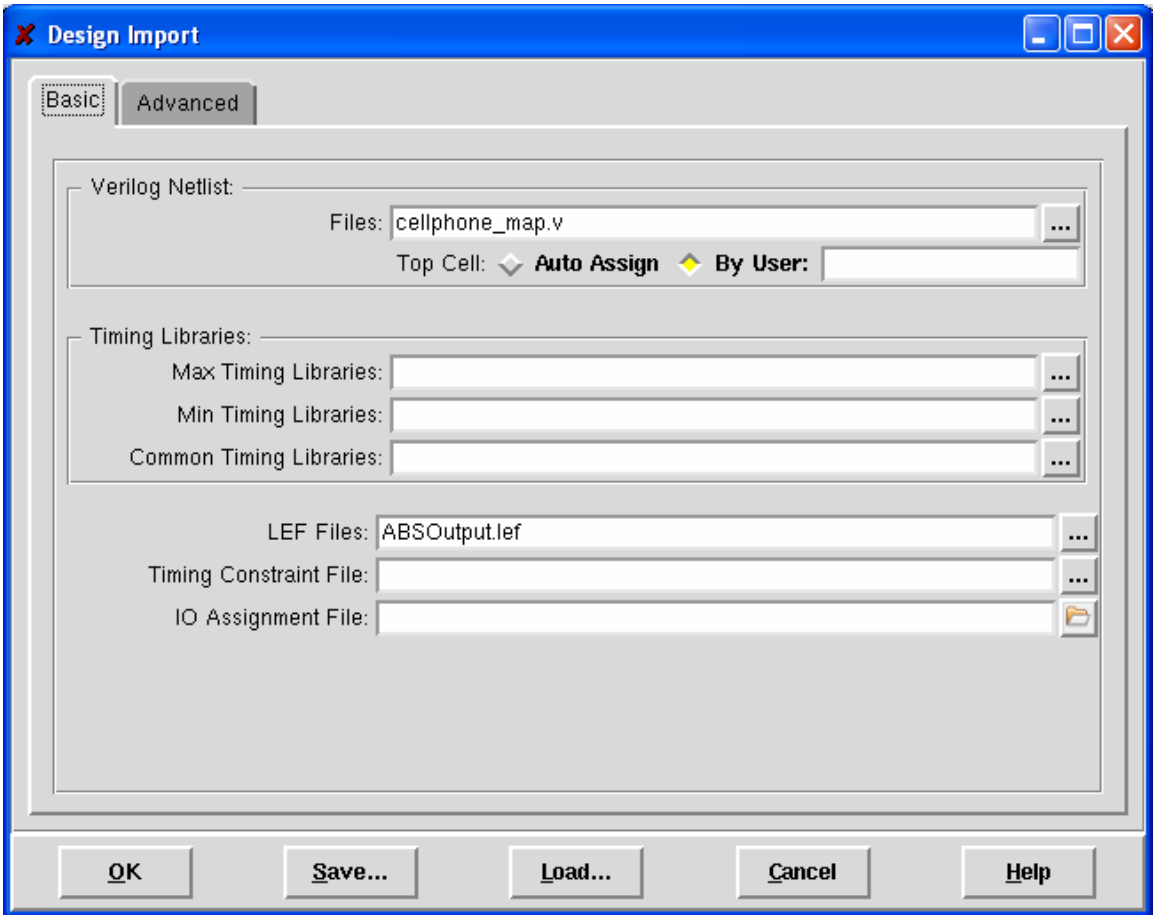
1) Put the ‘yourfile_map.v’ into your cadence directory.

2) Log into the joule server, and cd into the cadence directory.

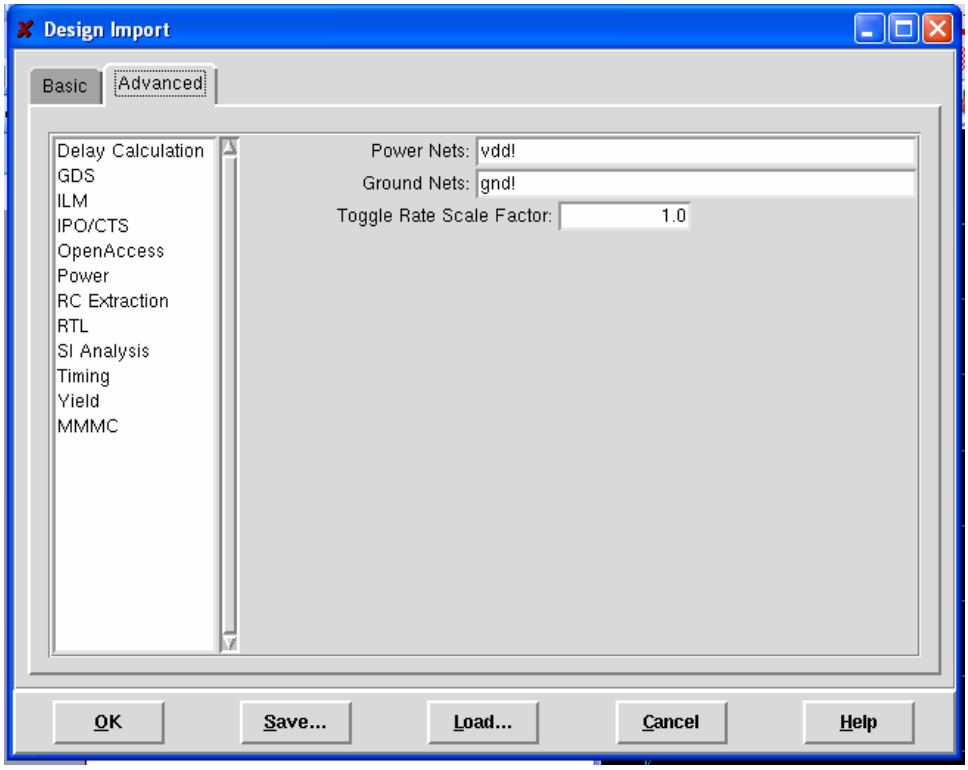
3) Go through Silicon Ensemble tutorial 1 (The Design Preparation)

4) After you successfully create the ABSOutput.lef, you now can start Encounter by typing ***encounter*** in the terminal window

5) Click on ***Design->Import Design***. Add ‘yourfile_map.v’ in Verilog Netlist. Select ***Auto Assign***. In the LEF files, add ‘ABSOutput.lef’



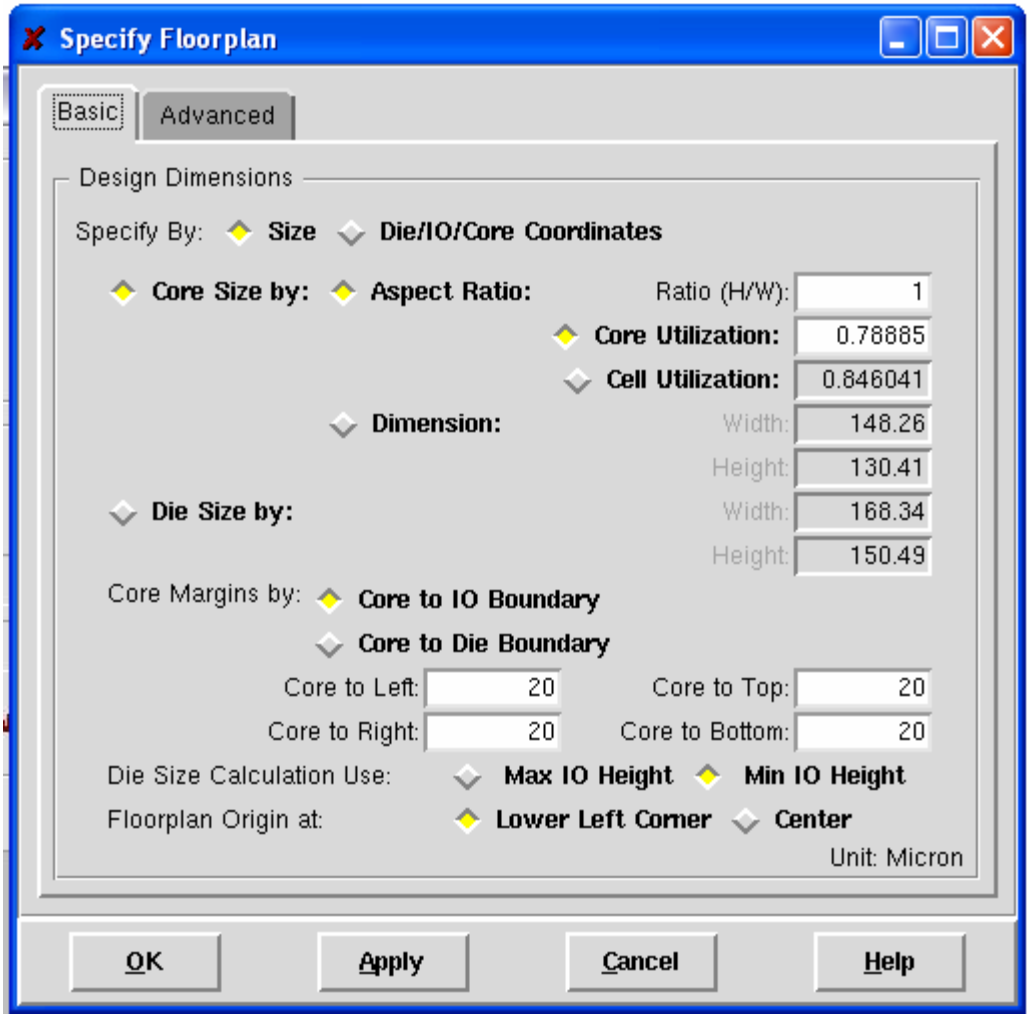
Click on the ‘Advanced’ Tab and fill **vdd!** and **gnd!** into power and gnd nets

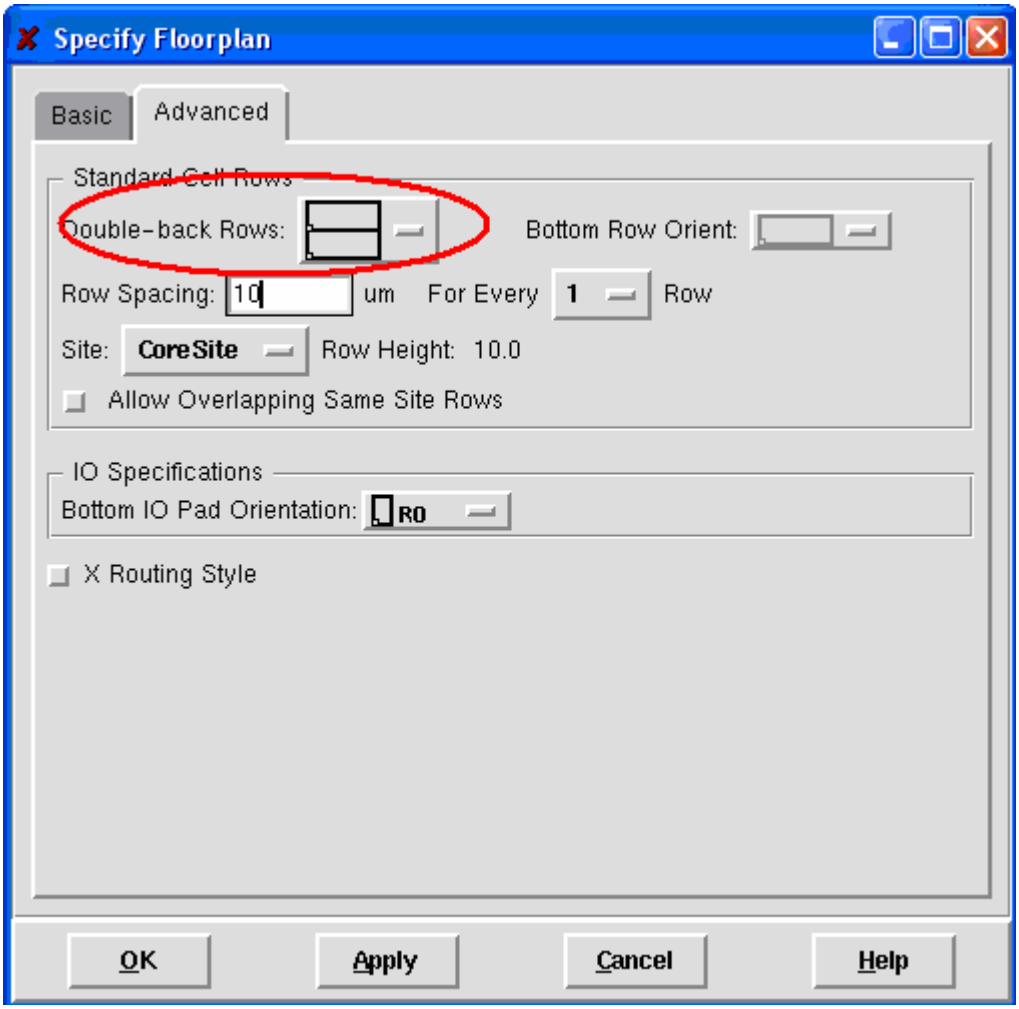


Click OK when you are done

Floorplanning

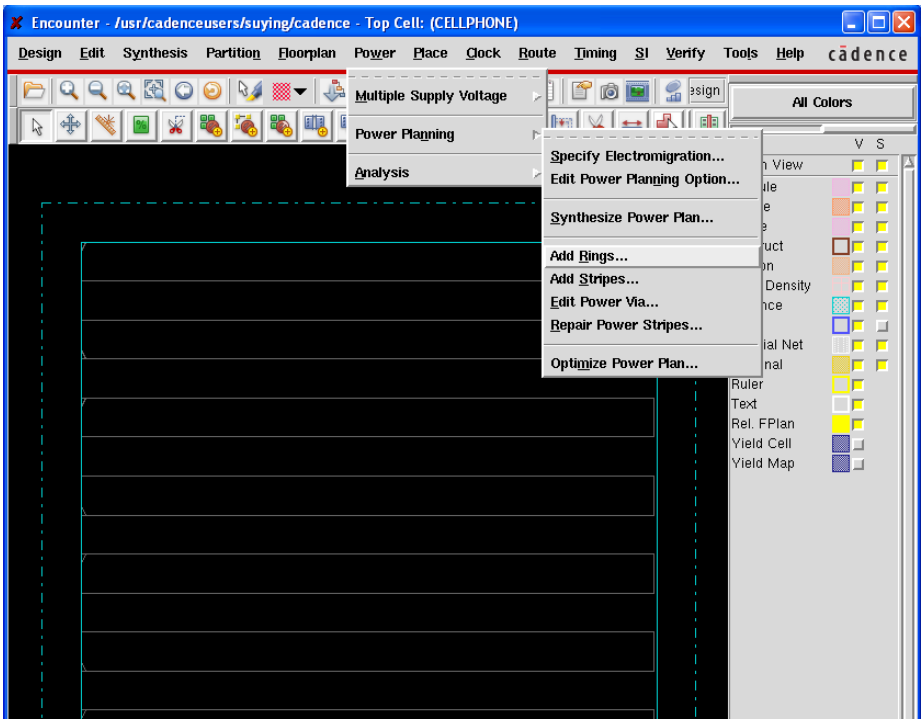
1) Select ***Floorplan->Specify Floorplan*** to open the *floorplanning* window. Make sure *Core Size by* is set to *Aspect Ratio* and *Aspect Ratio* is set to **1.0** (this controls the ratio between height and width of the design). Select *Core to IO Boundary* in *Core Margin*. Set the *Core to Left/Right/Top/Bottom* to **20** microns for all directions. If the design has room after routing, you may want to go back and re-run floorplanning with a smaller distance, as this will reduce the area of your design substantially. This will mean however that you will need to re-run all steps after floorplanning as well). Click the '***Advanced***' tab. Make sure you select the correct setting in the '***Double-back Rows***' as shown in the tutorial (very important!!). Set the *Row Spacing* setting **10um** for every **1 row** for now. It may be possible to later reduce this distance to shrink the design area, but it is necessary to view the routed design to determine this first. Click **OK** to finalize the floorplan.


Specify Floorplan
Basic
Advanced
Design Dimensions
Specify By: Size Die/IO/Core Coordinates
Core Size by: Aspect Ratio: Ratio (H/W): 1
Core Utilization: 0.78885
Cell Utilization: 0.846041
Dimension: Width: 148.26
Height: 130.41
Die Size by: Width: 168.34
Height: 150.49
Core Margins by: Core to IO Boundary
Core to Die Boundary
Core to Left: 20
Core to Top: 20
Core to Right: 20
Core to Bottom: 20
Die Size Calculation Use: Max IO Height Min IO Height
Floorplan Origin at: Lower Left Corner Center
Unit: Micron
OK
Apply
Cancel
Help

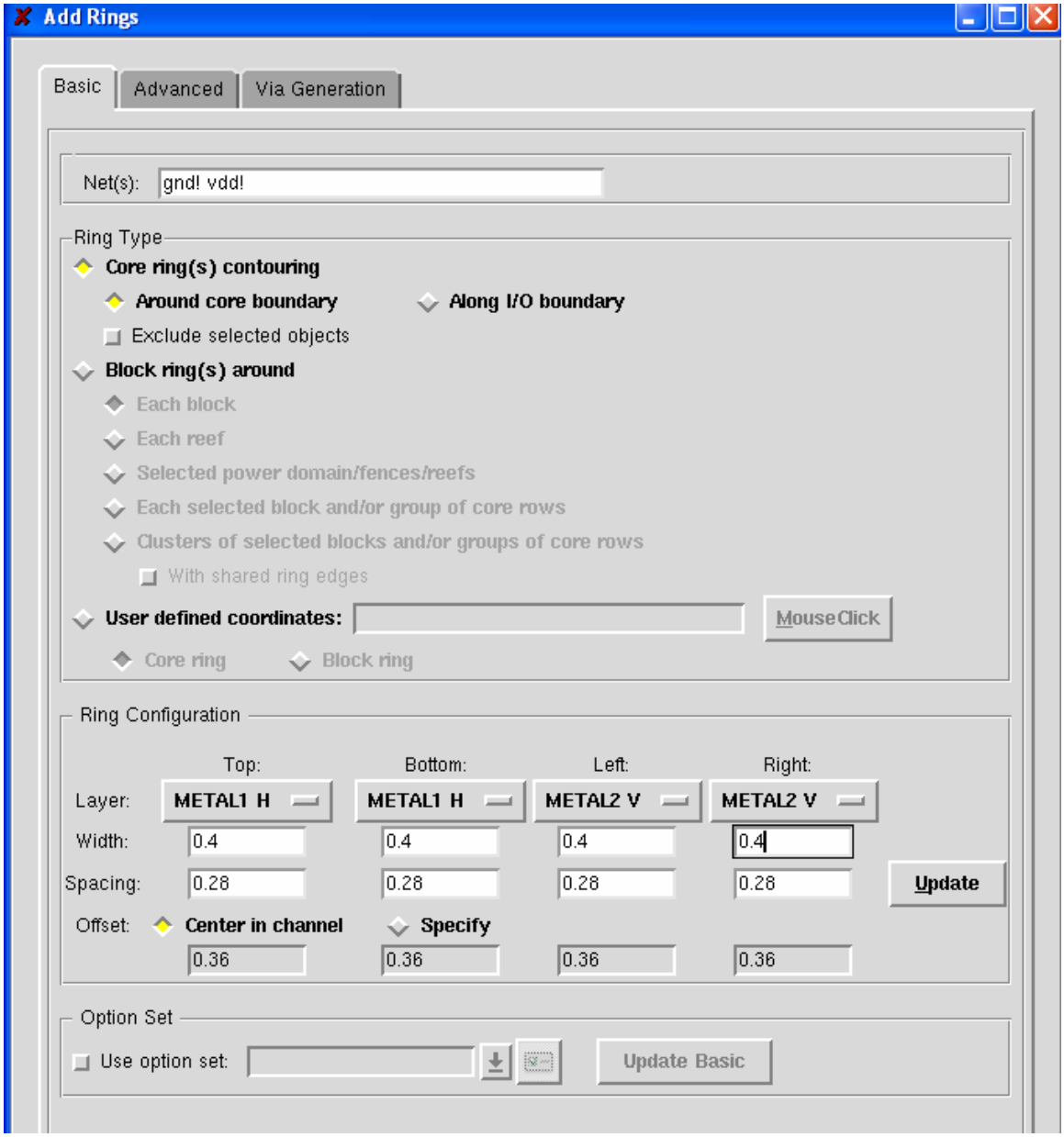


Power/Ground Ring

After floorplanning, do the power/ground ring: ***Power->Power Planning->Add Rings***

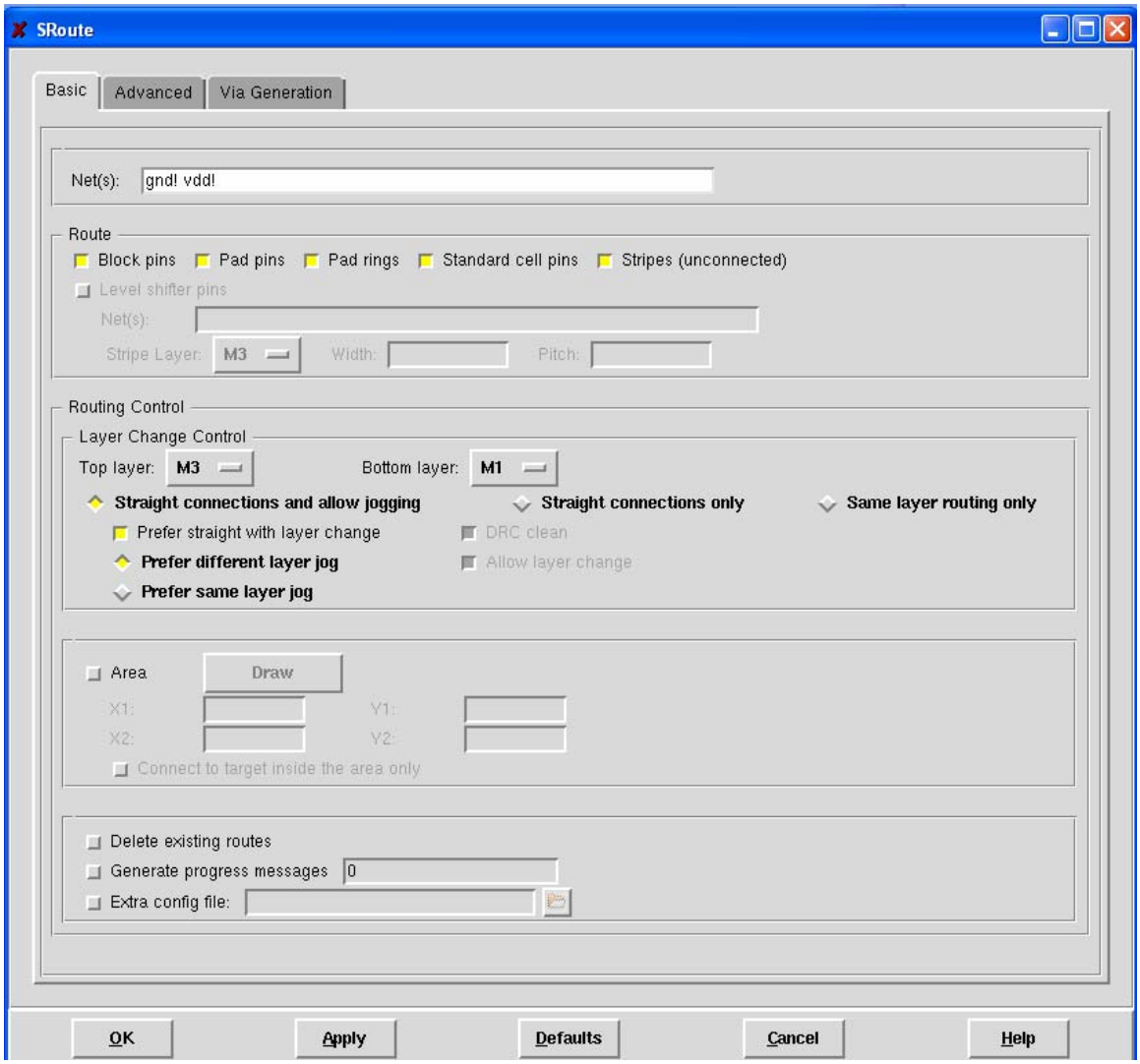


Set metal width to ***0.4um.*** Set ***Center in channel*** in the ***Offset***, then click ***OK***

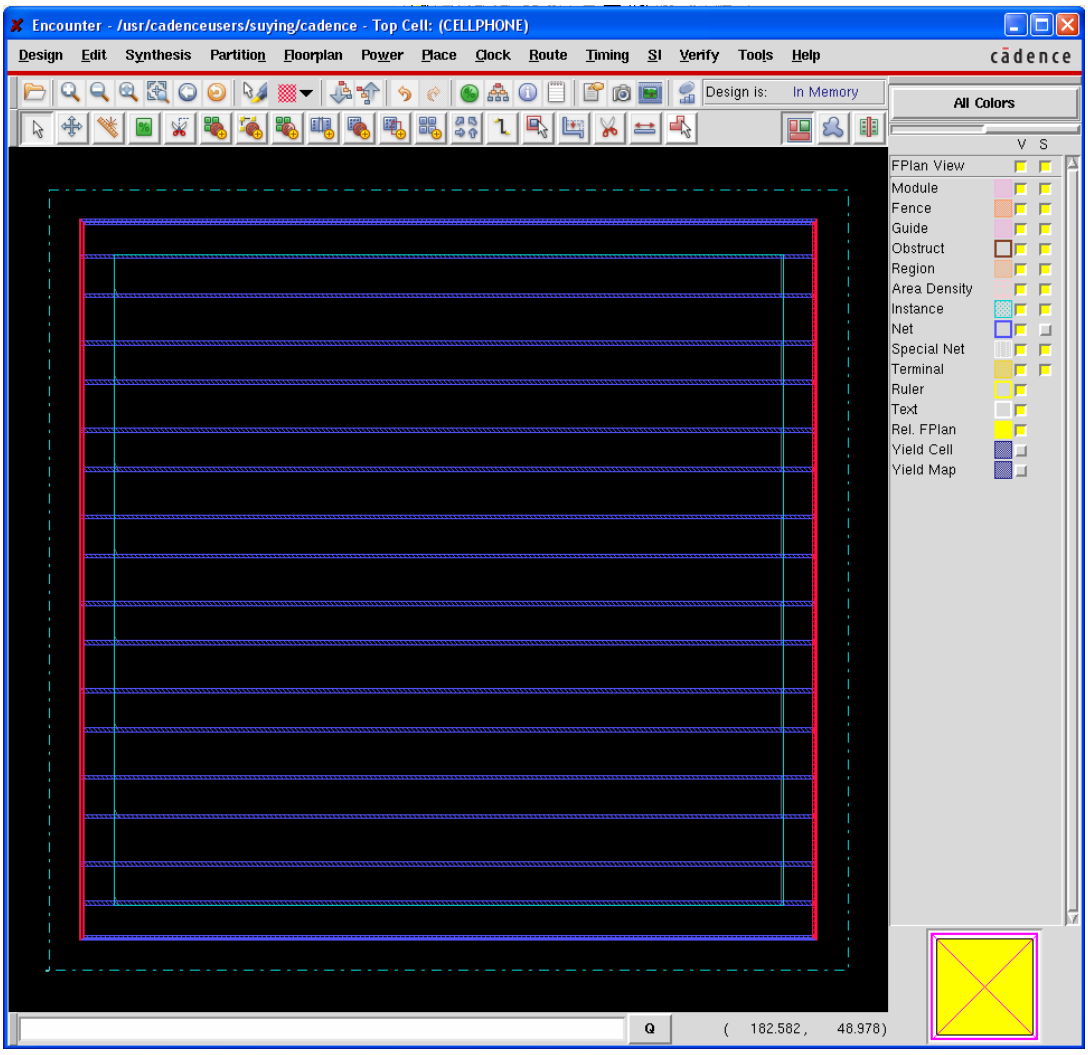


Route Power and ground

After added the power/gnd ring, the next step is routing the vdd/gnd net. Go to ***Route->Special Route***. The default setting is fine. Click OK on the SRoute form.

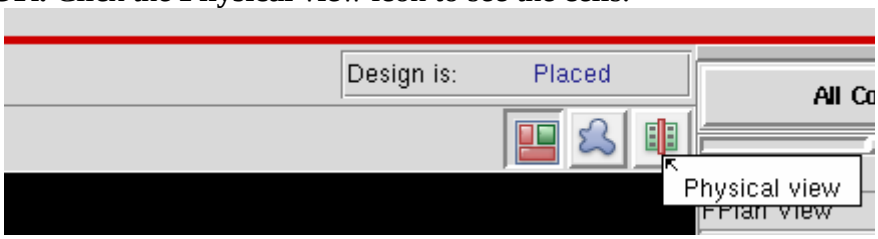


After this, you should have something looks similar to this picture.



Place Standard Cell

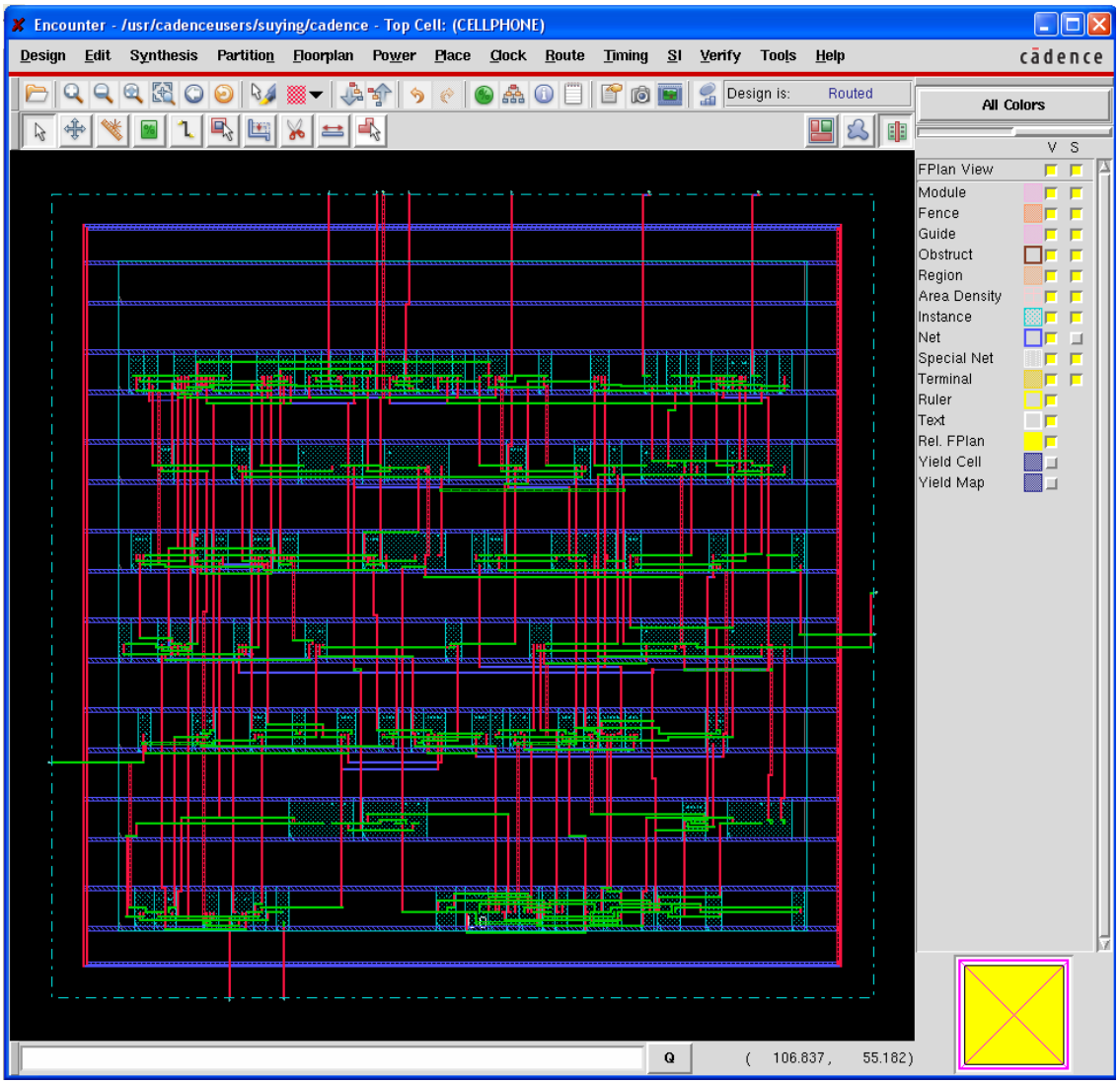
In the toolbar, select **Place->Standard Cells and Blocks**. The default setting should be ok. Click **OK.** Click the **Physical view** icon to see the cells.



Route

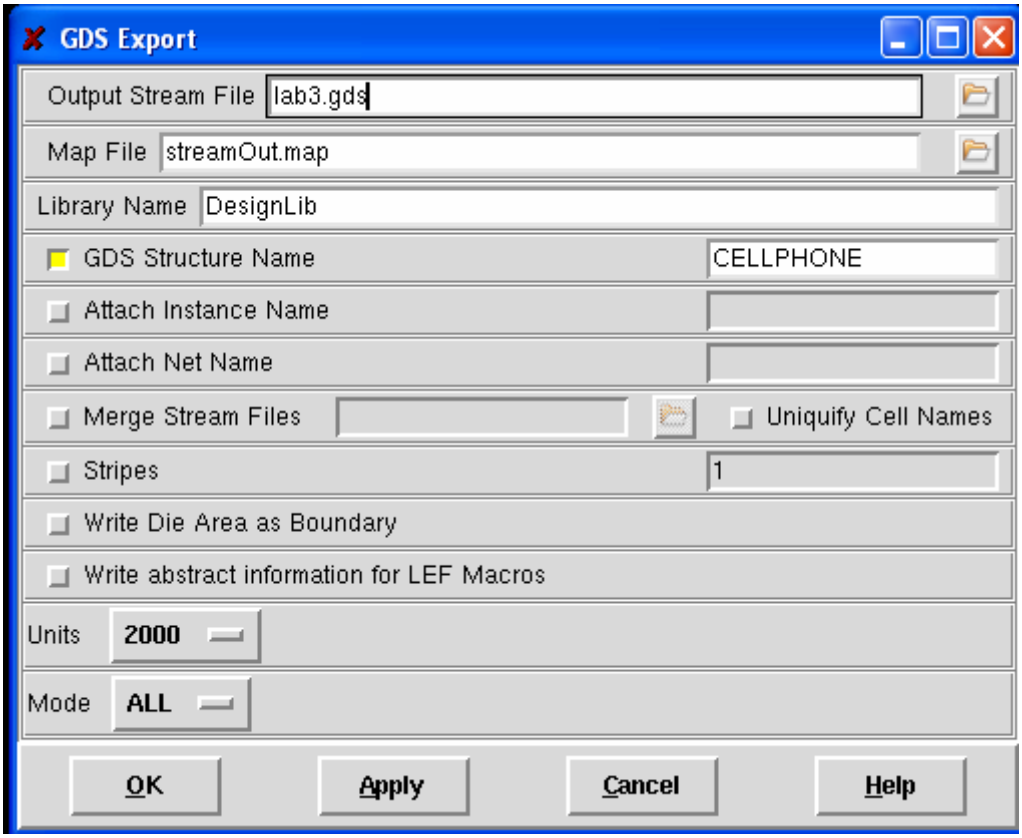
Rout the placed standard cell: ***Route->Nanoroute->Route***, the default setting should be ok. Click ok and it will start routing.

After routing is done, you should have something looks similar like this:



Save

After routing, you will have to save your design as a **gds** file. Go to ***Design->Save->GDS***
Output stream file: lab3.gds



Stream Design Back into Cadence

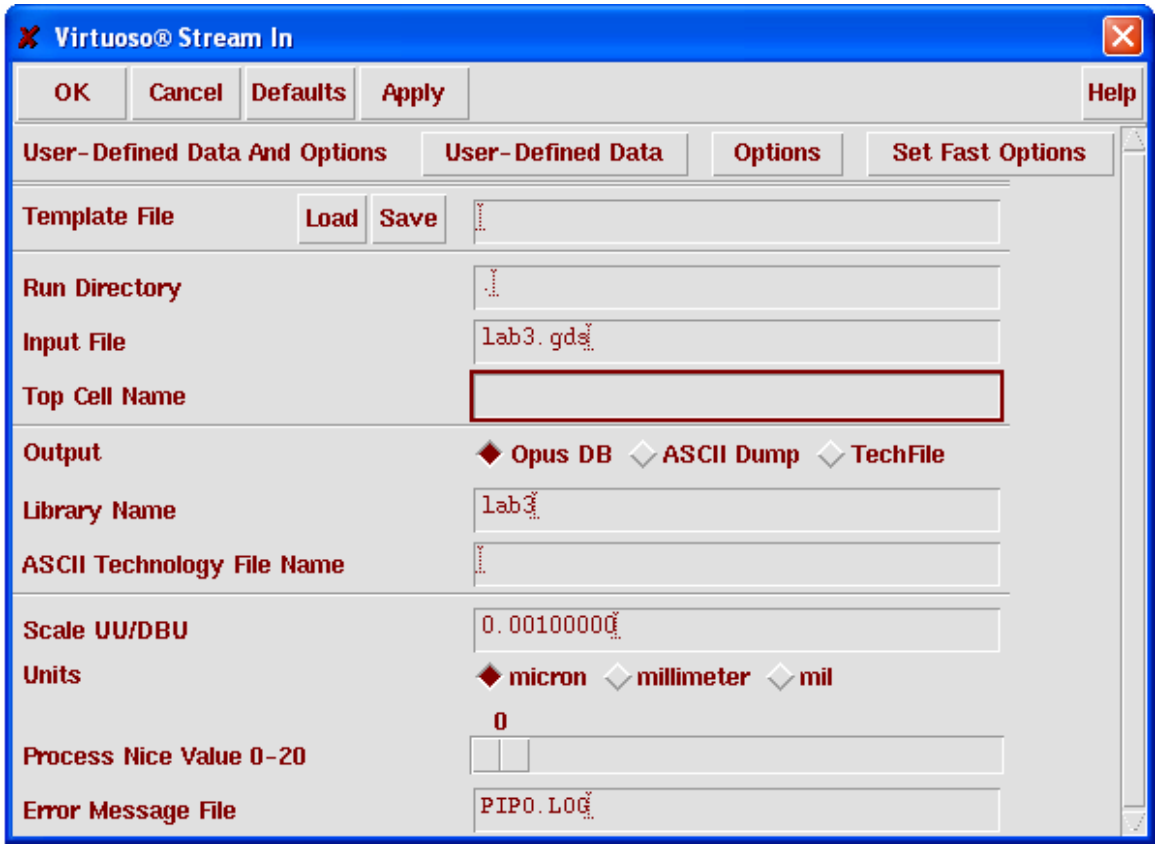
You can put Encounter work in the background now and start cadence. You don't want to quit Encounter since you will need it later.

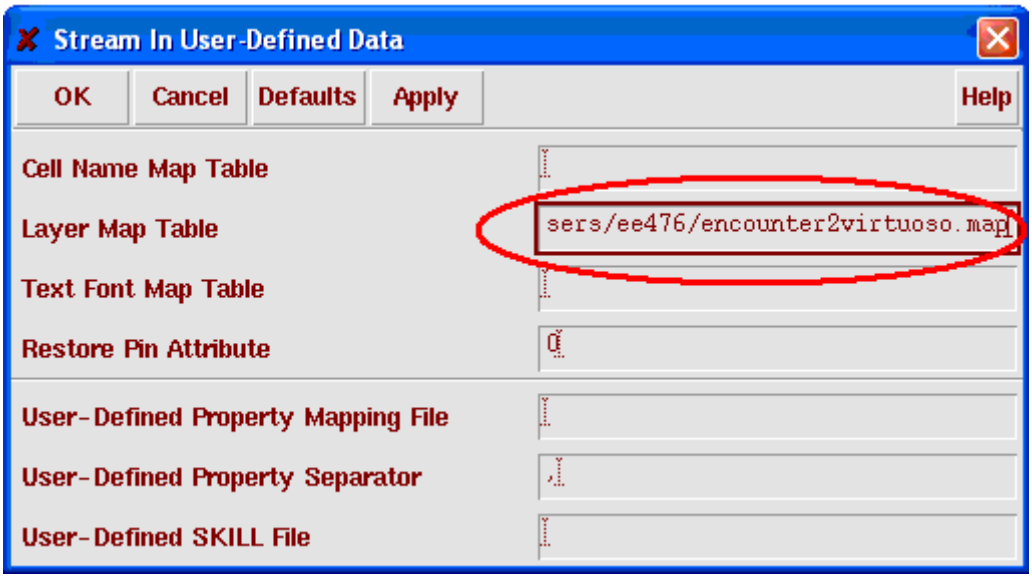
(In your terminal window, type '**Ctrl+z'** to suspend a Encounter. Use the '**icfb &**' command to start cadence. If you want to retrieve Encounter, type '**bg**' in the terminal window)

In the **icfb command window**, click on ***File->Import->Stream***. The gds stream in form will pop up.

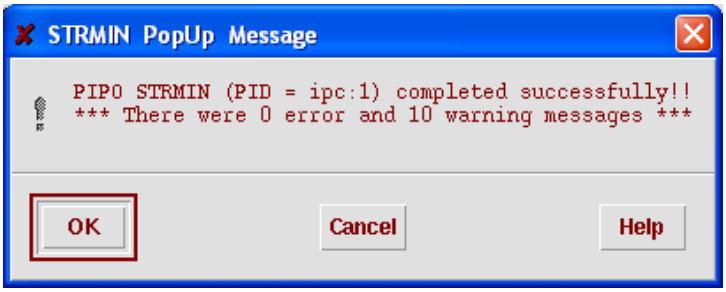
Input file is **lab3.gds**, library name is **lab3**. Click ***User-Defined Data***, in the layer map table, replace the old .map file with this:
/usr/local/cadenceusers/ee476/encounter2virtuoso.map

Click OK in the stream in user defined data form and the steam in form.

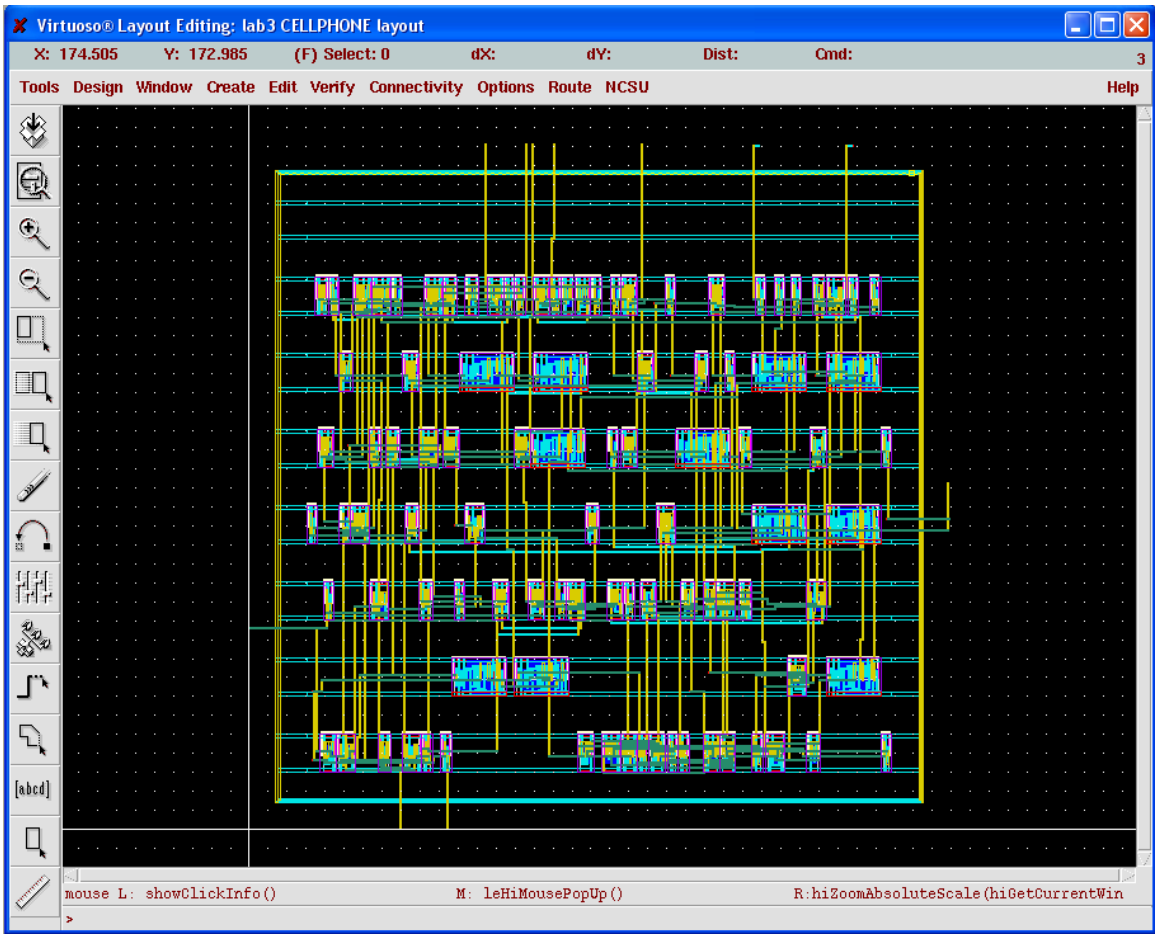




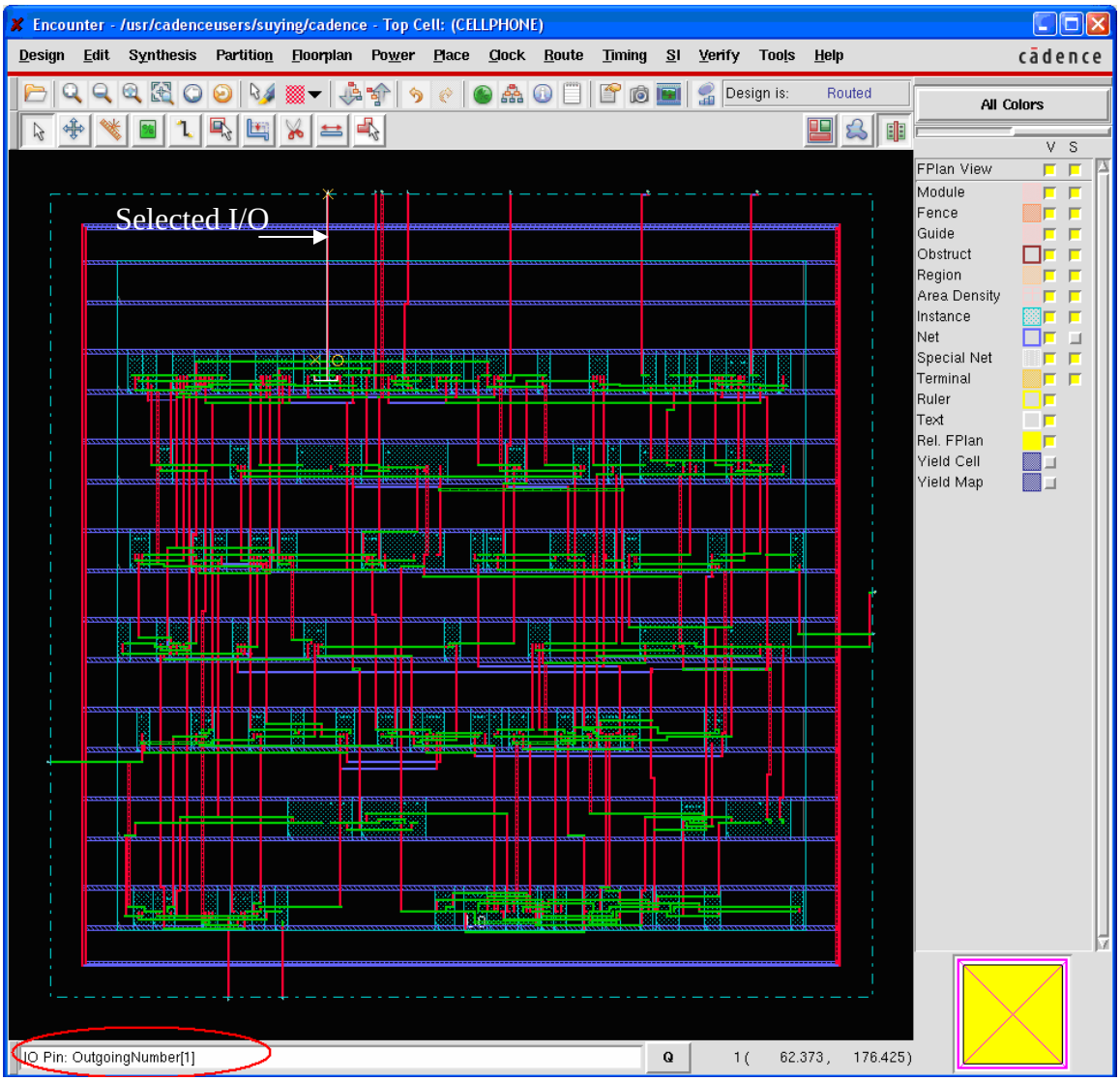
After you successfully stream in the gds file, you will see this pop up message:



Open your Cellphone Layout. Shift+f to view the transistor level design. Run DRC and clear the errors.



You also need to add I/O pins in this layout. You will need to go back to Encounter, and click on one I/O pin. The dialog window in Encounter tells you what connection is that. Go through the same step for all the I/O pins, and don't forget vdd and gnd.



After you clear all the DRC errors, create the extracted view, which is the same procedure in previous projects (remember to set the switch to '***PARASITIC_C***')

Open the extracted view and run LVS for the design.

By Ying Su