Tutorial for Cadence SOC Encounter Place & Route

For Encounter RTL-to-GDSII System 11.13

T. Manikas, Southern Methodist University, 6/7/13

Contents

1 Preliminary Setup 1
1.1 Helpful Hints 1
2 Starting Tool and Reading in the Design Files 2
2.1 Saving and Restoring Your Design 9
3 Floorplanning 11
3.1 Specify Floorplan 11
4 Power Planning 13
4.1 Connect Global Nets 13
4.2 Power Rings 14
4.3 Power Stripes 17
4.4 Connect Power to Standard Cell Rows 21
5 Placing the Standard Cells 22
6 Routing 24

1 Preliminary Setup

Create a separate directory for the above files in your account (e.g., Encounter). Create the subdirectories **synth** and **lib**

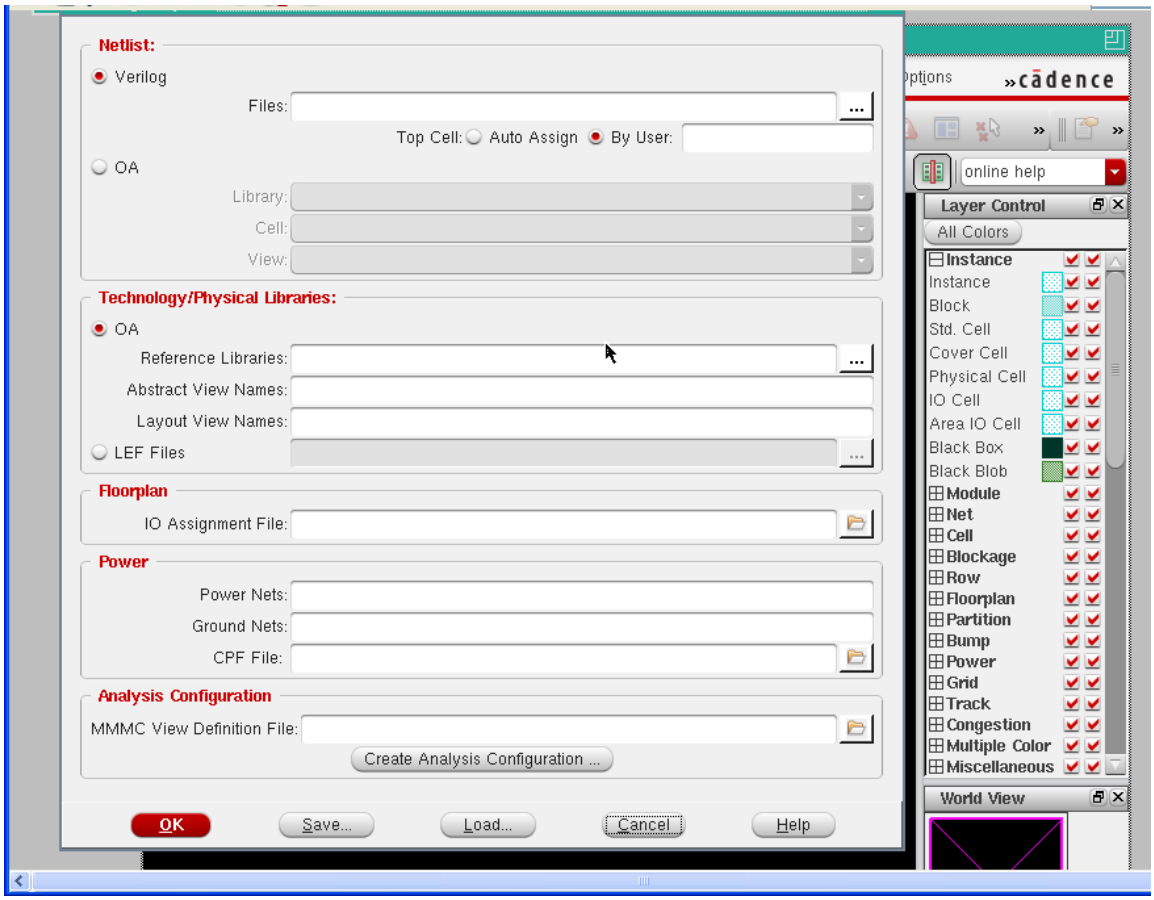
1. Move **full_adder_pads_synth.v** to the **synth** directory
2. Move **osu05_stdcells.lef** to the **lib** directory

1.1 Helpful Hints

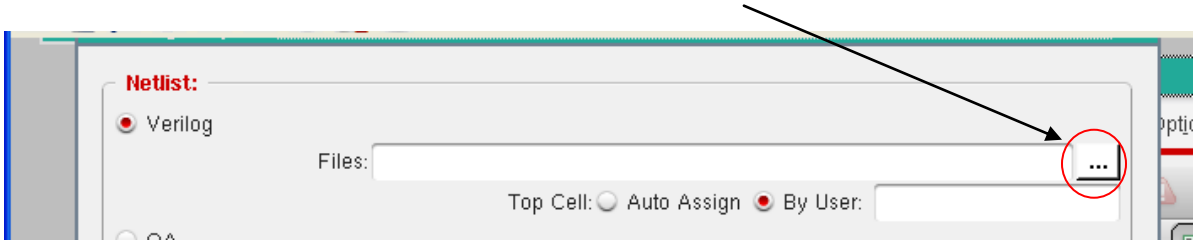
1. Some of the pop-up windows may be too big for your screen, making it hard to access the button on the bottom of the window. To move a window in X-windows, point your mouse anywhere in the window and press the **ALT** key and the **right** mouse button.

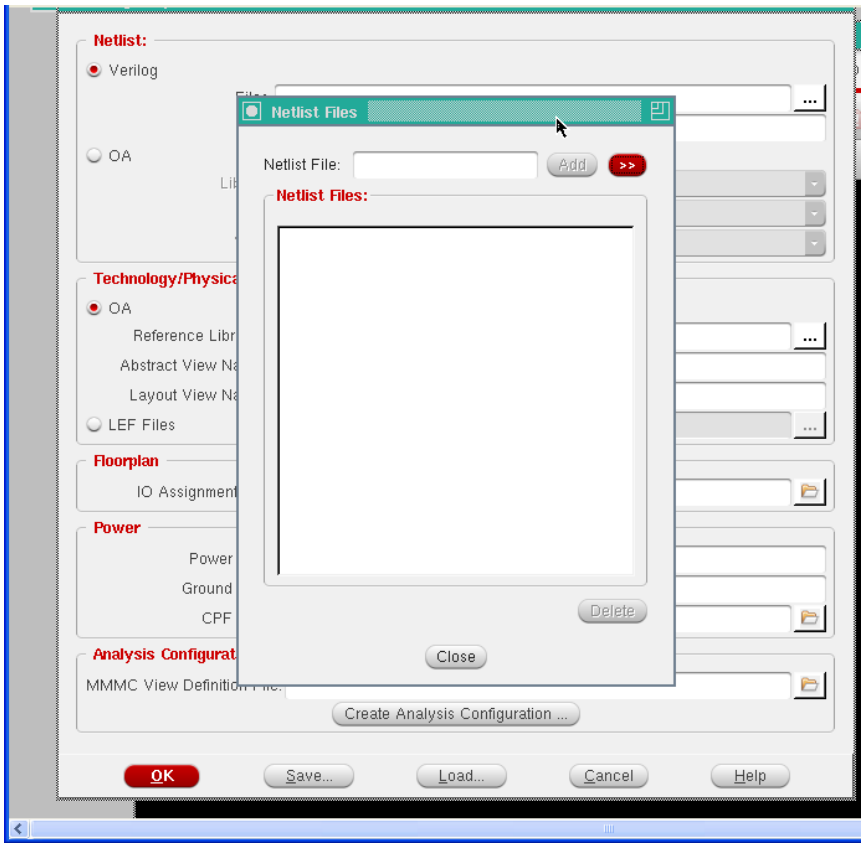
2 Starting Tool and Reading in the Design Files

1. Make sure that you are in your main separate directory (e.g., Encounter) as mentioned earlier
2. At the Unix prompt, type: **velocity**
3. When the Encounter tool window appears, go to the menu bar and select **File, Import Design** to get the **Design Import window**.

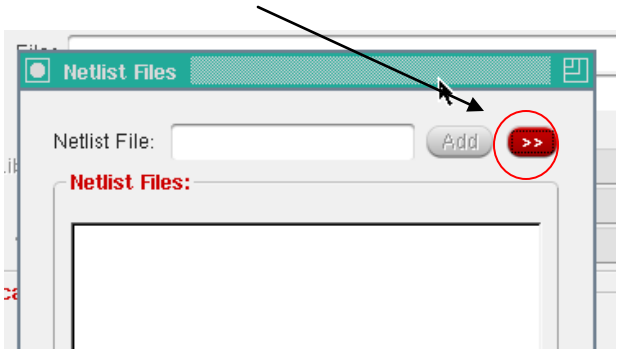


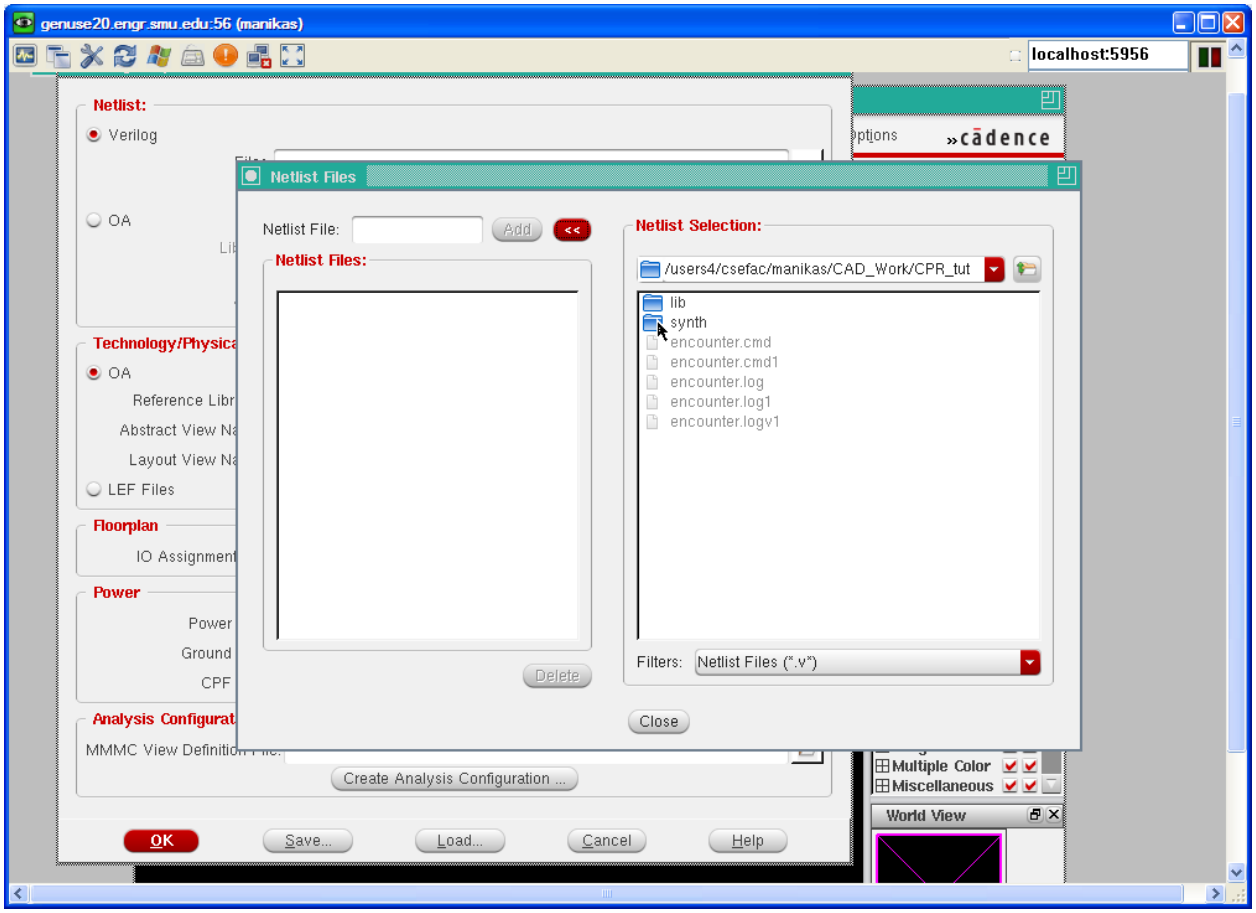
4. For the **Verilog Netlist**, click on the box with the dots **[…]** to open the **Netlist Files window**



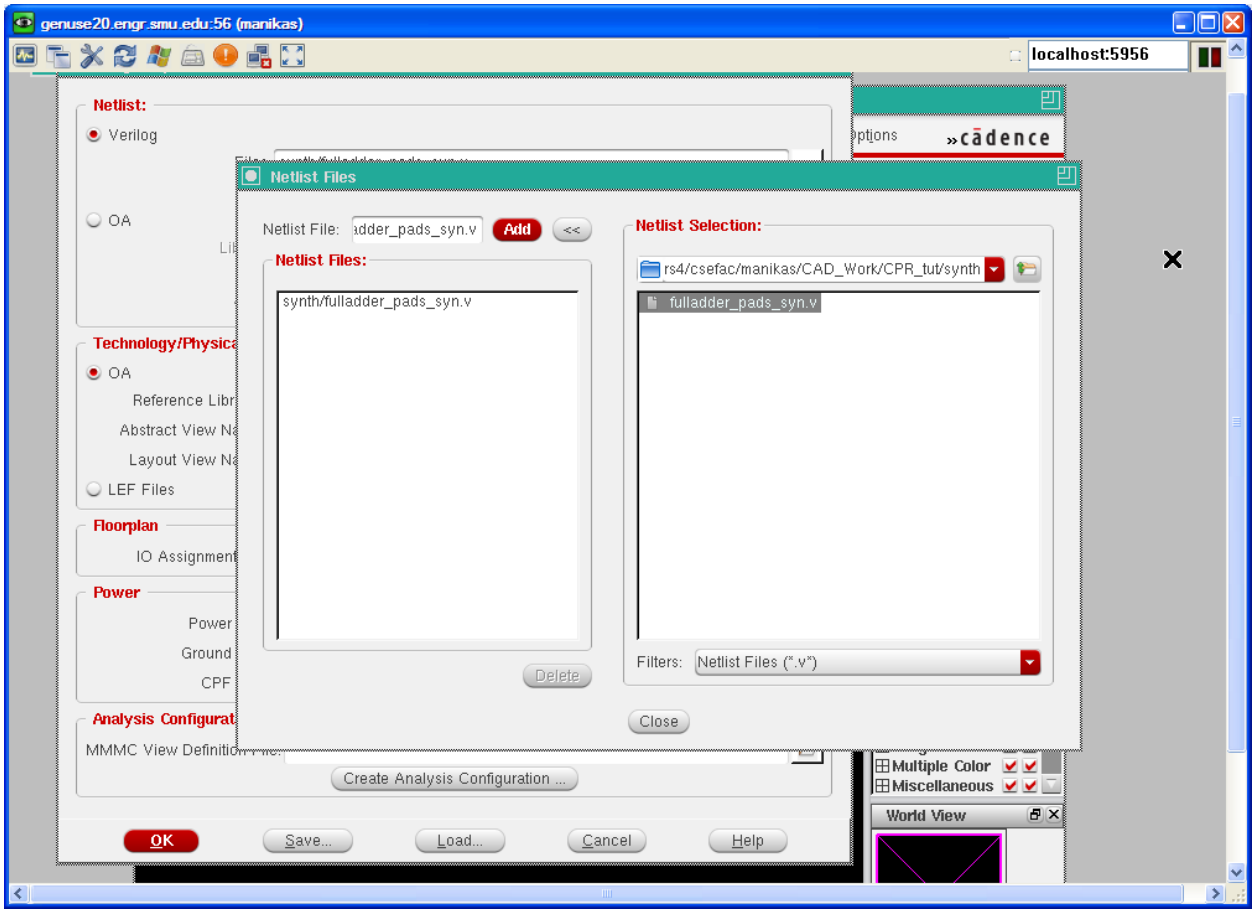


5. Click on the ">>" button to expand the window to show the directories:

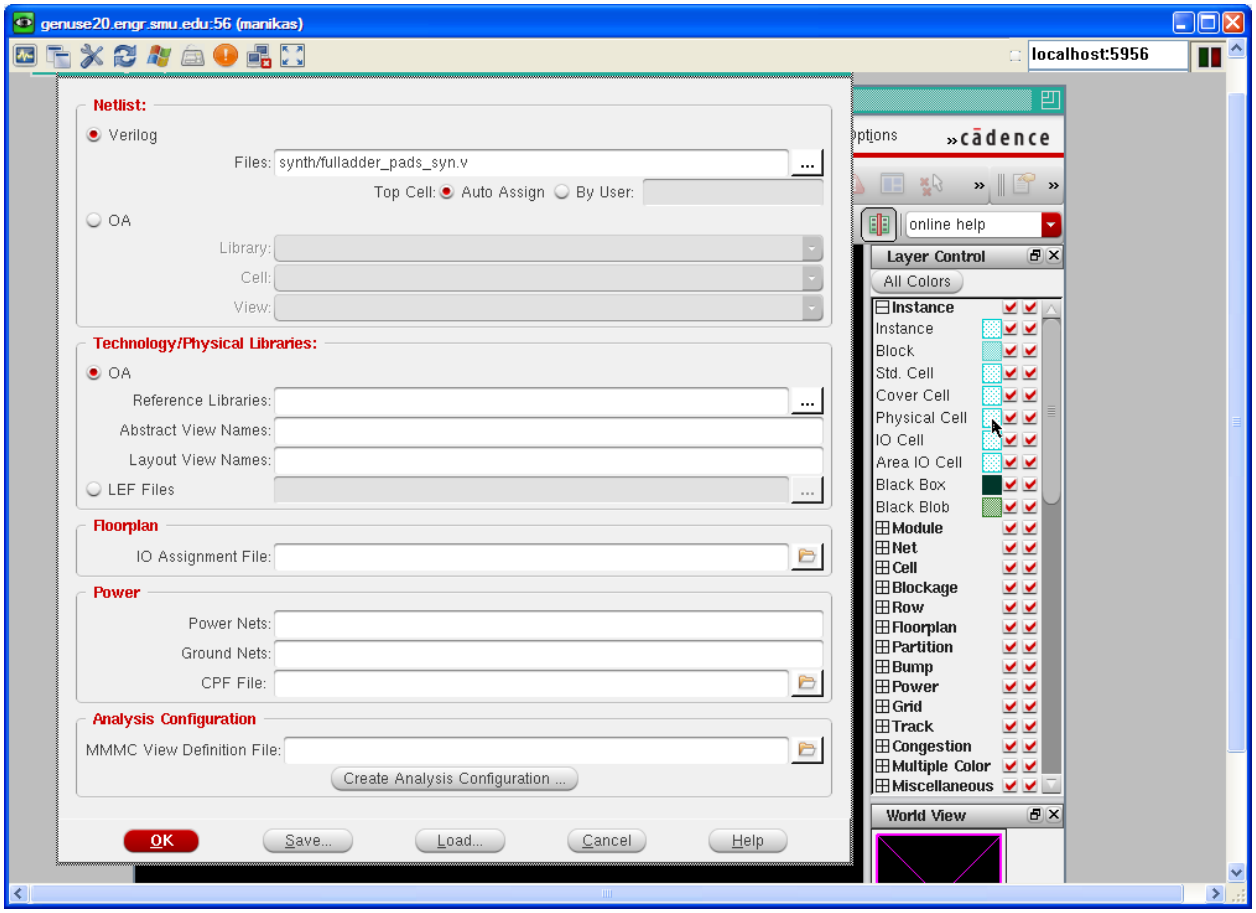




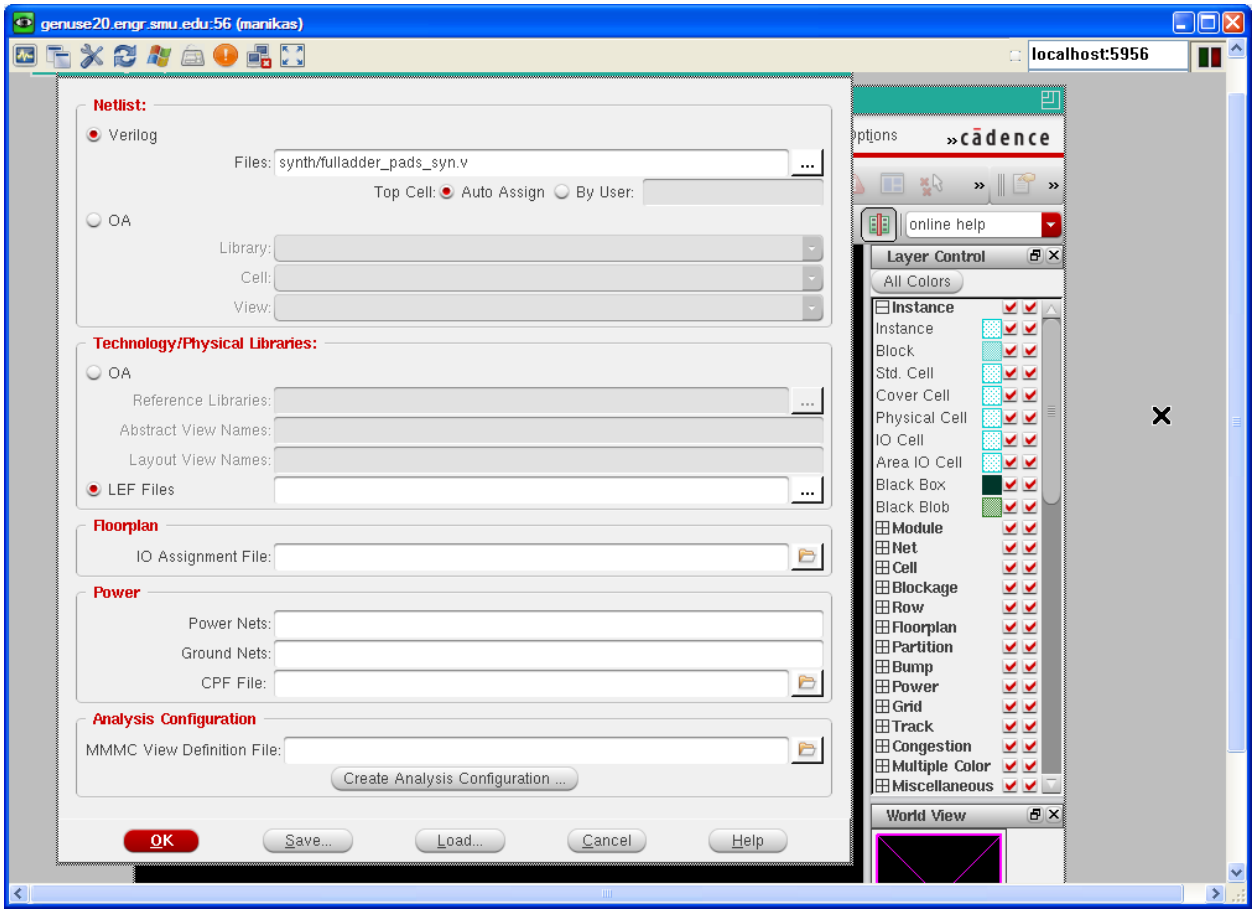
6. Double-click on the **Synth** folder, then select the file **full_adder_pads_synth.v** and click the **Add** button to add it to the Netlist Files list. Click **Close** to close the Netlist Files window.



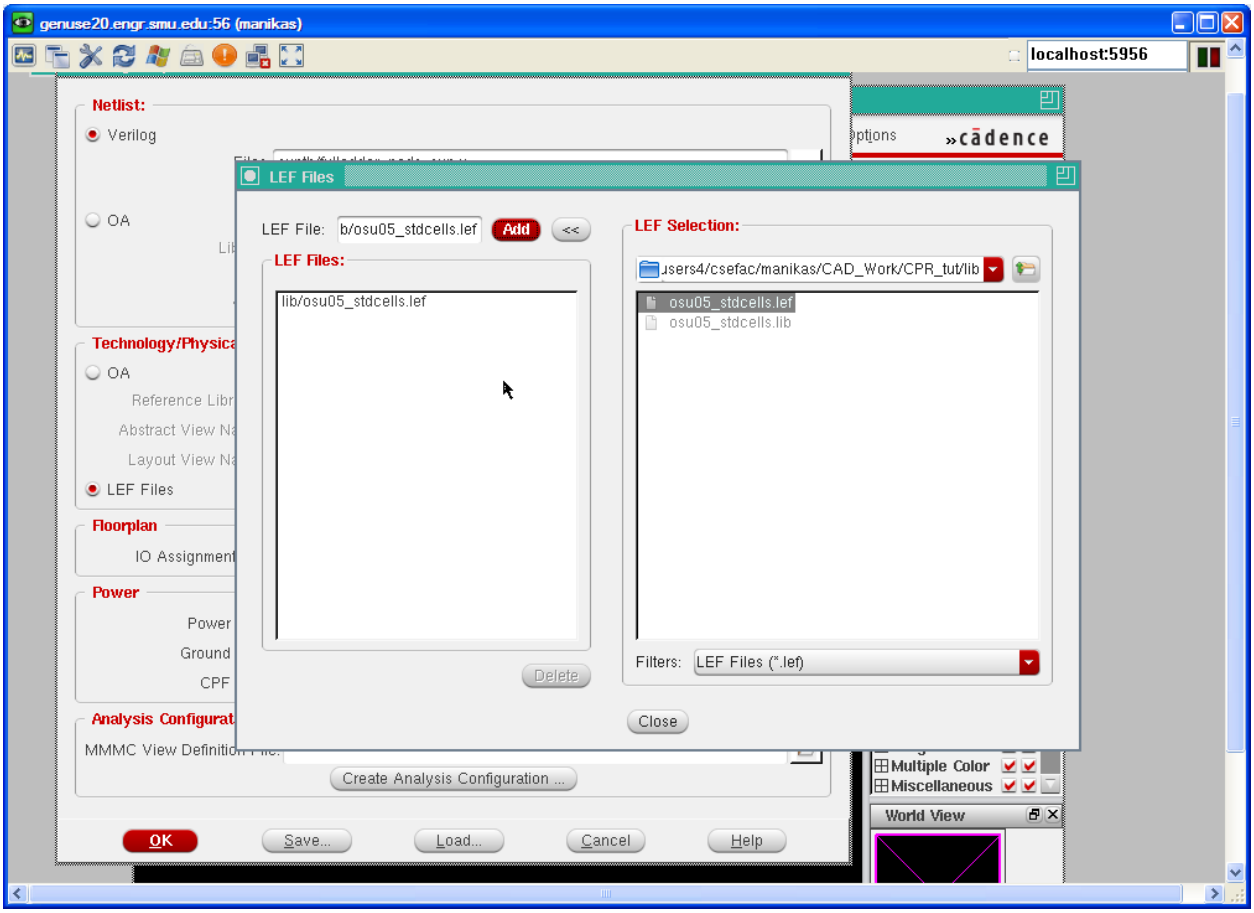
7. In the main window, for **Top Cell**, select "**Auto Assign**"



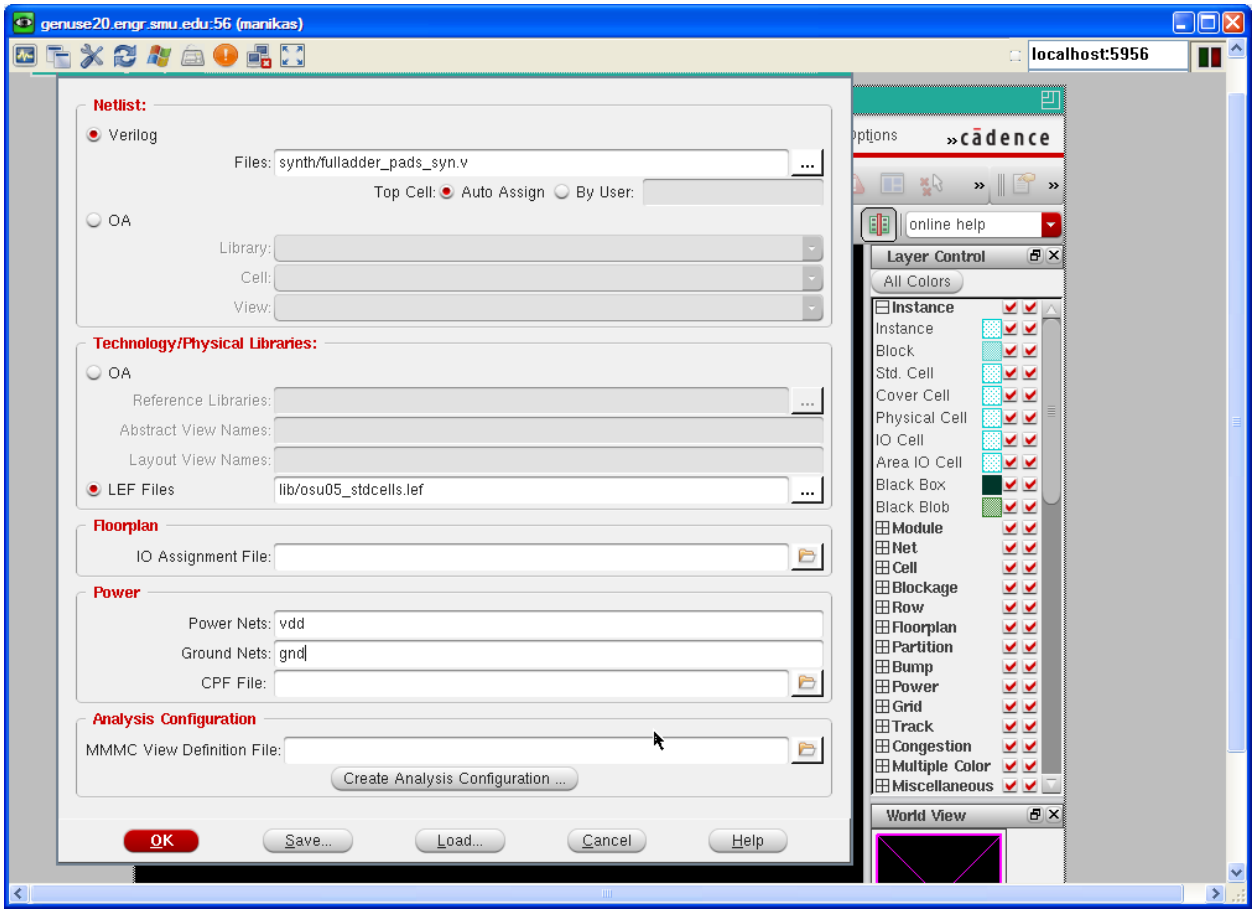
8. For **Technology/Physical Libraries**, select "**LEF Files**". Click on the […] button open the LEF Files window.



9. Using the same approach as for selecting the Verilog Netlist file, select the file **lib/osu05_stdcells.lef**

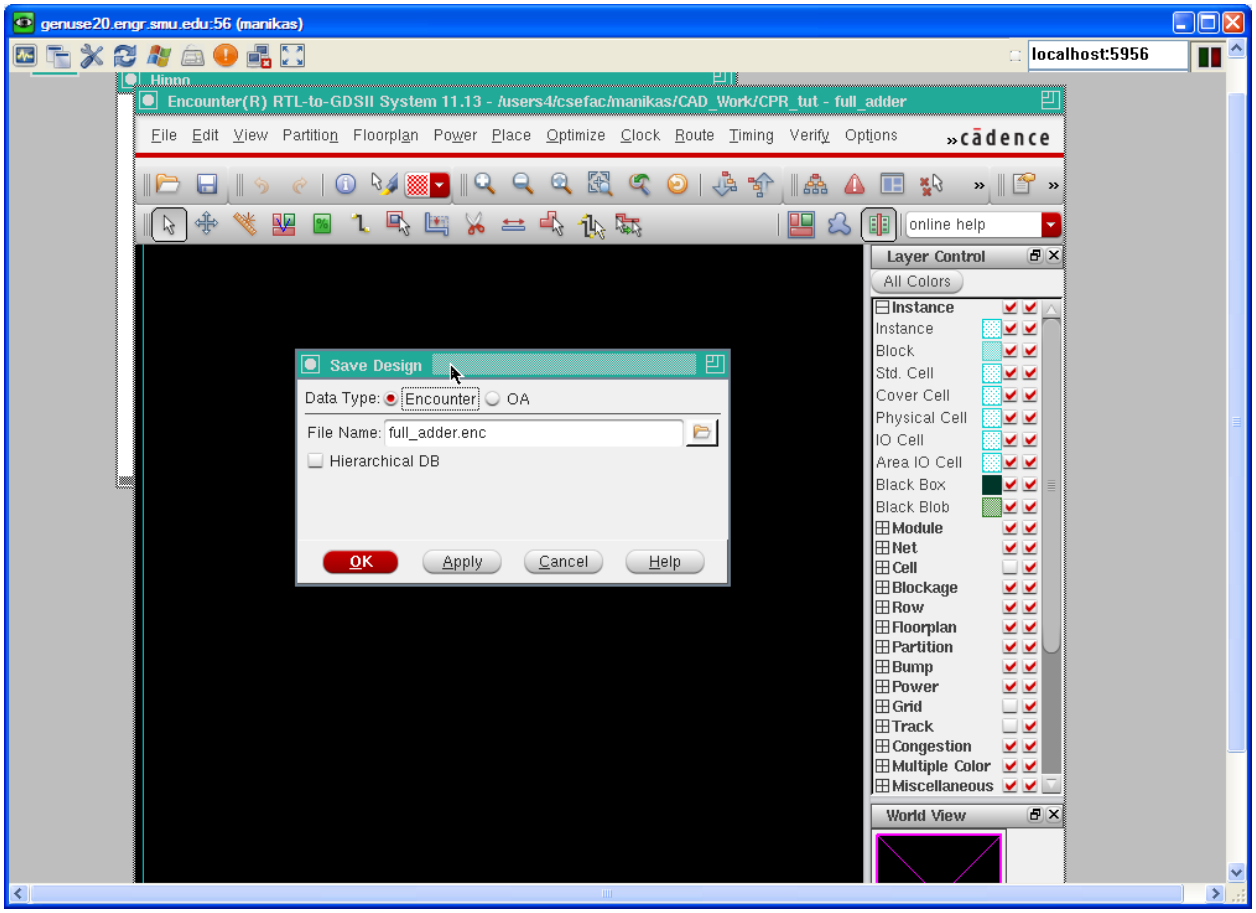


10. For **Power**, enter the following:
    a. Power Nets: **vdd**
    b. Ground Nets: **gnd**
11. Click on **OK**.

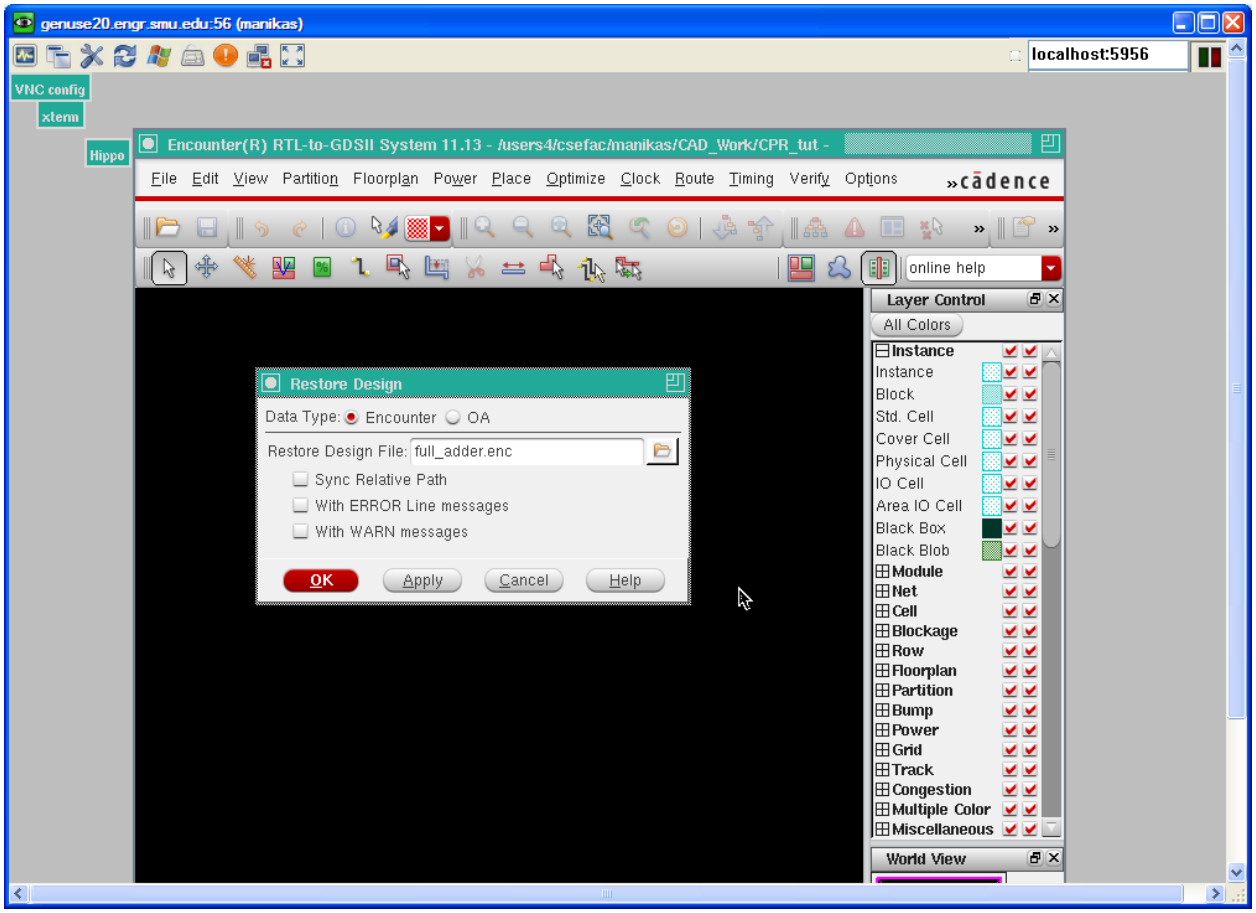


2.1 Saving and Restoring Your Design

NOTE: It is a good idea to save your design periodically. Select **File, Save Design**. In the Save Design Window, select **Data Type: Encounter**. The program will assign a default filename with extension *.enc. You may change the name, but do not change the extension.



To load a saved Encounter file, do **File, Restore Design**. In the Restore Design Window, select **Data Type: Encounter**. Select the file to be restored.

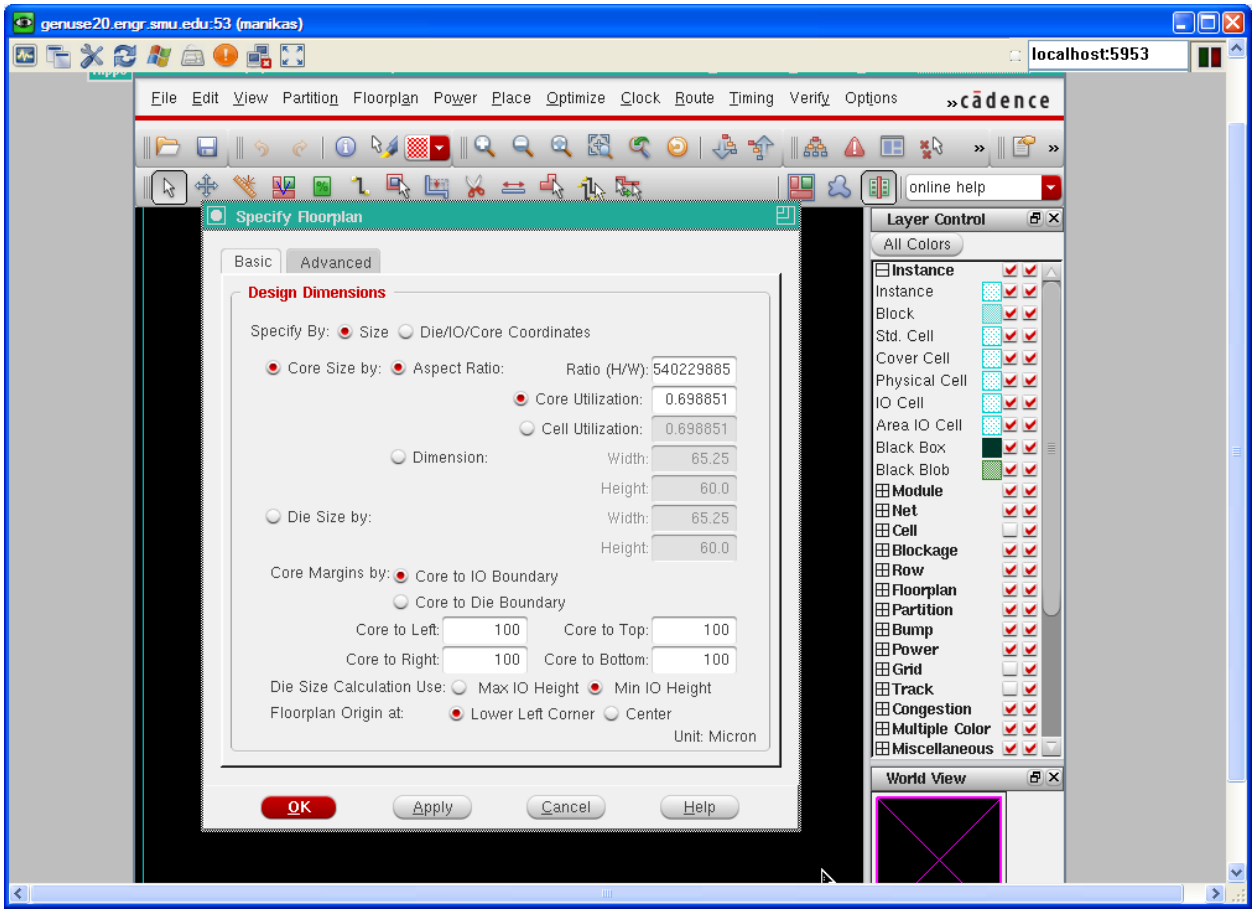


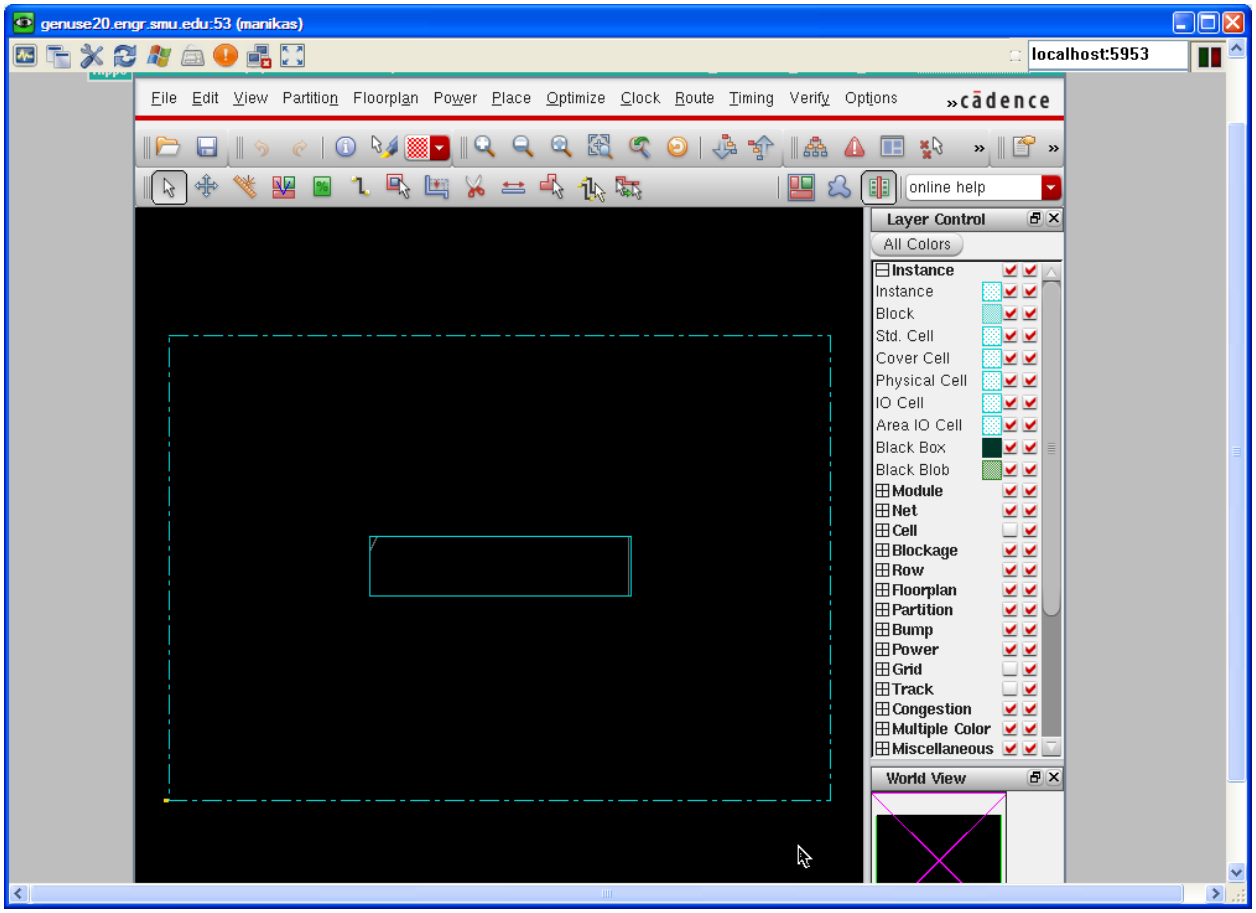
3 Floorplanning

3.1 Specify Floorplan

In Encounter tool menu bar, select **Floorplan**, **Specify Floorplan** to get the **Specify Floorplan** window.

1. In the **Basic** tab, select the following options:
    a. **Core Margins** – select Core to IO Boundary and set all margins to **100**
2. Click on **OK**.


genuse20.engr.smu.edu:53 (manikas)
localhost:5953
File Edit View Partition Floorplan Power Place Optimize Clock Route Timing Verify Options
cadence
online help
Specify Floorplan
Basic
Advanced
Design Dimensions
Specify By: Size Die/IO/Core Coordinates
Core Size by: Aspect Ratio:
Ratio (H/W): 540229885
Core Utilization: 0.698851
Cell Utilization: 0.698851
Dimension:
Width: 65.25
Height: 60.0
Die Size by:
Width: 65.25
Height: 60.0
Core Margins by: Core to IO Boundary
Core to Die Boundary
Core to Left: 100
Core to Top: 100
Core to Right: 100
Core to Bottom: 100
Die Size Calculation Use: Max IO Height Min IO Height
Floorplan Origin at: Lower Left Corner Center
Unit: Micron
OK
Apply
Cancel
Help
Layer Control
All Colors
Instance
Instance
Block
Std. Cell
Cover Cell
Physical Cell
IO Cell
Area IO Cell
Black Box
Black Blob
Module
Net
Cell
Blockage
Row
Floorplan
Partition
Bump
Power
Grid
Track
Congestion
Multiple Color
Miscellaneous
World View

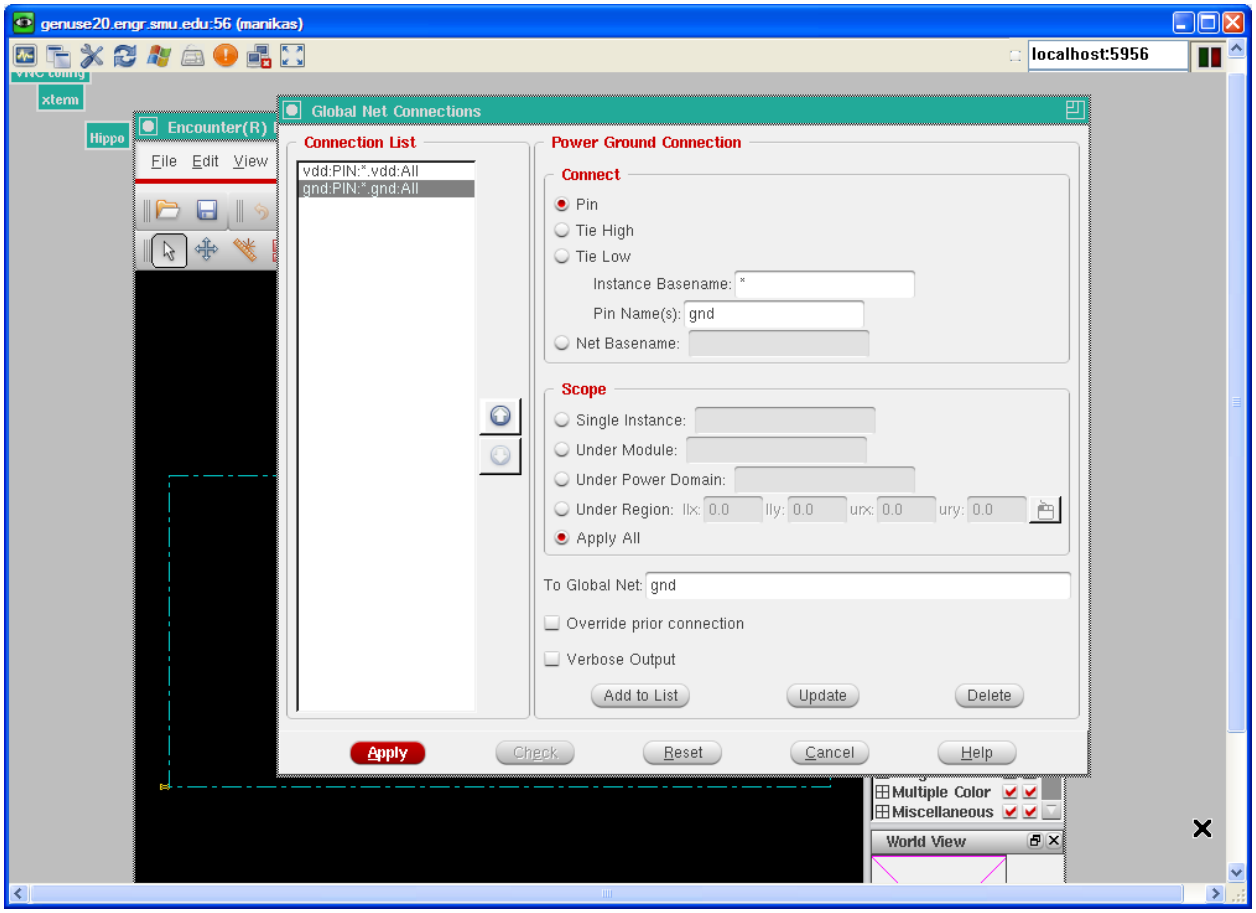


4 Power Planning

4.1 Connect Global Nets

In Encounter tool menu bar, select **Power, Connect Global Nets** to get the **Global Net Connections** Window.

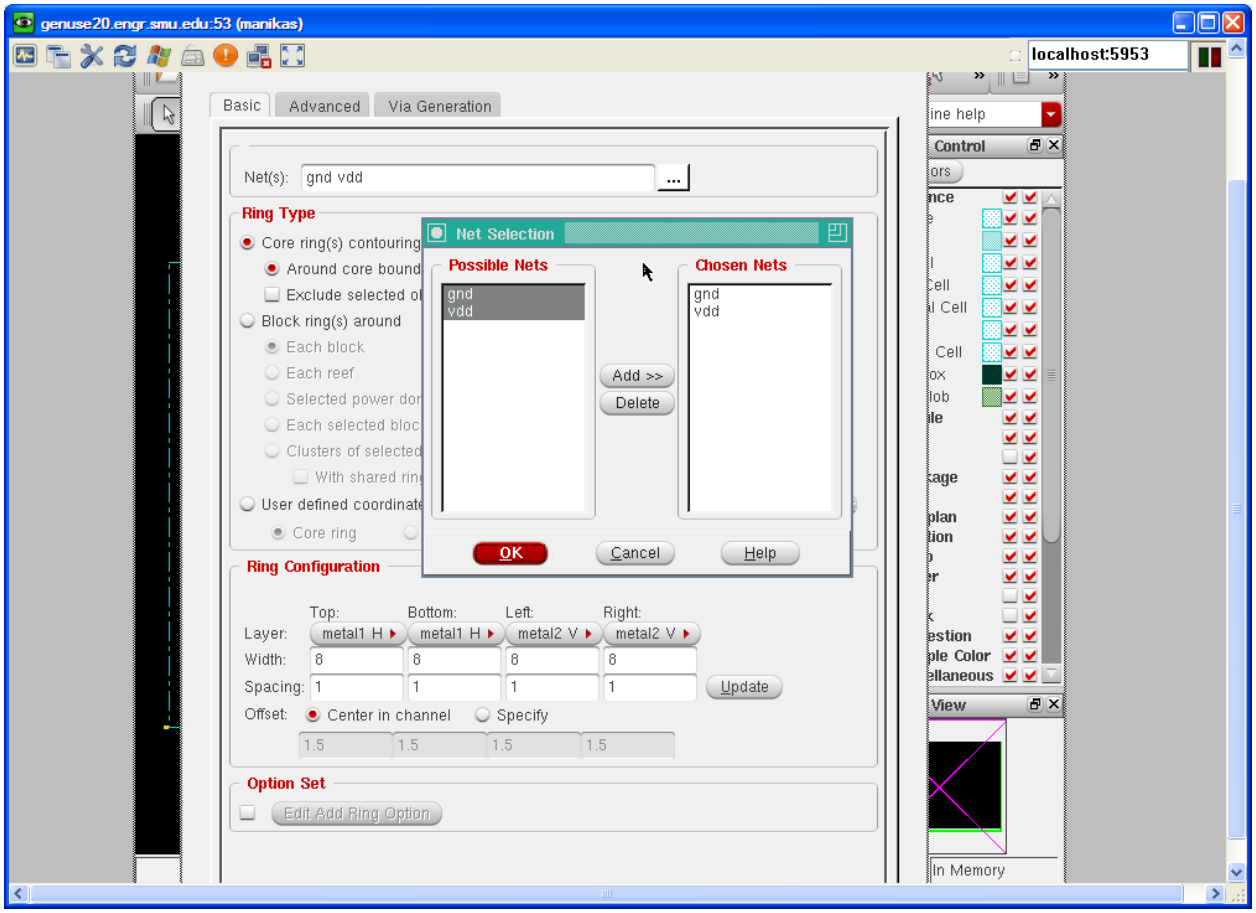
1. In **Power Ground Connection**
    a. In the **Connect** area, select **Pin**
    b. In the **Scope** area, select **Apply All**
2. For each net **vdd** and **gnd**, do the following:
    a. Enter the net name (vdd or gnd) in the following boxes:
        i. "To Global Net"
        ii. "Pin Name(s)"
    b. Click on the "Add to List" button
3. Click Apply, then click Cancel



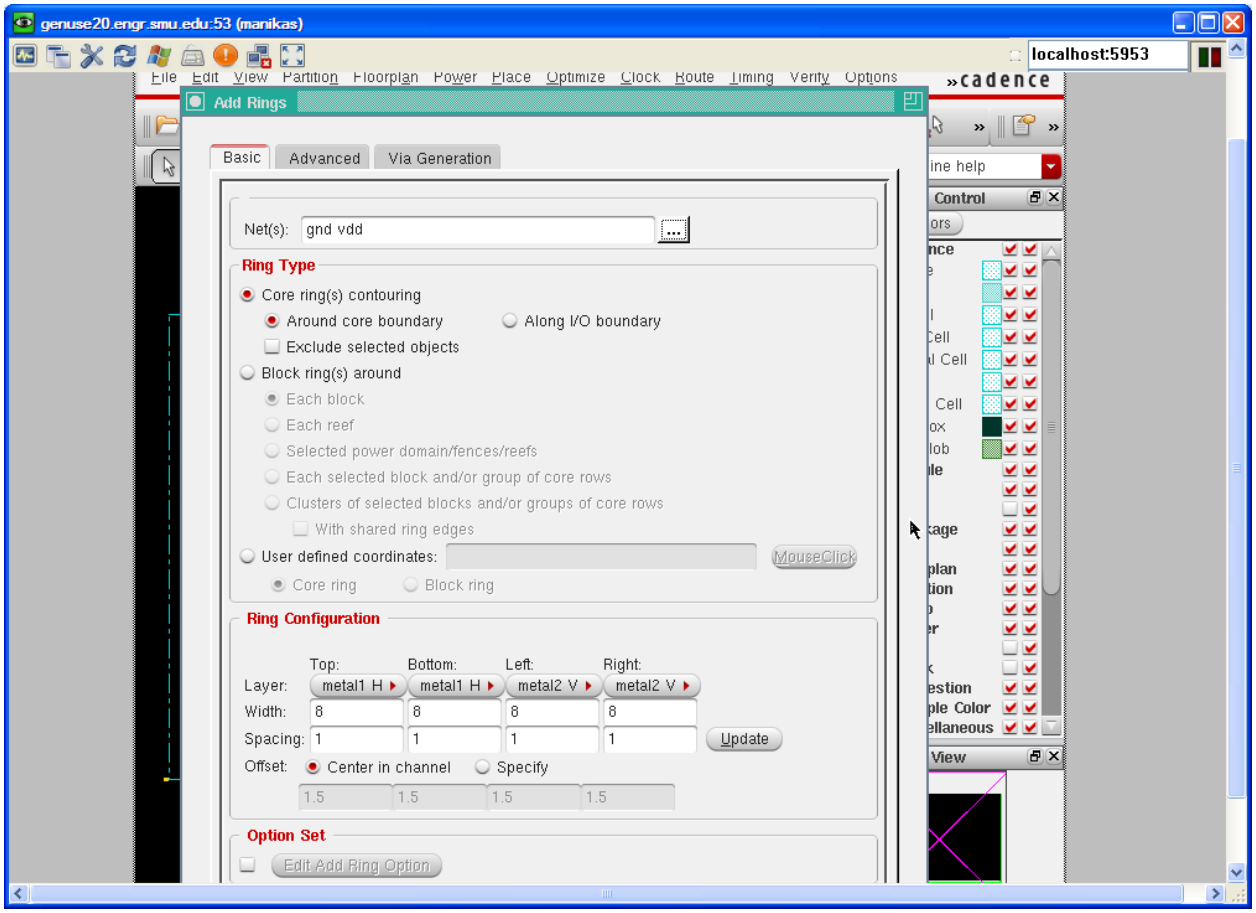
4.2 Power Rings

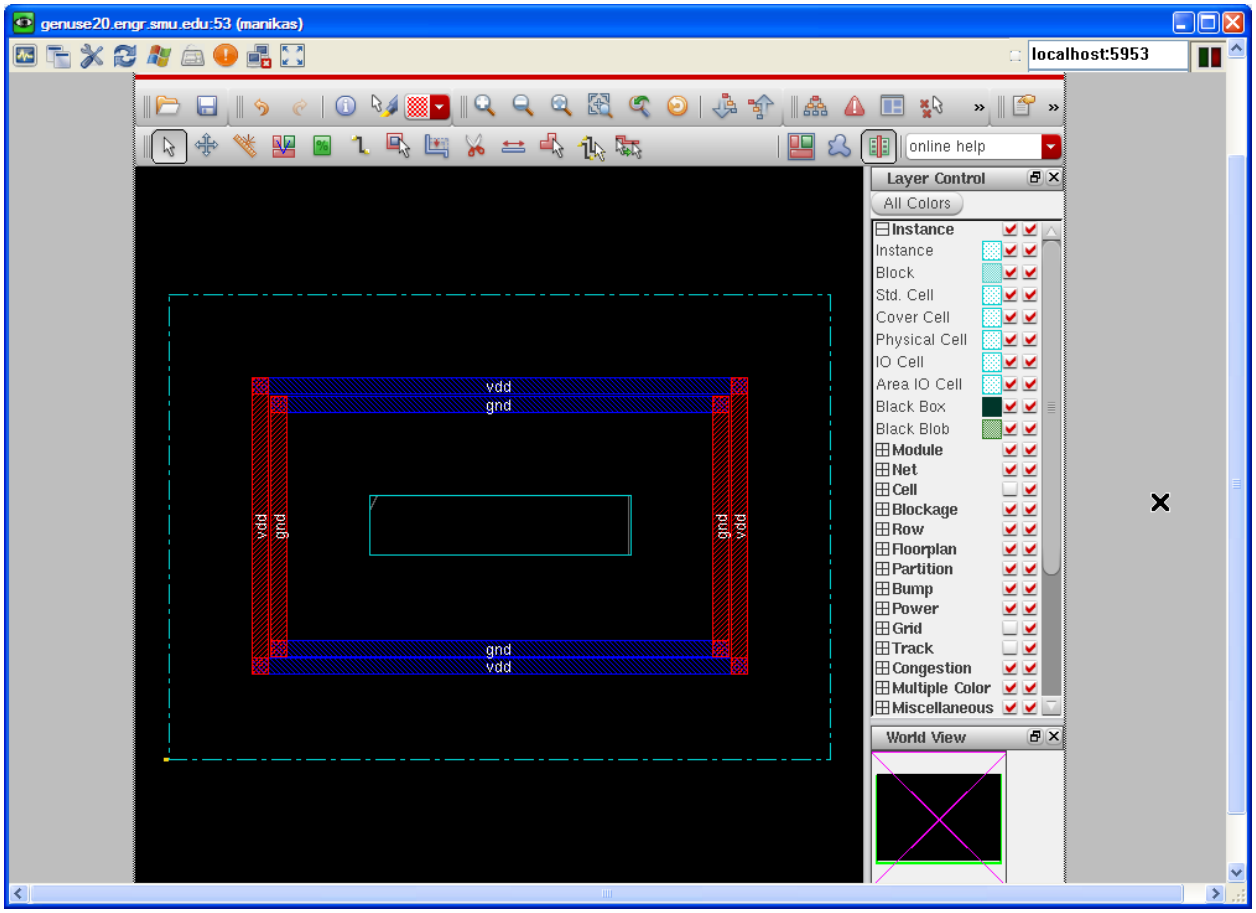
In Encounter tool menu bar, select **Power, Power Planning, Add Rings** to get the **Add Rings** window.

1. For Net(s), enter **vdd** and **gnd** nets as follows:
    a. Click on […] box to get Net Selection window
    b. Select **vdd** and **gnd** from Possible Nets column
    c. Click **Add** to copy to Chosen Nets column
    d. Click OK



2. In **Ring Configuration**, select **metal1** for Top and Bottom, **metal2** for Left and Right.
    a. Width should be 8
    b. Spacing should be 1
    c. Offset should be “Center in channel”
3. Click OK

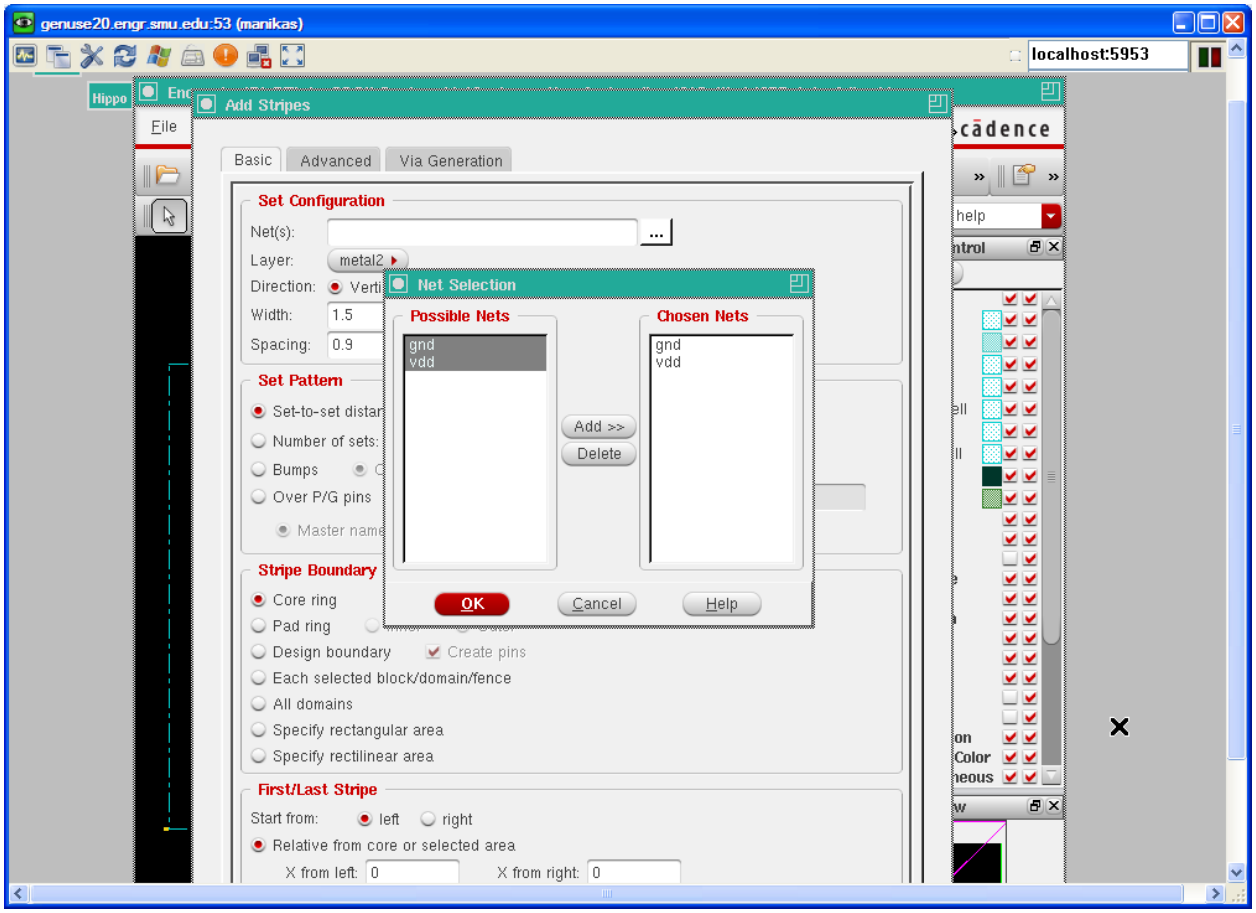

genuse20.engr.smu.edu:53 (manikas)
localhost:5953
File Edit View Partition Floorplan Power Place Optimize Clock Route Timing Verify Options
»cadence
Add Rings
Basic
Advanced
Via Generation
Net(s): gnd vdd
Ring Type
Core ring(s) contouring
Around core boundary
Along I/O boundary
Exclude selected objects
Block ring(s) around
Each block
Each reef
Selected power domain/fences/reefs
Each selected block and/or group of core rows
Clusters of selected blocks and/or groups of core rows
With shared ring edges
User defined coordinates:
MouseClick
Core ring
Block ring
Ring Configuration
Top:
Bottom:
Left:
Right:
Layer:
metal1 H
metal1 H
metal2 V
metal2 V
Width:
8
8
8
8
Spacing:
1
1
1
1
Update
Offset:
Center in channel
Specify
1.5
1.5
1.5
1.5
Option Set
Edit Add Ring Option
Control
View



4.3 Power Stripes

In Encounter tool menu bar, select **Power, Power Planning, Add Stripes** to get the **Add Stripes** window.

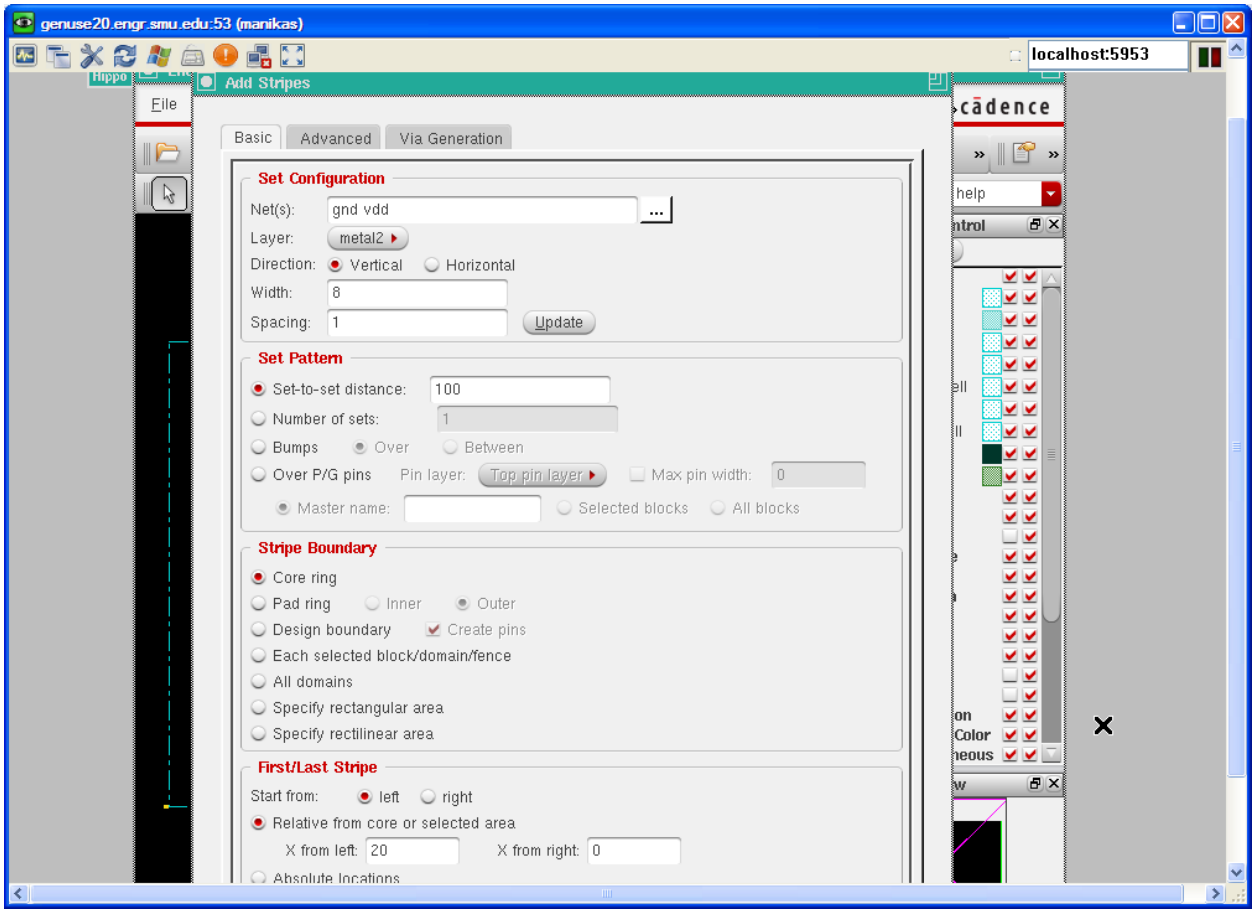
1. **Basic** Tab
    a. For Net(s), enter **vdd** and **gnd** nets as follows:
        i. Click on […] box to get Net Selection window
        ii. Select **vdd** and **gnd** from Possible Nets column
        iii. Click Add to copy to Chosen Nets column
        iv. Click OK



b. In **Set Configuration**, select Layer metal2 and Direction vertical. Width should be 8 and Spacing should be 1.

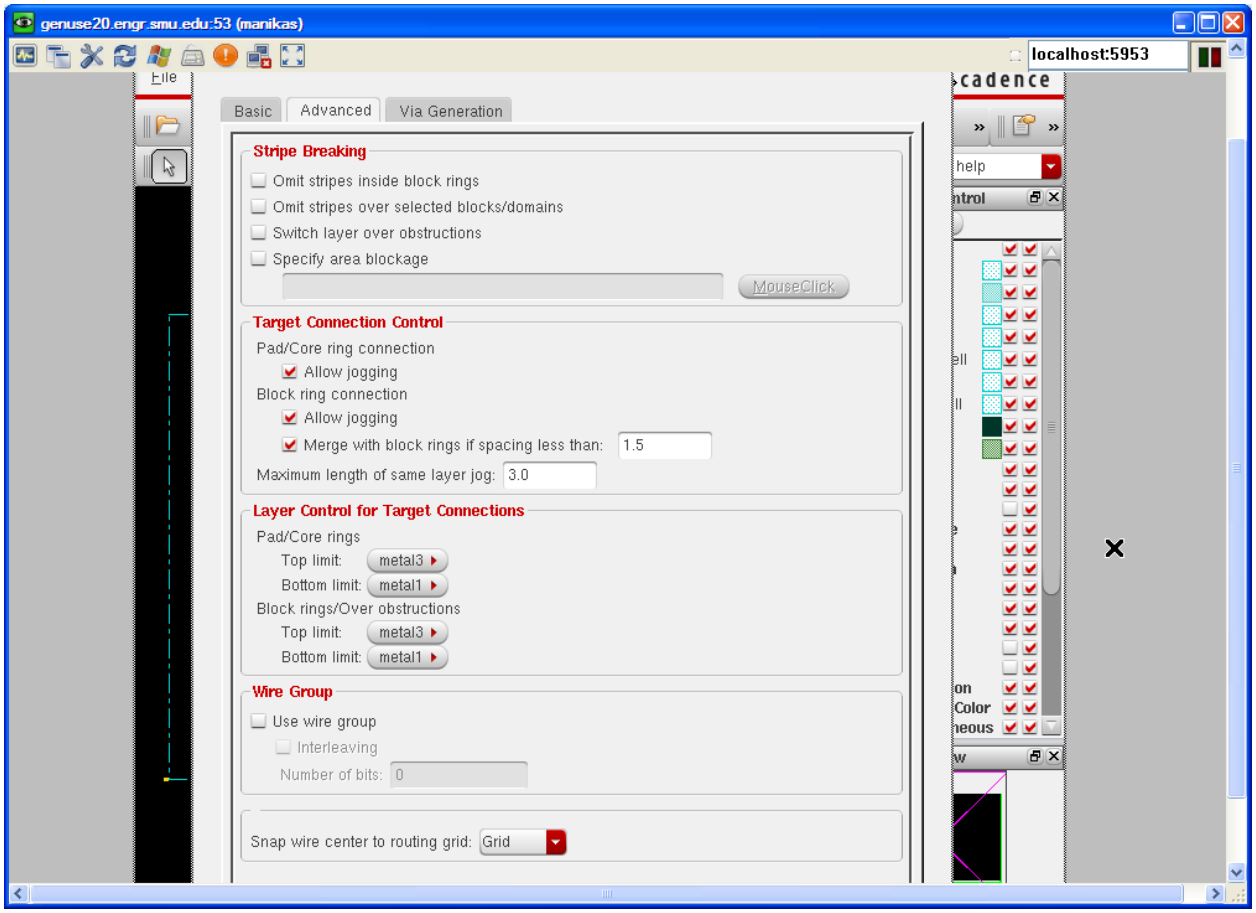
c. In **Set Pattern**, set Set-to-set distance to **100**

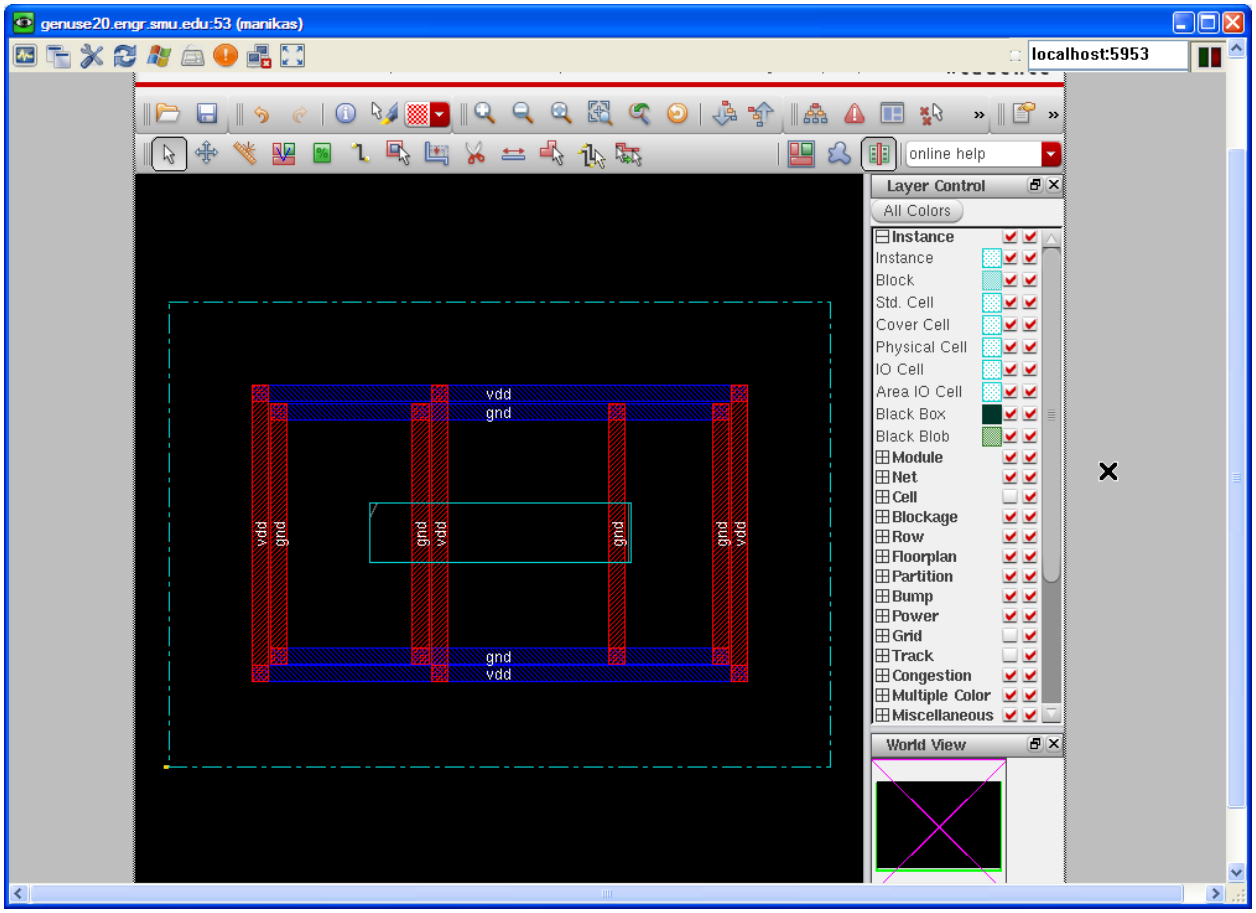
d. In **First/Last Stripe**, select Relative from core or selected area, X from left to 20



2. **Advanced** Tab
    a. Set Snap wire center to routing grid as Grid
3. Click OK

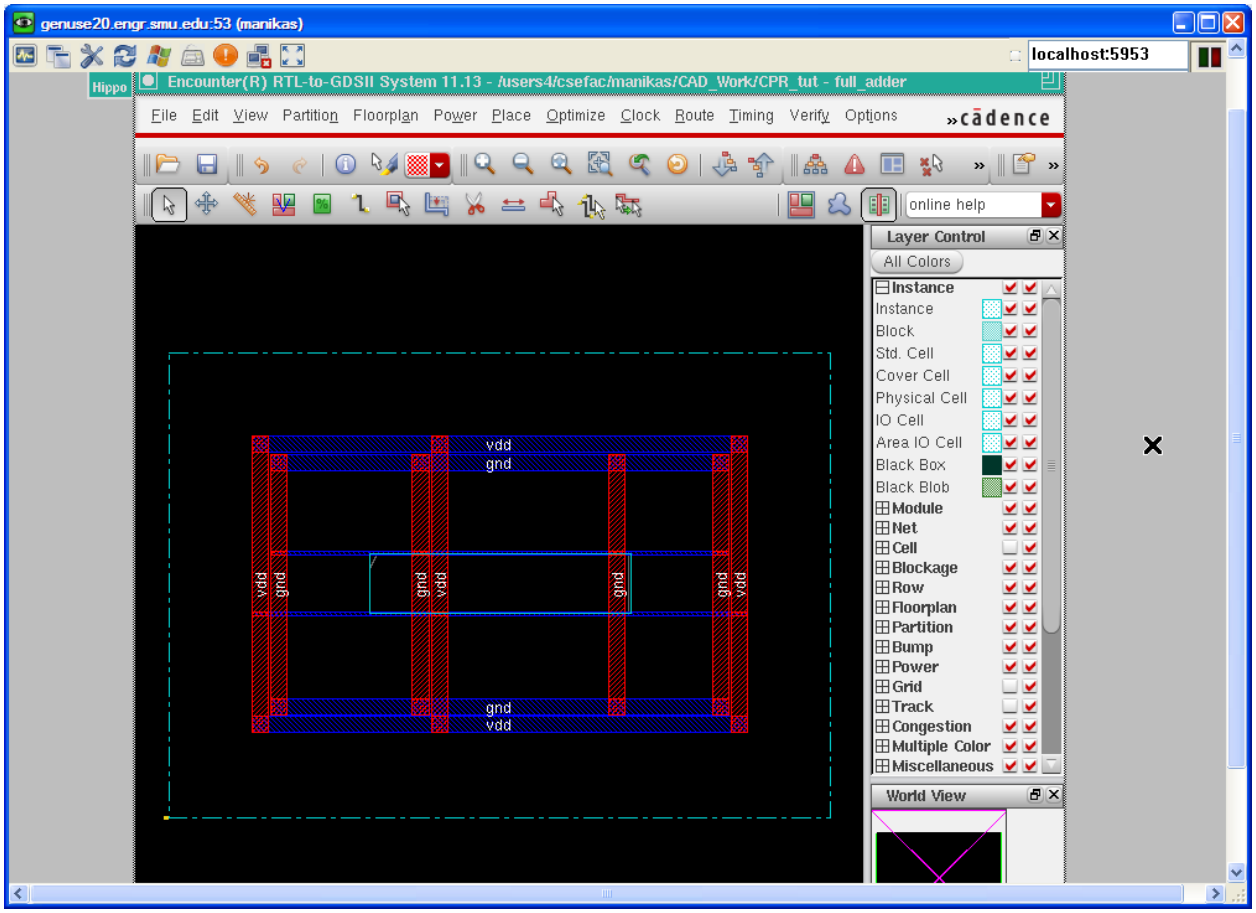
NOTE: MAY NEED TO USE ALT-RIGHT MOUSE TO MOVE WINDOW TO GET TO OK BUTTON (SEE HINT IN SECTION 1.1 above).


genuse20.engr.smu.edu:53 (manikas)
localhost:5953
File
Basic
Advanced
Via Generation
Stripe Breaking
Omit stripes inside block rings
Omit stripes over selected blocks/domains
Switch layer over obstructions
Specify area blockage
MouseClick
Target Connection Control
Pad/Core ring connection
Allow jogging
Block ring connection
Allow jogging
Merge with block rings if spacing less than: 1.5
Maximum length of same layer jog: 3.0
Layer Control for Target Connections
Pad/Core rings
Top limit: metal3
Bottom limit: metal1
Block rings/Over obstructions
Top limit: metal3
Bottom limit: metal1
Wire Group
Use wire group
Interleaving
Number of bits: 0
Snap wire center to routing grid: Grid
cadence
help



4.4 Connect Power to Standard Cell Rows

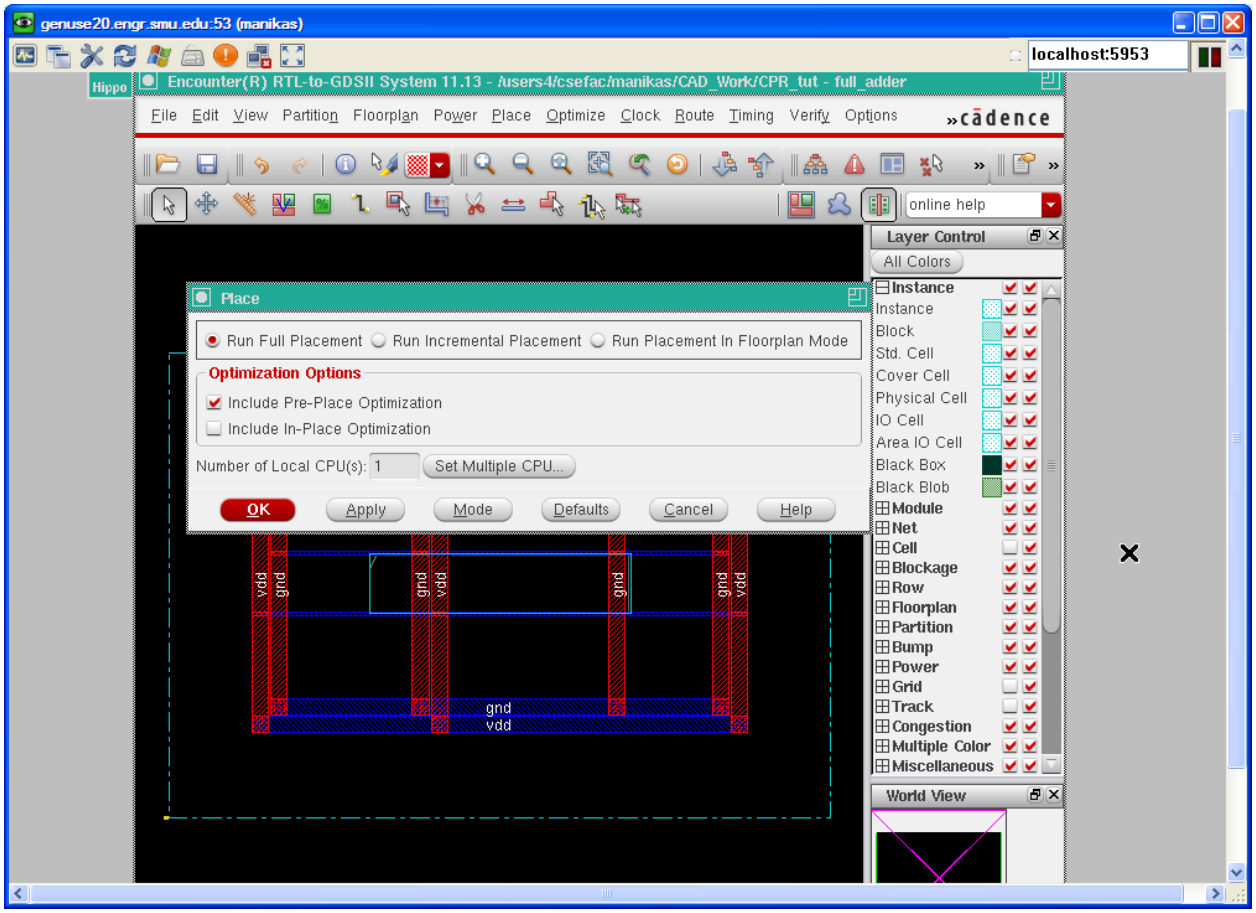
In Encounter tool menu bar, select **Route, Special Route**, and click OK. This will create power (vdd) and ground (gnd) rails for your standard cell rows. **Save your design using the procedure described in Section 2.1 above.**



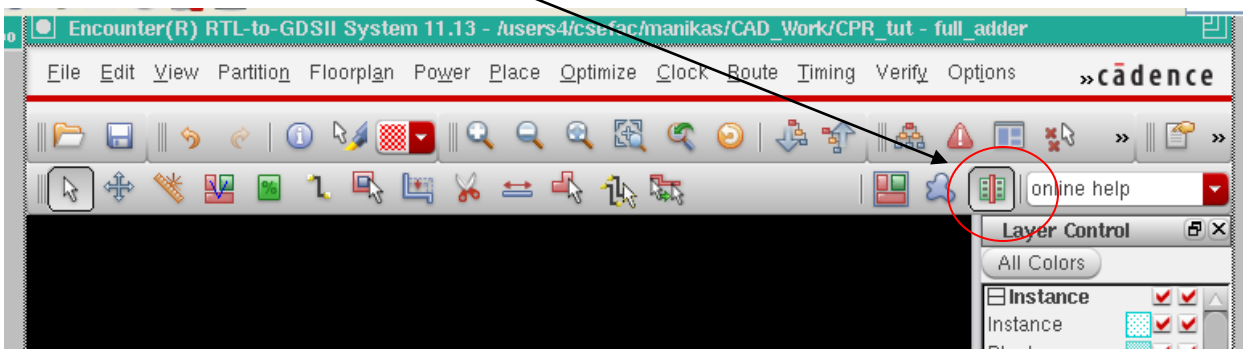
5 Placing the Standard Cells

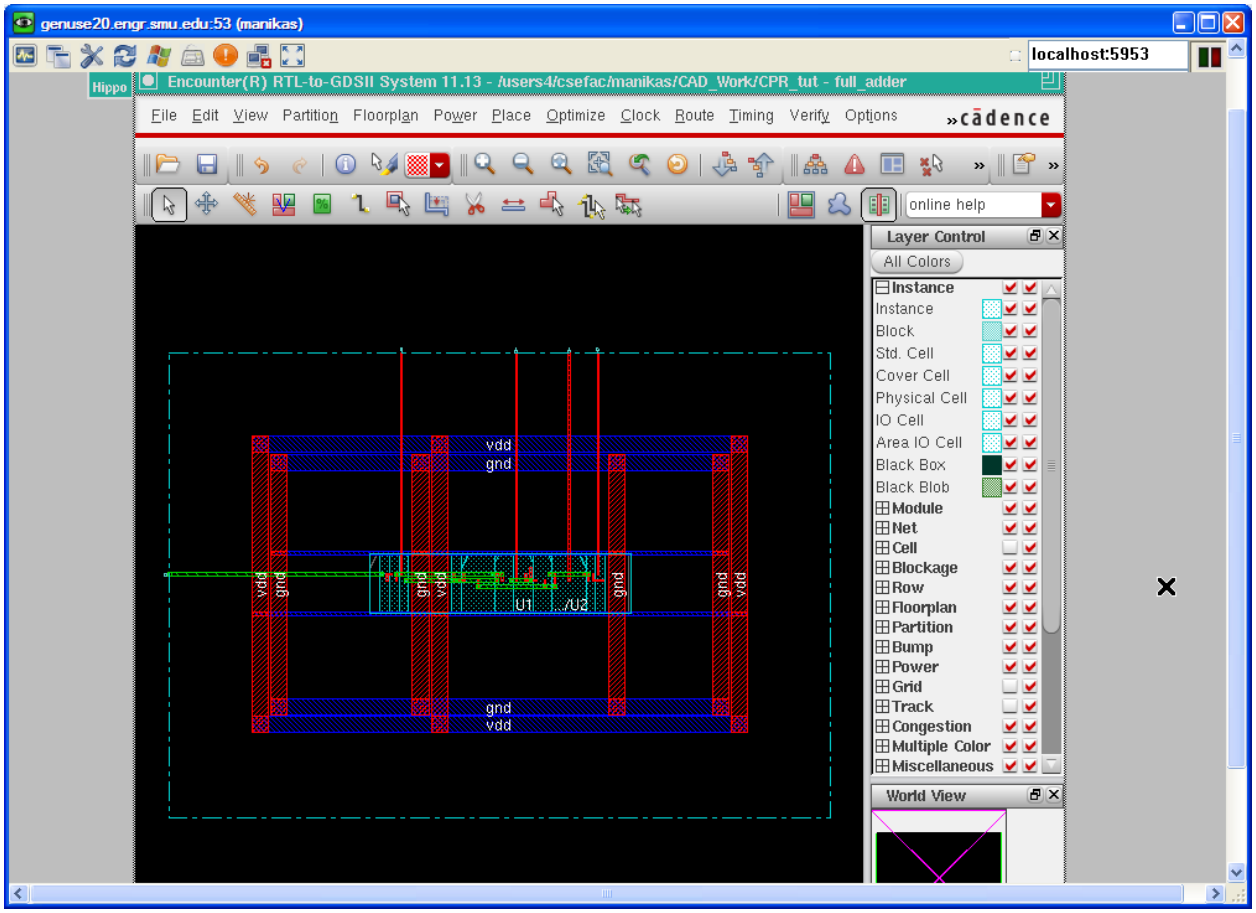
In Encounter tool menu bar, select **Place, Standard Cells** to get the Place window.

1. Select “Run Full Placement” and “Include Pre-Place Optimization”
2. Click OK



After cells are placed, change to **Physical View** in the Encounter Window to see placement results.

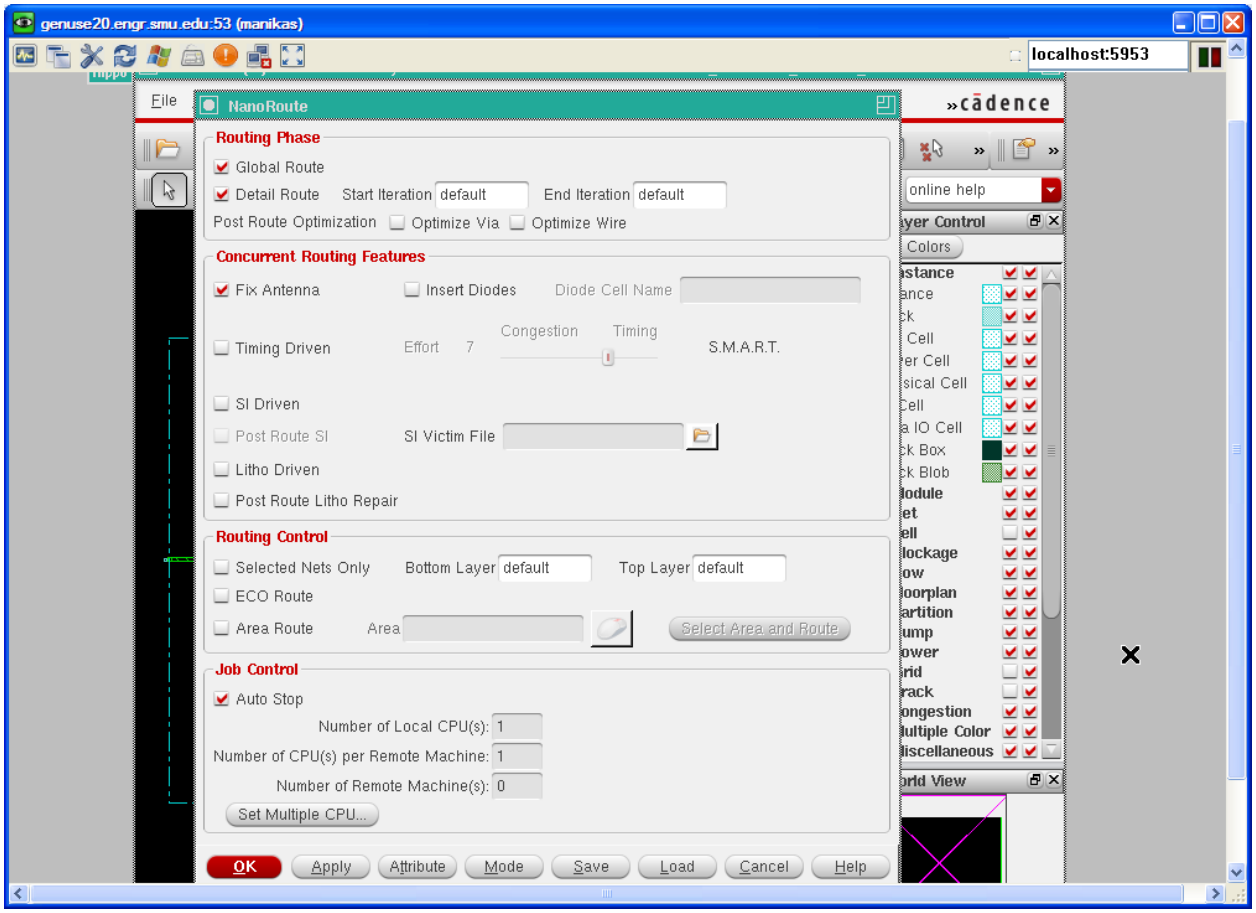


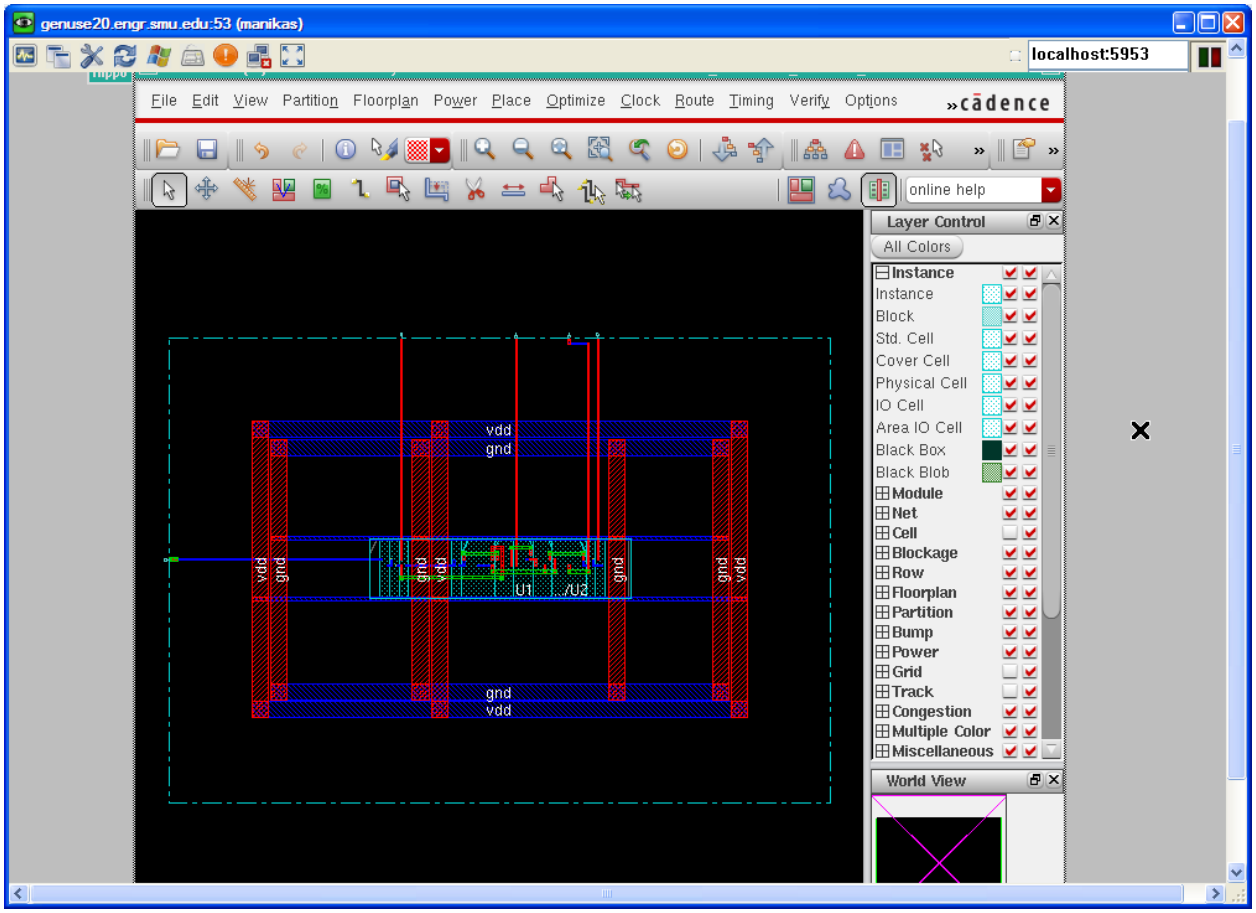


6 Routing

In Encounter tool menu bar, select **Route, NanoRoute, Route** to get the NanoRoute window.

1. Click OK.


genuse20.engr.smu.edu:53 (manikas)
localhost:5953
File
NanoRoute
»cadence
Routing Phase
Global Route
Detail Route
Start Iteration default
End Iteration default
Post Route Optimization
Optimize Via
Optimize Wire
Concurrent Routing Features
Fix Antenna
Insert Diodes
Diode Cell Name
Timing Driven
Effort 7
Congestion
Timing
S.M.A.R.T.
SI Driven
Post Route SI
SI Victim File
Litho Driven
Post Route Litho Repair
Routing Control
Selected Nets Only
Bottom Layer default
Top Layer default
ECO Route
Area Route
Area
Select Area and Route
Job Control
Auto Stop
Number of Local CPU(s): 1
Number of CPU(s) per Remote Machine: 1
Number of Remote Machine(s): 0
Set Multiple CPU...
OK
Apply
Attribute
Mode
Save
Load
Cancel
Help
online help
Colors


genuse20.engr.smu.edu:53 (manikas)
localhost:5953
File Edit View Partition Floorplan Power Place Optimize Clock Route Timing Verify Options
cadence
online help
Layer Control
All Colors
Instance
Instance
Block
Std. Cell
Cover Cell
Physical Cell
IO Cell
Area IO Cell
Black Box
Black Blob
Module
Net
Cell
Blockage
Row
Floorplan
Partition
Bump
Power
Grid
Track
Congestion
Multiple Color
Miscellaneous
World View
vdd
gnd
U1
U3