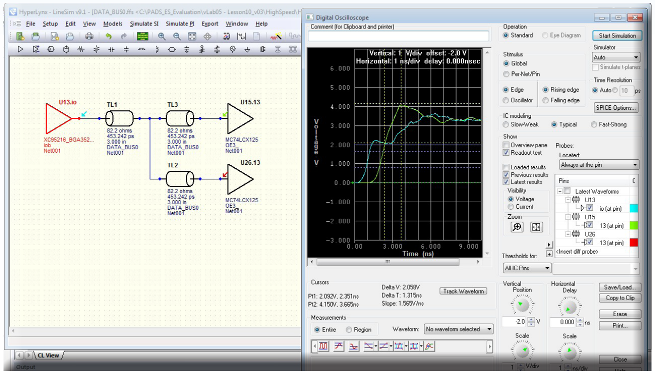
Pre-Layout Analysis

Lab 5

- Pre-Layout Signal Integrity Analysis



Operation: ● Standard ○ Eye Diagram

Simulator: Auto

☐ Simulate t-planes

Time Resolution: ● Auto ○ 10 ps

Stimulus: ● Global ○ Per-Net/Pin

● Edge ○ Oscillator

● Rising edge ○ Falling edge

IC modeling: ○ Slow-Weak ● Typical ○ Fast-Strong

Show: ☐ Overview pane ☑ Readout text

Probes: Located: Always at the pin

☐ Loaded results
☑ Previous results
☑ Latest results

Visibility: ● Voltage ○ Current

Thresholds for: All IC Pins

Cursors

Pt1: 2.092V, 2.351ns
Pt2: 4.150V, 3.665ns

Delta V: 2.058V
Delta T: 1.315ns
Slope: 1.565V/ns

Measurements: ● Entire ○ Region

Waveform: No waveform selected

Vertical Position: -2.0 V

Horizontal Delay: 0.000 ns

Scale: 1 V/div

Scale: 1 ns/div

Lab 5: Pre-Layout Signal Integrity Analysis

HyperLynx LineSim is a pre-layout PCB design simulation and analysis tool that enables you to evaluate the signal integrity performance of signal nets. In this exercise, you will experience the process of selecting a net for simulation, reviewing Simulation Models assigned in PADS Schematic Design environment, selecting a net for analysis, perform an analysis and save the analysis results for future use.

LineSim Link

LineSim Link can export a net to HyperLynx LineSim for pre-layout simulation.

① In PADS Schematic Design environment select **File > Open > Project** and select **E:\PADS_ES_Evaluation\Lesson10\Lesson10.prj**.

② In the Project Navigator, double-click the **Lesson 10** board, then double-click the **CORPORATE** schematic to display the list of schematic sheets.

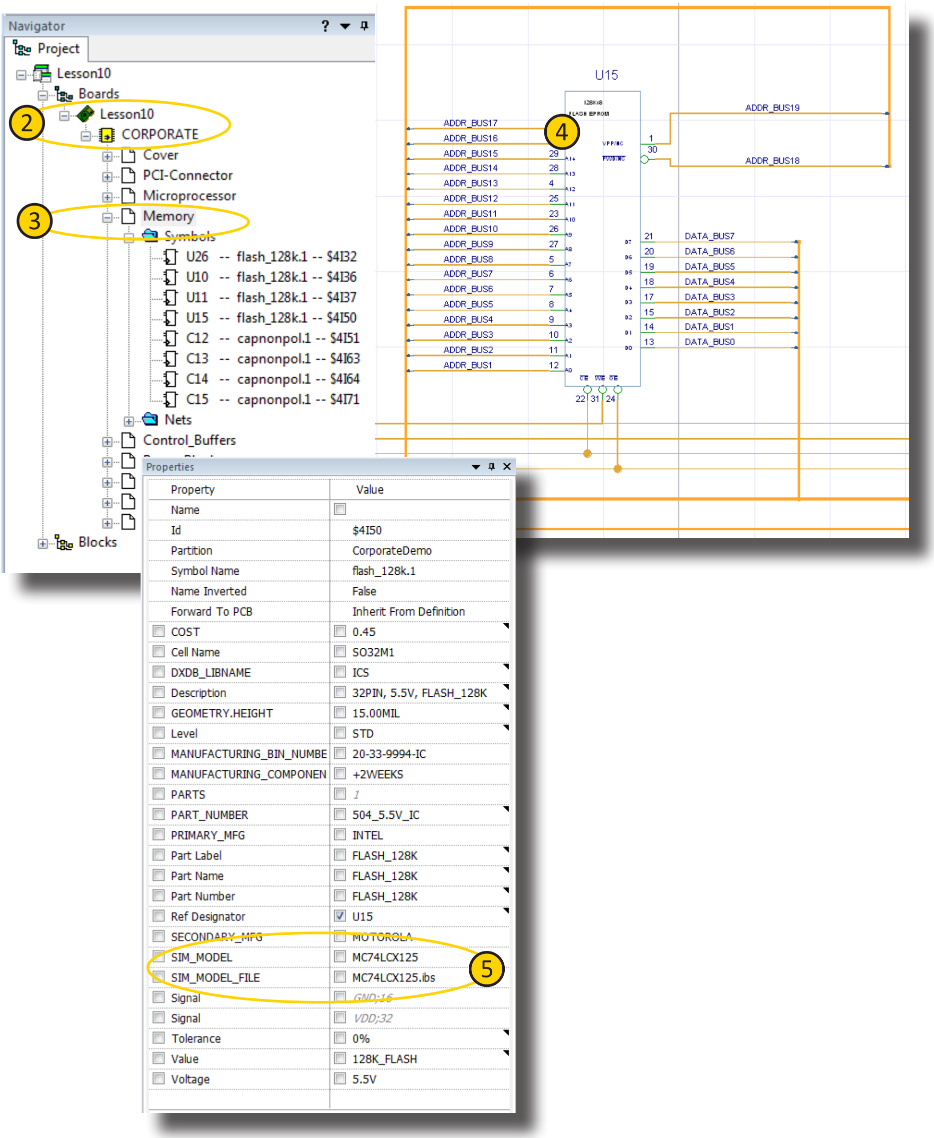
③ Now double-click the **Memory** schematic sheet in the Project Navigator.

④ Zoom to the upper left **IC** shown on the **Memory** sheet. Select the IC **U15**.

Note: Set the **Selection Filter** to **Symbol** if necessary.

⑤ In the **Properties** window, review the assigned Simulation IBIS models: **SIM_MODEL** and **SIM_MODEL_FILE**. (You may need to scroll down to see them).

Note: If the Properties Window is not visible, click the Properties icon on the View toolbar.

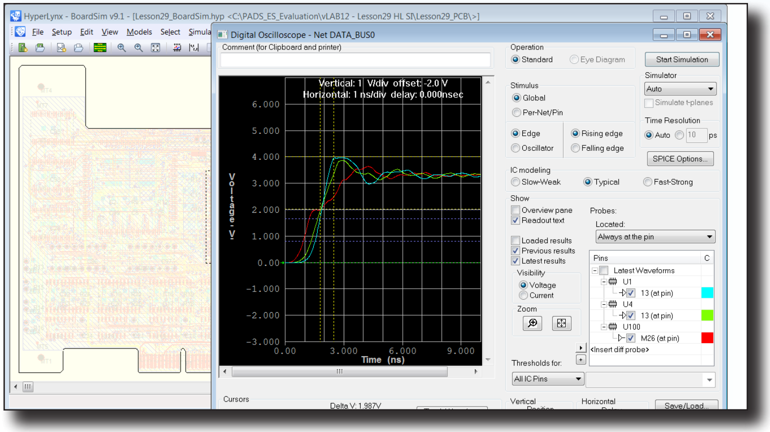


Property	Value
Name	☐
Id	$4I50
Partition	CorporateDemo
Symbol Name	flash_128k.1
Name Inverted	False
Forward To PCB	Inherit From Definition
☐ COST	☐ 0.45
☐ Cell Name	☐ SO32M1
☐ DXDB_LIBNAME	☐ ICS
☐ Description	☐ 32PIN, 5.5V, FLASH_128K
☐ GEOMETRY.HEIGHT	☐ 15.00MIL
☐ Level	☐ STD
☐ MANUFACTURING_BIN_NUMBE	☐ 20-33-9994-IC
☐ MANUFACTURING_COMPONEN	☐ +2WEEKS
☐ PARTS	☐ *1*
☐ PART_NUMBER	☐ 504_5.5V_IC
☐ PRIMARY_MFG	☐ INTEL
☐ Part Label	☐ FLASH_128K
☐ Part Name	☐ FLASH_128K
☐ Part Number	☐ FLASH_128K
☐ Ref Designator	☑ U15
☐ SECONDARY_MFG	☐ MOTOROLA
☐ SIM_MODEL	☐ MC74LCX125
☐ SIM_MODEL_FILE	☐ MC74LCX125.ibs
☐ Signal	☐ *GND;16*
☐ Signal	☐ *VDD;32*
☐ Tolerance	☐ 0%
☐ Value	☐ 128K_FLASH
☐ Voltage	☐ 5.5V

Post-Layout Analysis

Lab 12

- Signal Integrity Analysis



Operation: ● Standard ○ Eye Diagram

Simulator: Auto

☐ Simulate t-planes

Stimulus: ● Global ○ Per-Net/Pin

● Edge ○ Oscillator

● Rising edge ○ Falling edge

Time Resolution: ● Auto ○ 10 ps

IC modeling: ○ Slow-Weak ● Typical ○ Fast-Strong

Show: ☐ Overview pane ☑ Readout text

Probes: Located: Always at the pin

☐ Loaded results ☑ Previous results ☑ Latest results

Visibility: ● Voltage ○ Current

Pins	C
☐ Latest Waveforms	
U1	
☑ 13 (at pin)	🟦
U4	
☑ 13 (at pin)	🟩
U100	
☑ M26 (at pin)	🟥
<Insert diff probe>	

Thresholds for: All IC Pins

Delta V: 1.987V

Lab 12: HyperLynx BoardSim Simulation

This exercise will walk you through the process of sending a finished design from PADS Layout to HyperLynx BoardSim and selecting a net for simulation. We will also compare the simulation results with the pre-layout stage that we prepared earlier in LineSim.

HyperLynx BoardSim

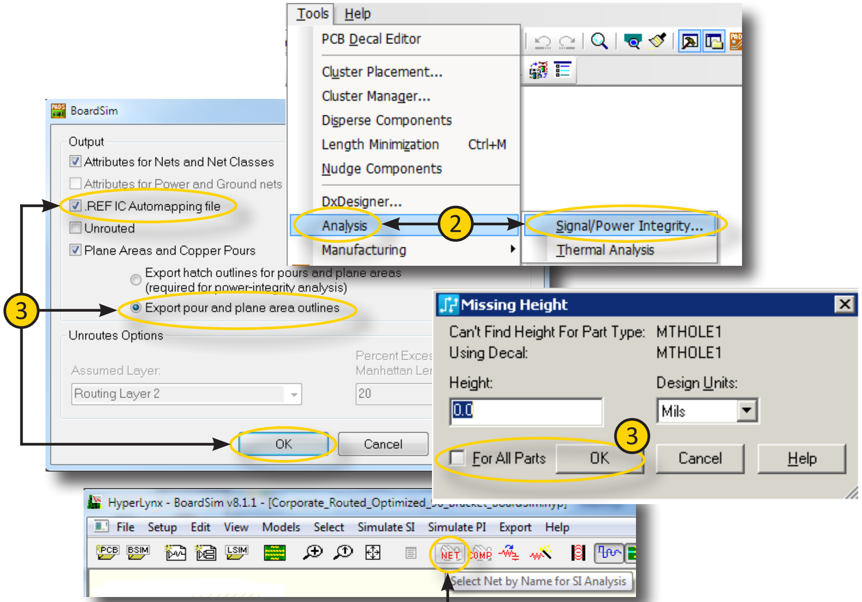
① In PADS Layout, select **File > Open** and open **E:\PADS_ES_Evaluation\Lesson29\Lesson29.pcb**.

② Select **Tools > Analysis > Signal/Power Integrity ...**

③ In the BoardSim dialog, enable the **.REF IC Automapping file** option, then select the radio button next to **Export pour and plane outlines** and finally select the **OK** button. This will extract all of the data and load design into HyperLynx. When prompted with the **Missing Height** dialog, enable the **For All Parts** option checkbox and click OK.

④ In HyperLynx BoardSim select the **NET** button.

⑤ In the **Select Net by Name** dialog, scroll down and select **DATA_BUS0** net and then click the **OK** button. This will only show that specific net routed on the board.



BoardSim

Output

☑ Attributes for Nets and Net Classes

☐ Attributes for Power and Ground nets

☑ .REF IC Automapping file

☐ Unrouted

☑ Plane Areas and Copper Pours

○ Export hatch outlines for pours and plane areas (required for power-integrity analysis)

● Export pour and plane area outlines

Unroutes Options

Assumed Layer: Routing Layer 2

Percent Exces / Manhattan Len: 20

Missing Height

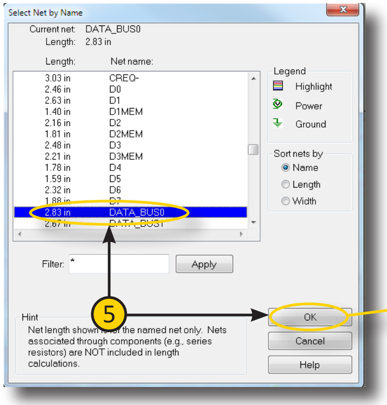
Can't Find Height For Part Type: MTHOLE1

Using Decal: MTHOLE1

Height: 0.0

Design Units: Mils

☐ For All Parts



Current net: DATA_BUS0

Length: 2.83 in

Length:	Net name:
3.03 in	CREQ-
2.46 in	D0
2.63 in	D1
1.40 in	D1MEM
2.16 in	D2
1.81 in	D2MEM
2.48 in	D3
2.21 in	D3MEM
1.78 in	D4
1.59 in	D5
2.32 in	D6
1.88 in	D7
2.83 in	DATA_BUS0
2.67 in	DATA_BUS1

Sort nets by

● Name

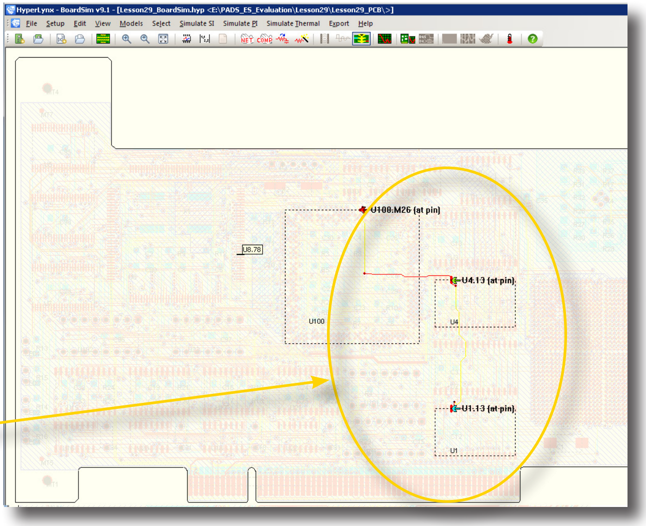
○ Length

○ Width

Filter: *

Hint

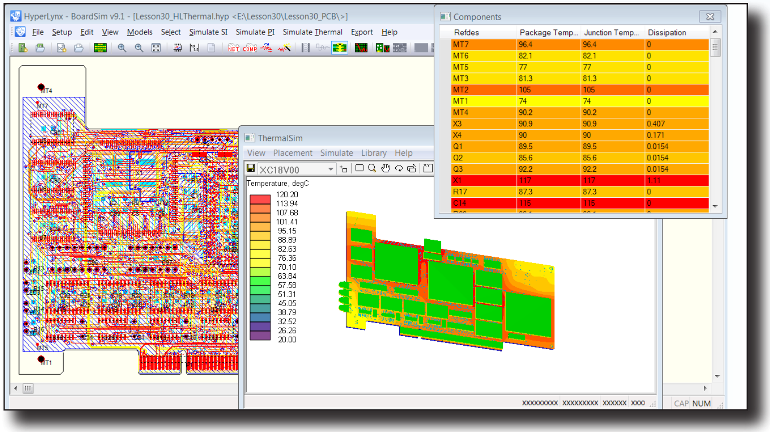
Net length shown is for the named net only. Nets associated through components (e.g., series resistors) are NOT included in length calculations.



Post-Layout Analysis

Lab 13

- Thermal Analysis



Refdes	Package Temp...	Junction Temp...	Dissipation
MT7	96.4	96.4	0
MT6	82.1	82.1	0
MT5	77	77	0
MT3	81.3	81.3	0
MT2	105	105	0
MT1	74	74	0
MT4	90.2	90.2	0
X3	90.9	90.9	0.407
X4	90	90	0.171
Q1	89.5	89.5	0.0154
Q2	85.6	85.6	0.0154
Q3	92.2	92.2	0.0154
X1	117	117	1.11
R17	87.3	87.3	0
C14	115	115	0

Lab 13: HyperLynx Thermal Analysis

This exercise will walk you through the process of sending a finished design from PADS Layout to HyperLynx Thermal for evaluating any possible heat problems and possible solutions to eliminate excessive heat areas. This exercise does not cover all of the aspects of the HyperLynx Thermal software but highlights a few important features.

HyperLynx Thermal Analysis

This section will demonstrate how to perform a HyperLynx Thermal simulation.

① In PADS Layout, select **File > Open** and select **E:\PADS_ES_Evaluation\Lesson30\Lesson30.pcb**.

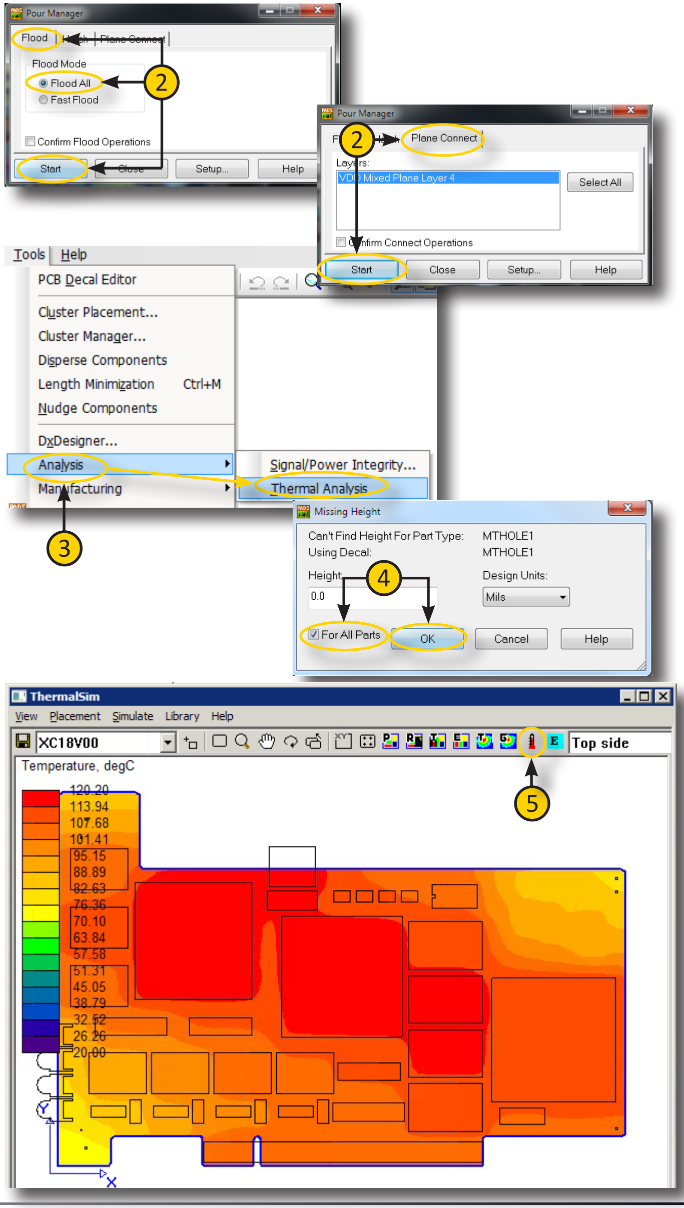
② We need to pour Copper and Split/Mixed planes before we transfer the design to HyperLynx Thermal. Select **Tools > Pour Manager** and in the Flood tab, select **Flood All**. Then click the **Start** button. Now select the **Plane Connect** tab and click the **Start** button (if any warning messages about missing thermal connections come up, please ignore). **Close** the Pour Manager window.

③ Select **Tools > Analysis > Thermal Analysis**.

④ In the **Missing Height** dialog, enable the check box **For All Parts**, then click **OK**. This will extract all of the data and load design into HyperLynx Thermal.

⑤ In HyperLynx Board Sim, if prompted by the Restore Session Edits dialog, click OK, then in the Thermal Sim window select the **Run Thermal Simulation** icon.

Note: Some components are running hot at 113degC. We will try to resolve two component problems.



Can't Find Height For Part Type: MTHOLE1
Using Decal: MTHOLE1
Height: 0.0
Design Units: Mils
☑ For All Parts

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