EE-584

INTRODUCTION TO VLSI DESIGN AND TESTING

REPORT ON

ETEST OP-AMP

SUBMITTED BY

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Introduction

An operational amplifier (op-amp) is basically a differential amplifier having a large voltage gain, very high input impedance and low output impedance. The op-amp has a "inverting" or (-) input and "non-inverting" or (+) input and a single output. Op-amps are widely used electronic devices today, being utilized in a vast array of consumer, industrial and scientific devices.

A few uses of op-amps include:
Audio and video pre-amplifiers and buffers, voltage comparators, differential amplifiers, differentiators and integrators, filters, precision rectifiers, voltage regulator and current regulator, analog-to-digital converter, digital-to-analog converter, voltage clamps, oscillators and waveform generators, Schmitt trigger, gyrator, comparator, active filter and as an analog computer.

In this project an op-amp is designed for certain specifications such as gain and slew rate. The process that is being used here is the 0.18 micro-meter process and corresponding values of threshold voltages and parameters like K (transconductance parameter in saturation) were used while designing the circuit. The variation in the performance of the op-amp with variations in the width and length of the CMOS were observed. Corner simulations in all possible cases such as varying temperature and power supply were performed and the variation in the performance of the op-amp was observed.

The schematics, layouts and simulations in this project were carried out in the Cadence Environment. Tools like the schematic editor and layout editor were used to draw the schematics and layouts. The spectre simulator was used to perform the various simulations shown in this document.

Block diagram

The general block diagram of an op-amp with an output buffer is shown below.

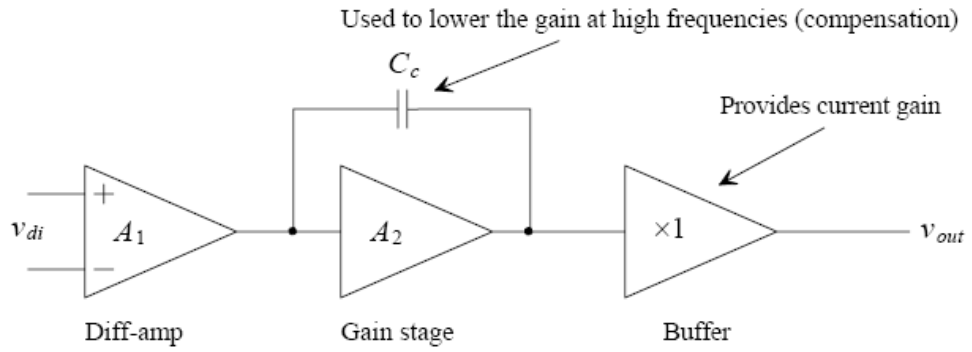


Figure 1 : Block diagram of two-stage op-amp with output buffer[1]

[1]The first stage of the op-amp is a differential amplifier. It has two inputs which are the inverting and non-inverting voltages. The difference of these voltages is the output of the differential stage. This is followed by the gain stage. This stage amplifies the voltage of the differential amplifier. If the op-amp is intended to drive a small purely capacitive load, which is the case in many switched capacitor or data conversion applications, the output buffer is not used. [1]

[1] = CMOS Circuit Design. Layout, and Simulation By R. Jacob Baker.

Design Strategy:

[2]The design process involves two distinct activities:

Architecture Design

• Find architecture already available and adapt it to present requirements

• Create a new architecture that can meet requirements

Component Design

• Design transistor sizes

• Design compensation network

If available architectures do not meet requirements, then an existing architecture must be modified, or a new one designed. Once a satisfactory architecture has been obtained, then devices and the compensation network must be designed.[2]

Circuit of the op-amp

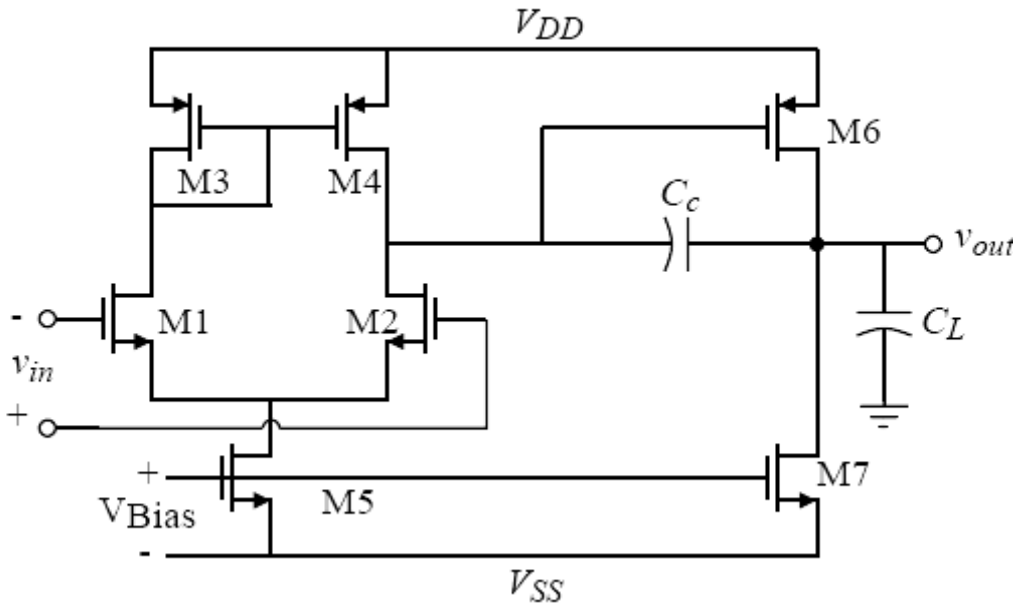


Figure 2 : Circuit Diagram of two stage op-amp [2]

In this project, an architecture that is already available is used and is adapted to the present requirements. For this architecture, devices and the compensation network is designed.

Design Procedure:

[2]In this project we aim to design an op-amp with a gain of 20000 V/V and a slew rate of 20 MV/Sec.

The steps that are followed in designing the op-amp are:

1. The compensation capacitance is chosen to be at least 0.22 times the load capacitance $Cc > 0.22C_{L.}$

Here Cc is the compensation capacitance and C_L is the load capacitance.

2. Determine the value for the "tail current" (I_5).

$I_5 = SR .Cc$

Here SR is the slew rate of the op-amp.

3. Design for S3 from the maximum input voltage specification.

$S3 = (\quad I_5 \div K'3\left(\left[VDD - Vin(\max) - |VT03|(\max) + VTI(\min)\right]^2\right)) \geq 1$

I_5 is the drain current of $M_{5,}$ VDD is the positive supply voltage, Vin is the input voltage, VT is the threshold voltage and K is the transconductance parameter (in saturation).

Also, S = (W/L).

4. Design for S_1 (S_2) to achieve the desired GB.

$g_{m1} = GB. Cc \Rightarrow S2 = g^2{}_{m2} / K'_2 I_5$

GB is the gain bandwidth and g_m is the small signal transconductance from gate to channel.

5. Design for S_5 from the minimum input voltage. First calculate V_{DS5} (sat) then find S_5.

$V_{DS5}(sat) = V_{in}(min) - V_{SS} - \sqrt{I5/\beta 1} - V_{T1}(\max)$

$S_5 = 2I_5 / K'_5 [V_{DS5}(sat)]^2$

Where, β is the MOS transconductance parameter and V_{SS} is the negative supply voltage.

6. Find g_{m6} and $S_{6.}$

$g_{m6} = 2.2g_{m2}(C_L/Cc)$

$S_6 = S_3 (g_{m6} / g_{m3})$

7. Calculate I_6:

$I_6 = (S_6/S_4)\ I_4 = (S_6/S_4)(I_5/2)$

8. Design S_7 to achieve the desired current ratios between I_5 and I_6.

$S_7 = (I_6/I_5)\ S_5$

9. Simulate the circuit to check to see that all specifications are met.[2]

Design and Calculations for an op-amp with given specifications

Specifications:

Gain = 20,000 V/V Slew rate = 20 MV/sec

The positive supply voltage VDD = 1.5V

The negative supply voltage VSS = -1.5V

The maximum input voltage Vin (max) = 1.4V

The minimum input voltage Vin (min) = -0.97V

The load capacitance C_L = 1pF and gain bandwidth = $2\Pi \times 27.5 \times 10^6$

For 0.18 micrometer process:

The threshold voltages for CMOS = Vthn = Vthp =0.3V $\pm 10\%$

The transconductance parameter (in saturation) for

NMOS = Kn = 288 μ A / V^2

PMOS = Kp = 77.84 μ A / V^2

[2] CMOS Analog Circuit Design By Phillip E. Allen and Douglas R. Holberg

1.) $Cc > 0.22C_{L.}$

$\Rightarrow Cc > 0.22 \times 1$ pF.

$\Rightarrow Cc > 0.22$ pF

Choosing the compensation capacitance, **Cc as 220 fF**.

2.) $I_5 = SR \cdot Cc$

$\Rightarrow I_5 = 20 \times 10^6 \times 220 \times 10^{-15} = 4.4 \times 10^{-6}$ A

3.) $S3 = \left(I_5 \div K'3\left(\left[VDD - Vin(\max) - |VT03|(\max) + VTI(\min)\right]^2\right)\right)$

$\Rightarrow S3 = (4.4 \times 10^{-6} \div 77.84 \times 10^{-6} ([1.5 - 1.4 - 0.345 + 0.255])^2)$

$\Rightarrow S3 \cong 5.$

$\Rightarrow$ **(W/L) 3 = (W/L) 4 = 5**

4.) $g_{m1} = GB. Cc$

$g_{m1} = 2\Pi \times 27.5 \times 10^6 \times 220 \times 10^{-15} = 38.01 \times 10^{-6}$

$\Rightarrow g_{m1} = g_{m2} = 38.01 * 10^{-6}$

$\Rightarrow S2 = g^2{}_{m2} / K'_2 I_5$

$\Rightarrow S2 = 38.01 \times 10^{-6} \times 38.01 * 10^{-6} \div (288 \times 10^{-6} \times 4.4 \times 10^{-6})$

$\Rightarrow S2 \cong 1$

$\Rightarrow$ **(W/L)2= (W/L)1= 1**

5.) $V_{DS5}(sat) = V_{in}(min) - V_{SS} - \sqrt{I5/\beta 1} - V_{T1}(\max)$

$\Rightarrow V_{DS5}(sat) = -0.97 - (-1.5) - \sqrt{(4.4 * 10^{-6}) \div 288 \times 1} - 0.345$

$\Rightarrow V_{DS5}(sat) = 0.061V$

$S_5 = 2I_5 / K'_5 [V_{DS5}(sat)]^2$

$\Rightarrow S_5 = 2 \times 4.4 \times 10^{-6} \div (288 \times 10^{-6} \times 0.061^2)$

$\Rightarrow S_5 \cong 8$

$\Rightarrow$ **(W/L)5 = 8**

6.) $g_{m6} = 2.2g_{m2}(C_L/Cc)$

$\Rightarrow g_{m6} = 2.2 \times 38.01 \times 10^{-6} \times (1pF / 220\ fF)$

$\Rightarrow g_{m6} = 380 \times 10^{-6}$

$S_6 = S_3 (g_{m6} / g_{m3})$

$g_{m3} = \sqrt{2 \times 77.84 \times 10^{-6} \times 5 \times 2.2 \times 10^{-6}}$

$g_{m3} = 41.4 \times 10^{-6}$

$\Rightarrow S_6 = 5 \times (380 / 41.4)$

$\Rightarrow S_6 = 46$

$\Rightarrow$ **$(W/L)_6 = 46$**

7.) $I_6 = (S_6/S_4)\ I_4 = (S_6/S_4) \times (I_5/2)$

$\Rightarrow I_6 = (46/5) \times 2.2 \times 10^{-6}$

$\Rightarrow I_6 = 20.24 \times 10^{-6}$

8.) $S_7 = (I_6/I_5)\ S_5$

$\Rightarrow S_7 = (20.24/4.4) \times 8$

$\Rightarrow S_7 = 37$

$\Rightarrow$ **$(W/L)_7 = 37$**

The (W/L) values of all the mosfets are as follows:

M1 and M2 : (W/L) = 1

M3 and M4 : (W/L) = 5

M5 : (W/L) = 8

M6 : (W/L) = 46

M7 : (W/L) = 37

Schematic of Op-amp

The schematic is now drawn using the Virtuoso schematic editor in Cadence. The values of the length and width have been calculated. This schematic is for a load of 1pF. The input pins are Vdd which is the positive supply voltage, Vss (ground) which is the negative supply voltage, Vini (the inverting input voltage), Vinn (the non-inverting input voltage) and Vbias (the biasing voltage – 0.5 V). Vout is the output of the op-amp. A supply voltage of 1.5 to -1.5 volts is given.

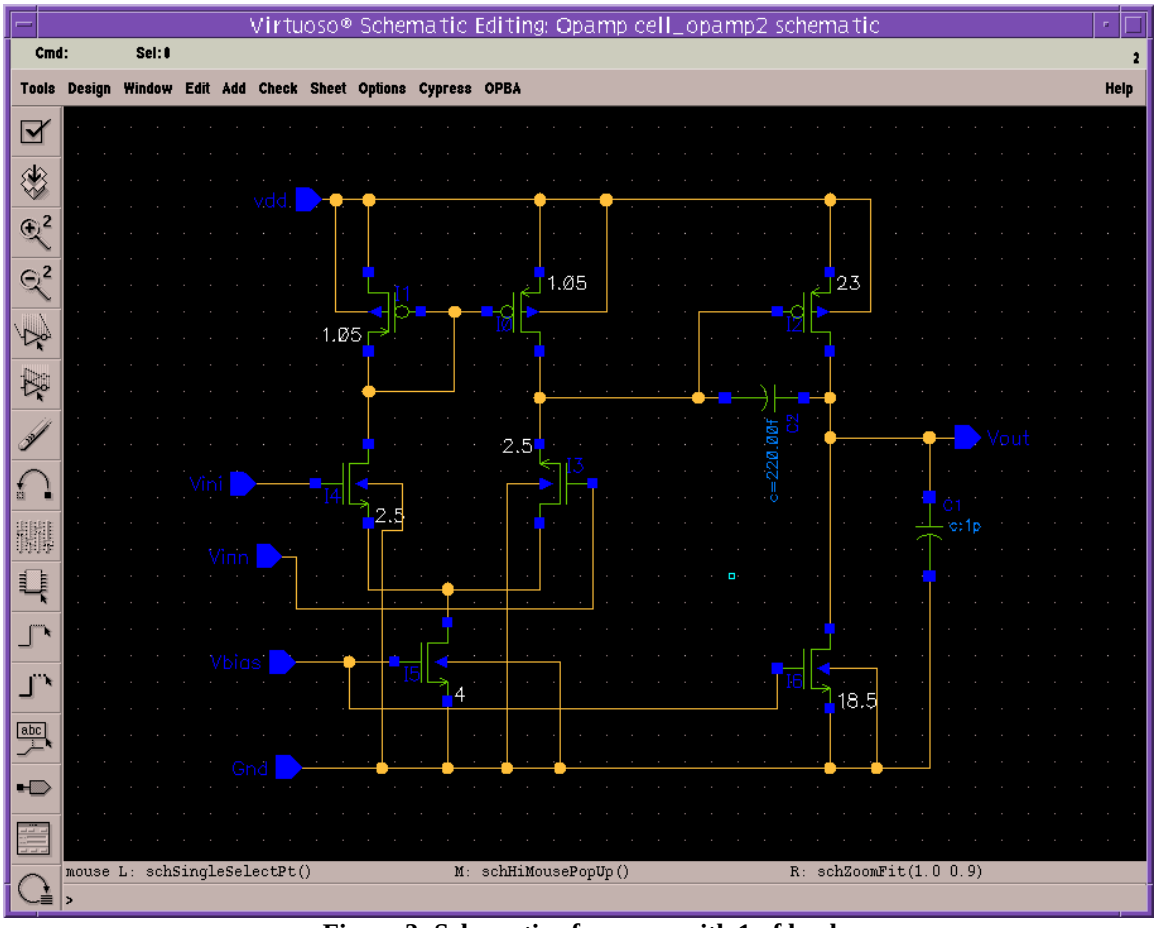


Figure 3: Schematic of op-amp with 1 pf load

Output of op-amp

The circuit is simulated for an inverting voltage of 500m. The non-inverting voltage is given as a pulse input. The values of the non-inverting voltage swing from 400mV to 600mV. The pulse width is 500ns and period is 1000ns. The rise time and fall time are both specified to be 60ns.

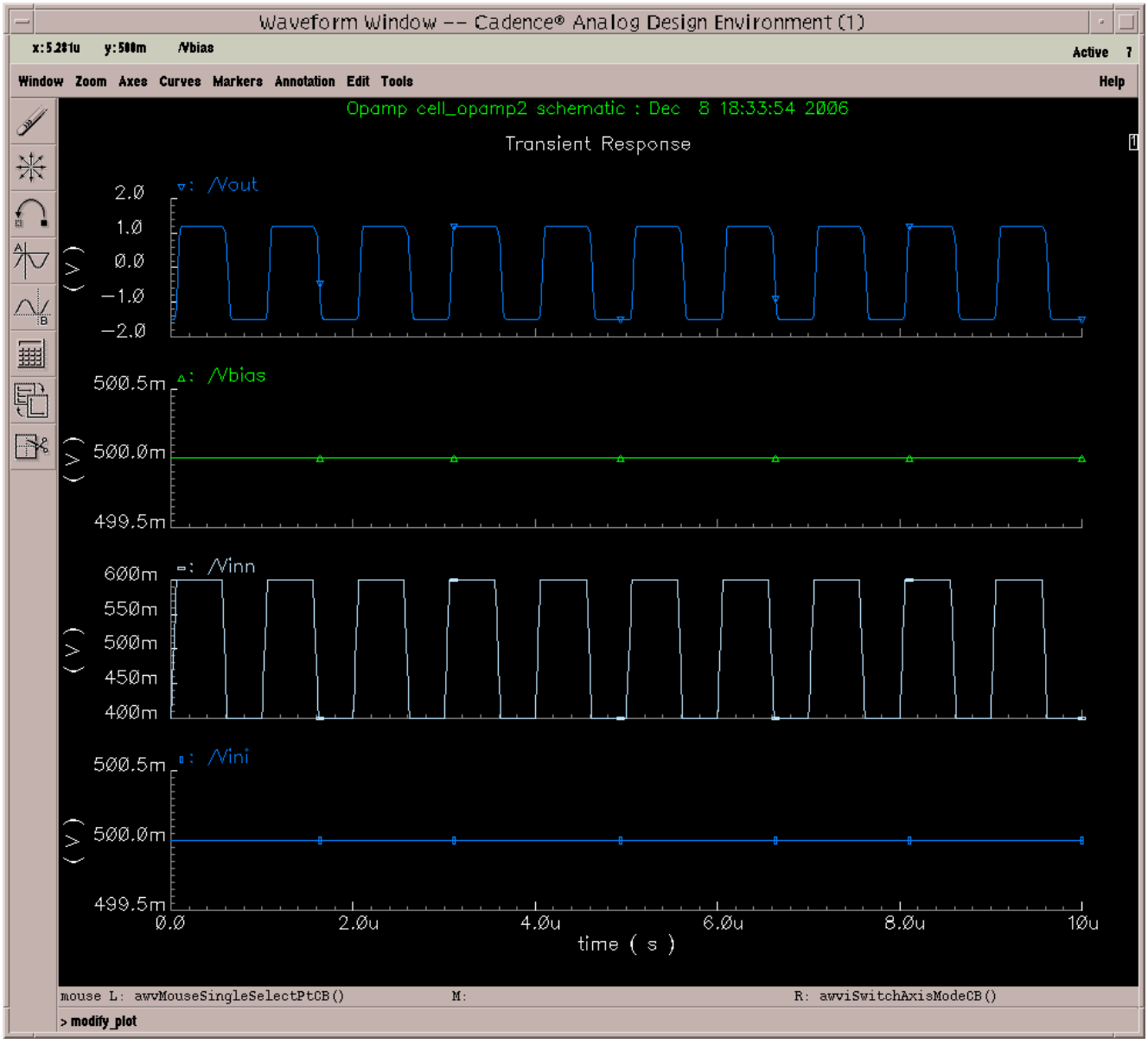


Figure 4: Simulation of op-amp with 1 pf load

Vout is the voltage of the op-amp. It is observed that when the inverting voltage is more than the non-inverting voltage, the output of the op-amp is negative and vice-versa.

Output Buffer

This op-amp has been designed for a load of 1pF. However, when the output of the op-amp is measured using an oscilloscope, it introduces a capacitive load of 20pF. A large capacitive load can significantly increase the delay in a circuit. The op-amp that has been designed cannot drive this load satisfactorily. In order to minimize this delay we use a buffer circuit (a string of inverters)

In order to calculate an ideal number of stages we use the formula:

The number of stages (N) $N=\ln (C_L / C_{in})$

Where C_L is the load capacitance and C_{in} is the input capacitance at the first inverter in the buffer circuit. The width of the mosfets in each inverter stage is made 'A' times the previous inverter stages' width. The channel length is kept constant. By making the width wider by a factor 'A' the resistance decreases by a factor 'A' and capacitance increases by a factor 'A'.

The output capacitance of the op-amp is $\cong$ 220fF and this becomes the input capacitance of the buffer circuit. The value of the output capacitance is 20pF. The ideal number of output stages is calculated as being 5. However, with an odd number of stages, the output will be an inverse of the input and so another stage is added.

The width of NMOS in the inverter for various stages are : 1.05 for first stage, 2.718 for second stage, 7.34 for third stage, 19.9 for fourth stage, 54.08 for fifth and sixth stages. The width of PMOS is double the value of NMOS. The output of the buffer will now swing between -1.5 to 1.5 volts depending on the value of the input (output of the op-amp).

Schematic of Op-amp with buffer

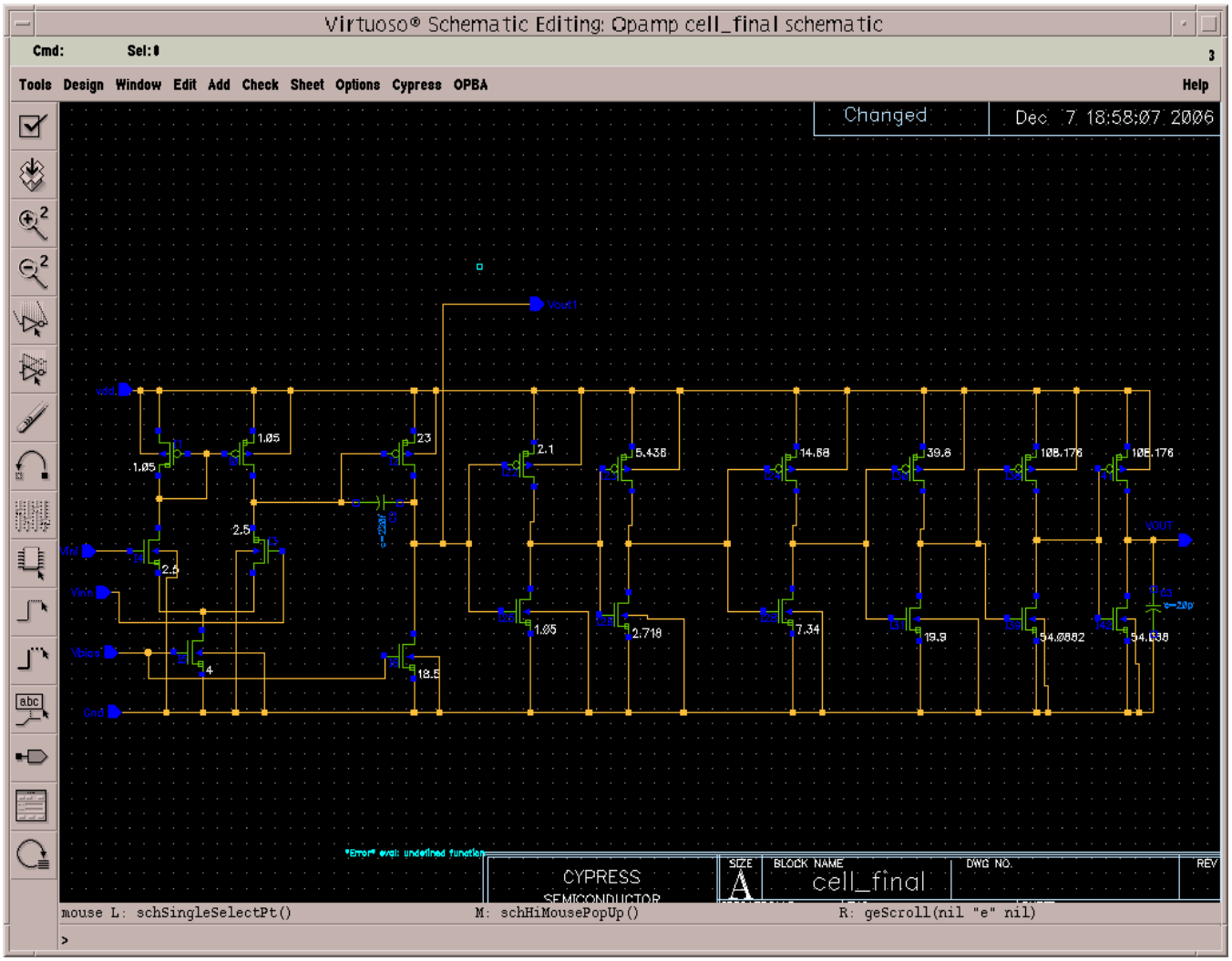


Figure 5: Schematic of op-amp with output buffer driving an output load of 20 pf.

Simulation:

The output of the circuit with a load of 20 pF is shown below. In these graphs the output of the op-amp and the output of the buffer are seen.

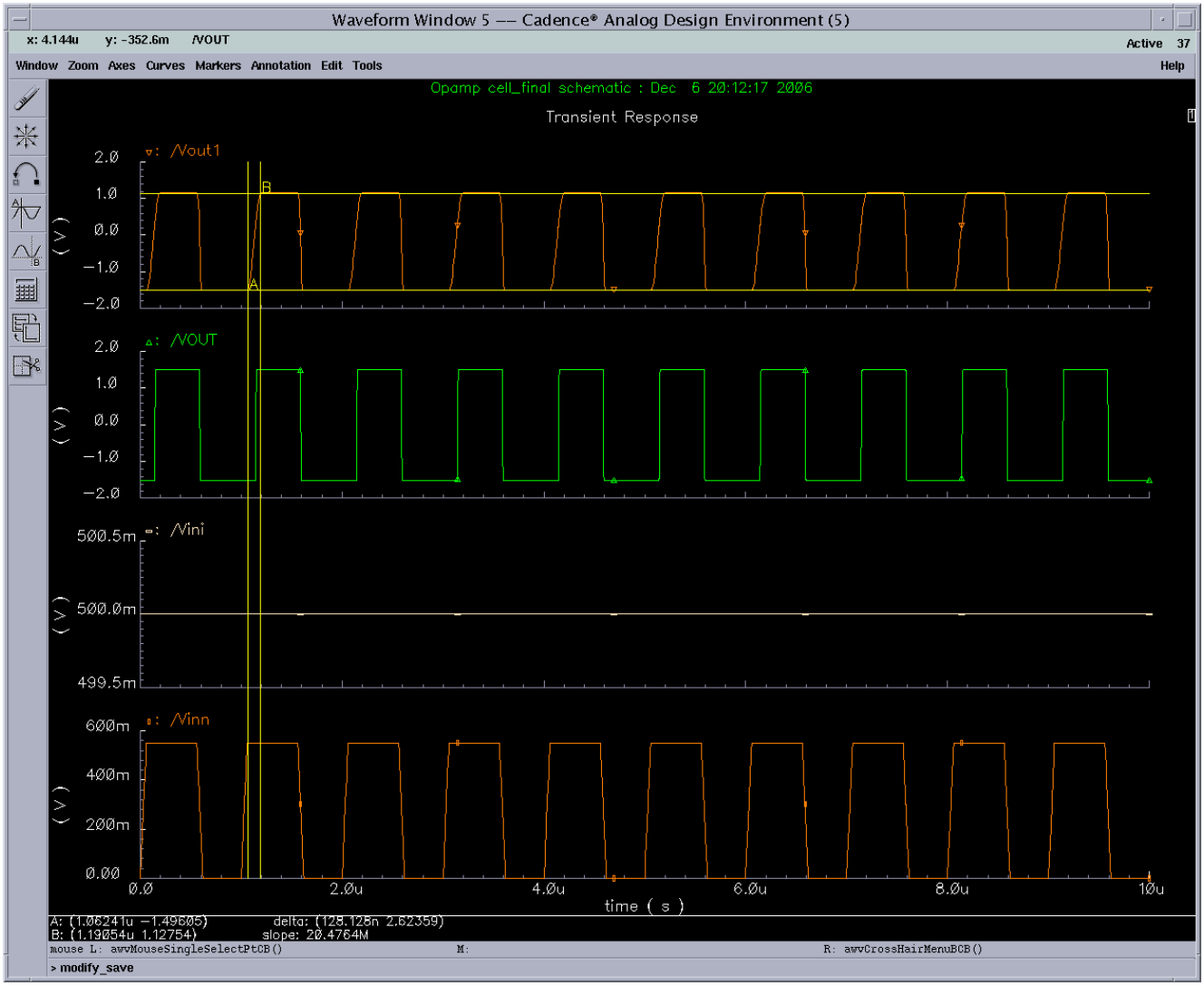


Figure 6: Output of the op-amp with load of 20 pf

The output of the op-amp is Vout1. The output of the buffer is VOUT. The slew rate of the op-amp, which is the slope of the output voltage curve; is observed to be 20.476 MV/ sec.

The Gain of the Op-amp

The circuit is now simulated with an inverting voltage of 1.4V and a non inverting voltage of 1.40005 volts. This means that the difference of non-inverting and inverting voltage is 5×10^{-5} V. The output of the op-amp is (Vout1). So, the gain of the op-amp is [(5×10^{-5}) / Vout1] V/V.

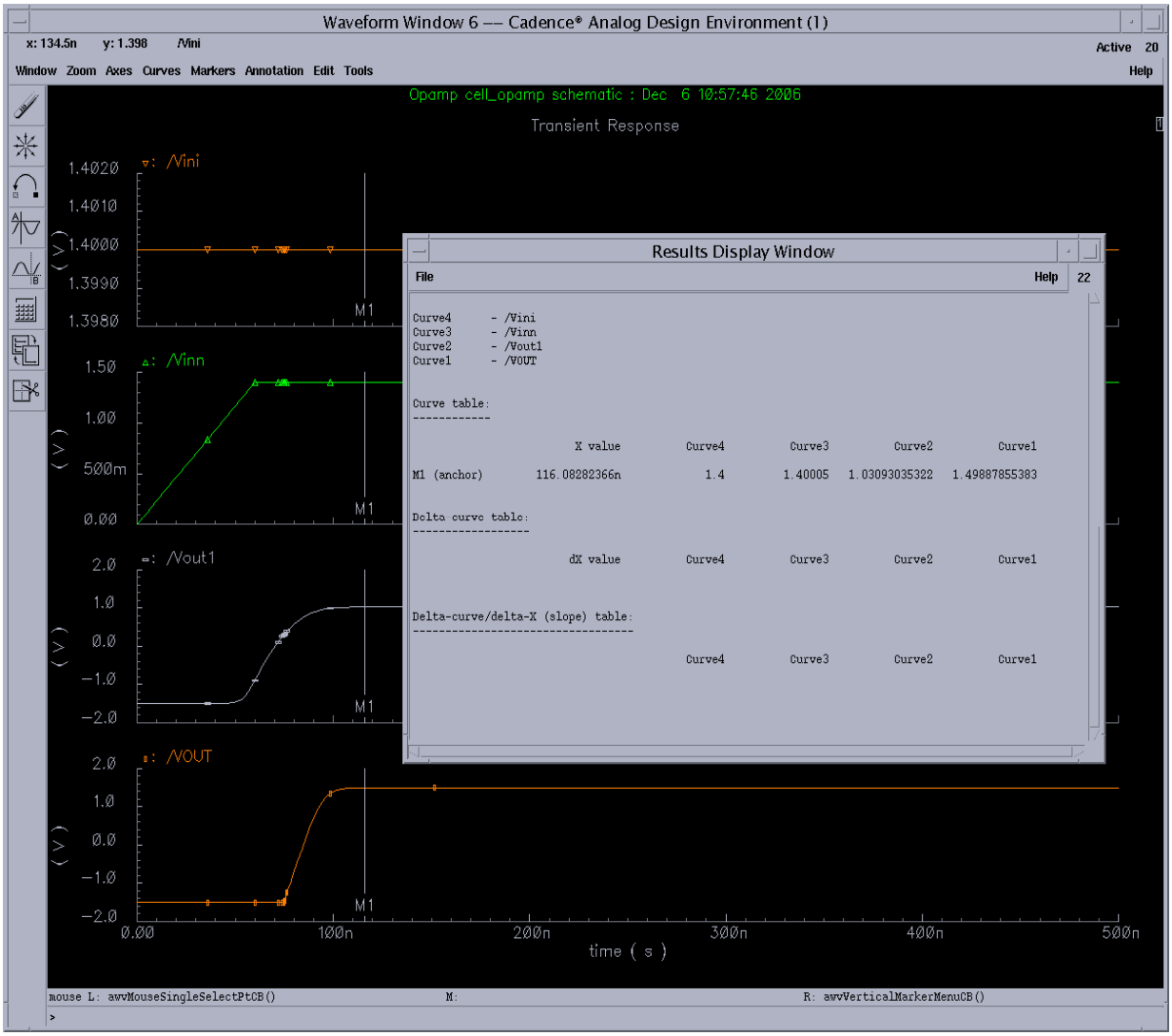


Figure 7: The gain of op-amp is observed from the waveform.

Here, the value of the op-amp Vout1 (curve 2) is 1.0309 volts. So, the gain of the op-amp is 20,600 V/V. Notice that the output of the inverter is 1.5 volts and this value depends on the value of the positive input voltage.

Variation in the gain of Op-amp with different W and L values

Variation in gain with variation in the length L2

The circuit is simulated with different values of L2 (length of channel M2) and the change in the gain of the op-amp is observed.

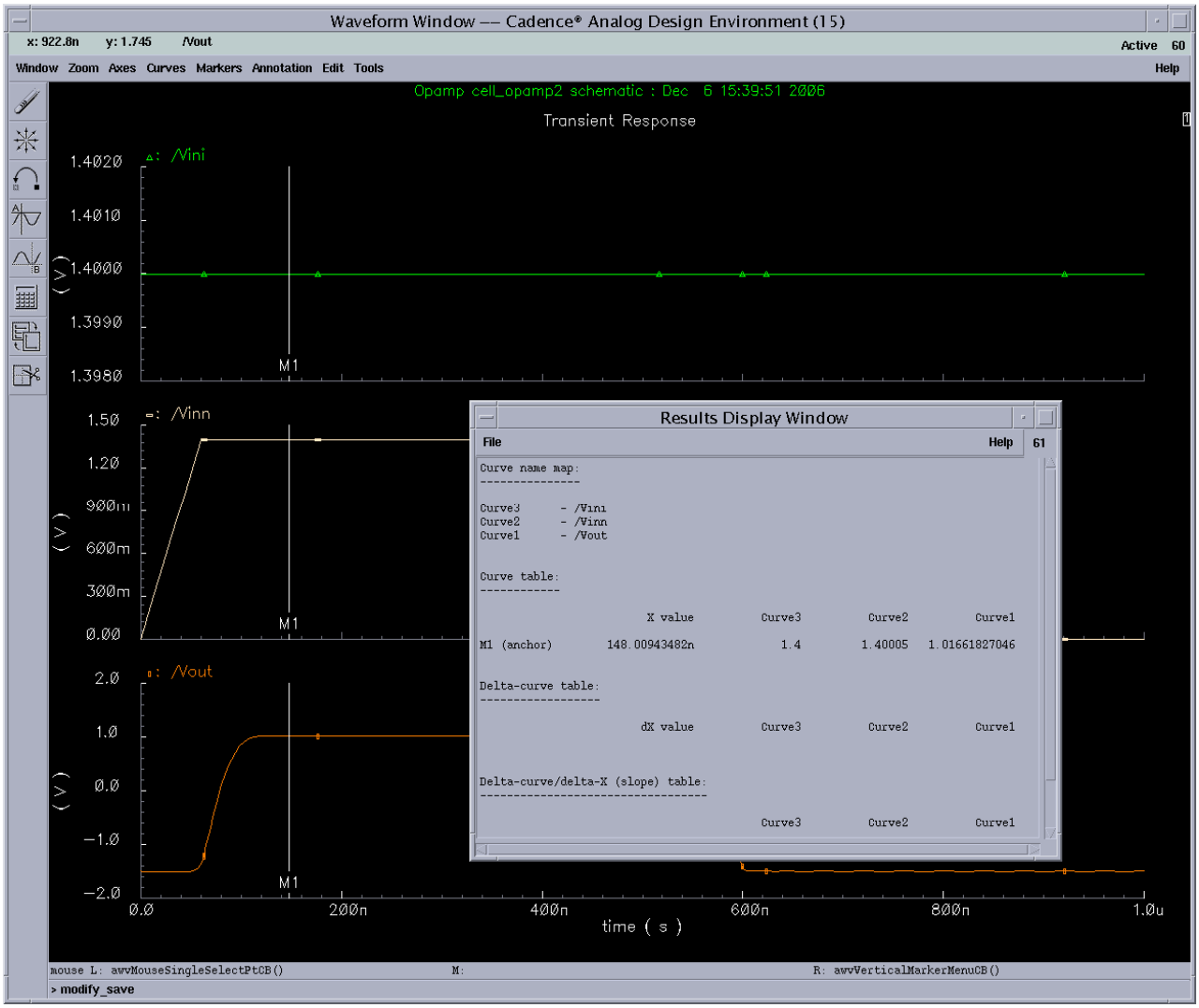


Figure 8: Gain of op-amp with L2=0.75.

The value of L2 here is 0.75.

Here, the value of the op-amp Vout (curve) is 1.0166 volts. So, the gain of the op-amp is 20,300 V/V

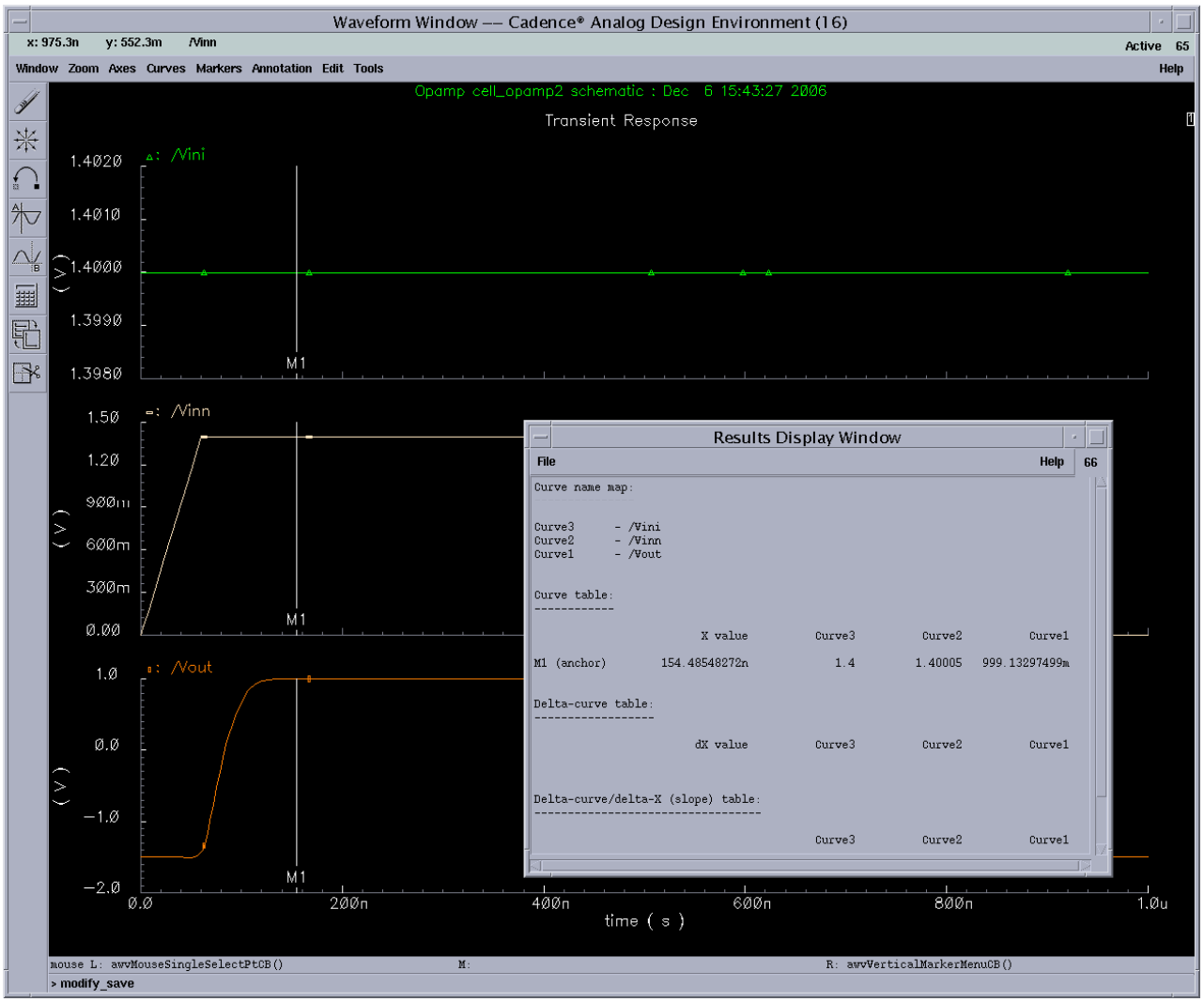


Figure 9: Gain of op-amp with L2=1.00.

The value of L2 here is 1.00.

Here, the value of the op-amp Vout (curve) is 999m volts. So, the gain of the op-amp is 19,950 V/V

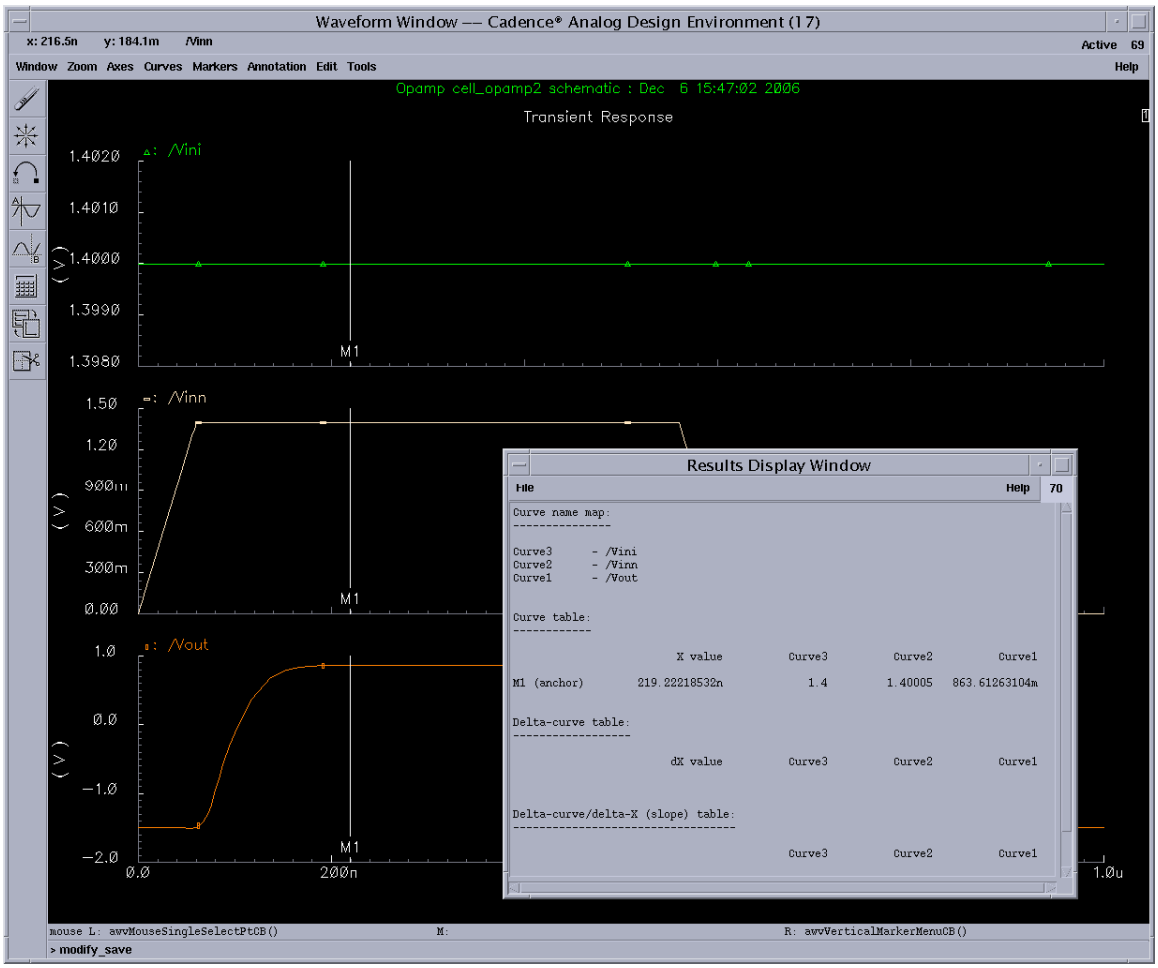


Figure 10: Gain of the op-amp with L2=2.00.

The value of L2 here is 2.00.

Here, the value of the op-amp Vout (curve) is 863m volts. So, the gain of the op-amp is 17,250 V/V

We observe that the value of gain is decreasing with an increase in L2.

Variation in gain with variation in the length L3

The circuit is simulated with different values of L3 (length of M3) and the change in the gain of the op-amp is observed.

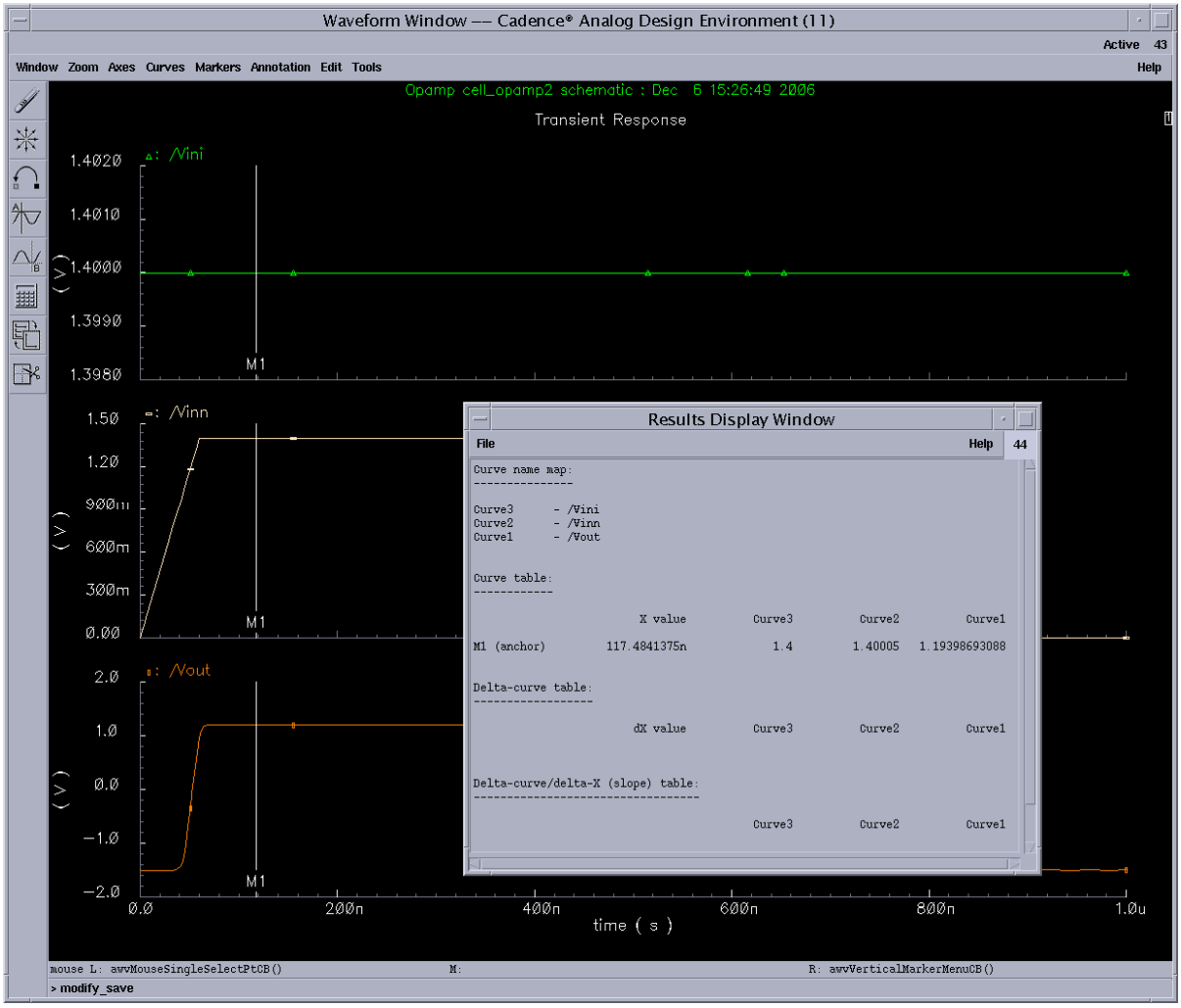


Figure 11: Gain of the op-amp with L3=0.75.

The value of L3 here is 0.75.

Here, the value of the op-amp Vout (curve 1) is 1.193 volts. So, the gain of the op-amp is 23,860 V/V

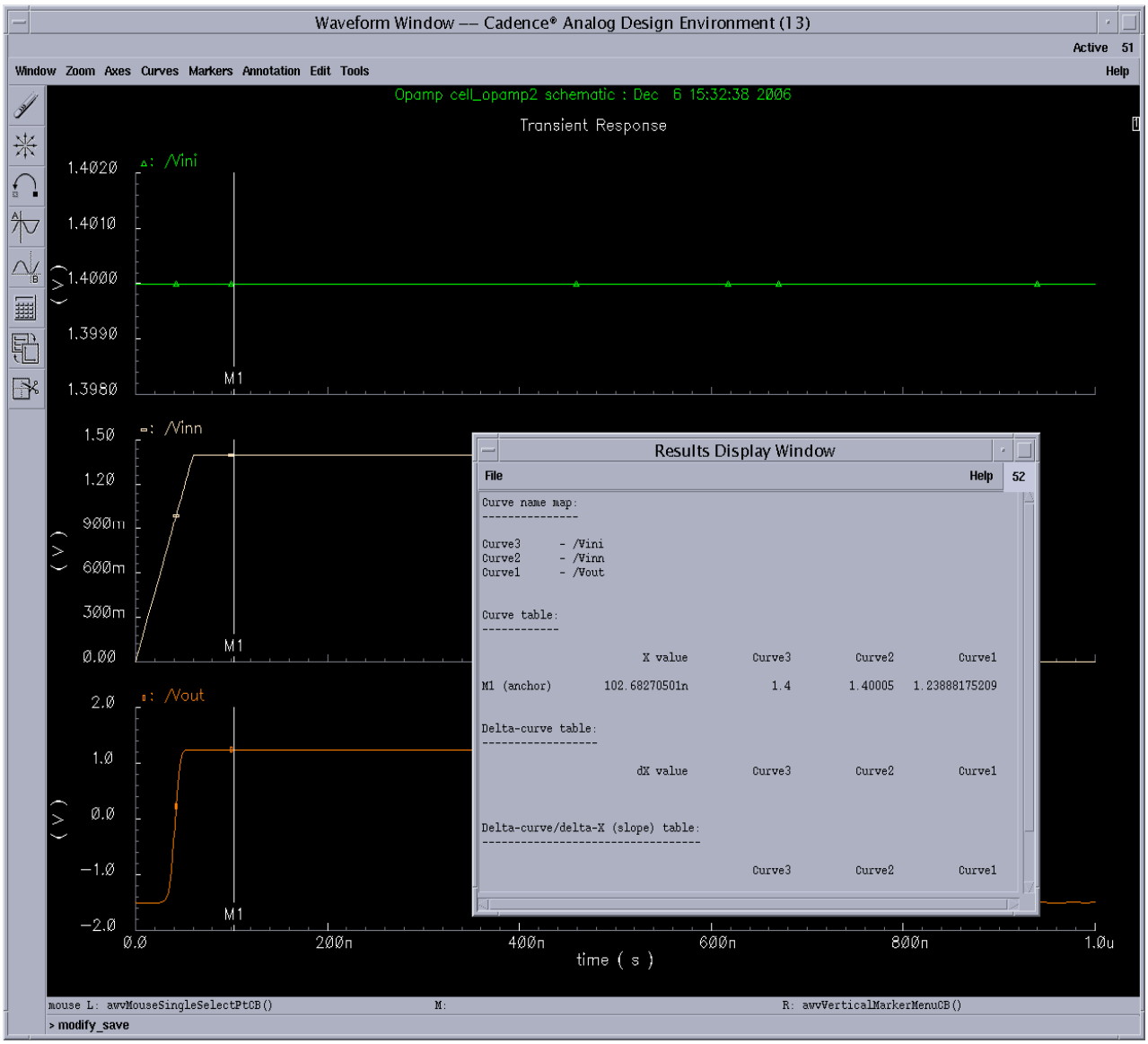


Figure 12: Gain of the op-amp with L3=1.50.

The value of L3 here is 1.50.

Here, the value of the op-amp Vout (curve 1) is 1.238 volts. So, the gain of the op-amp is 24,760 V/V

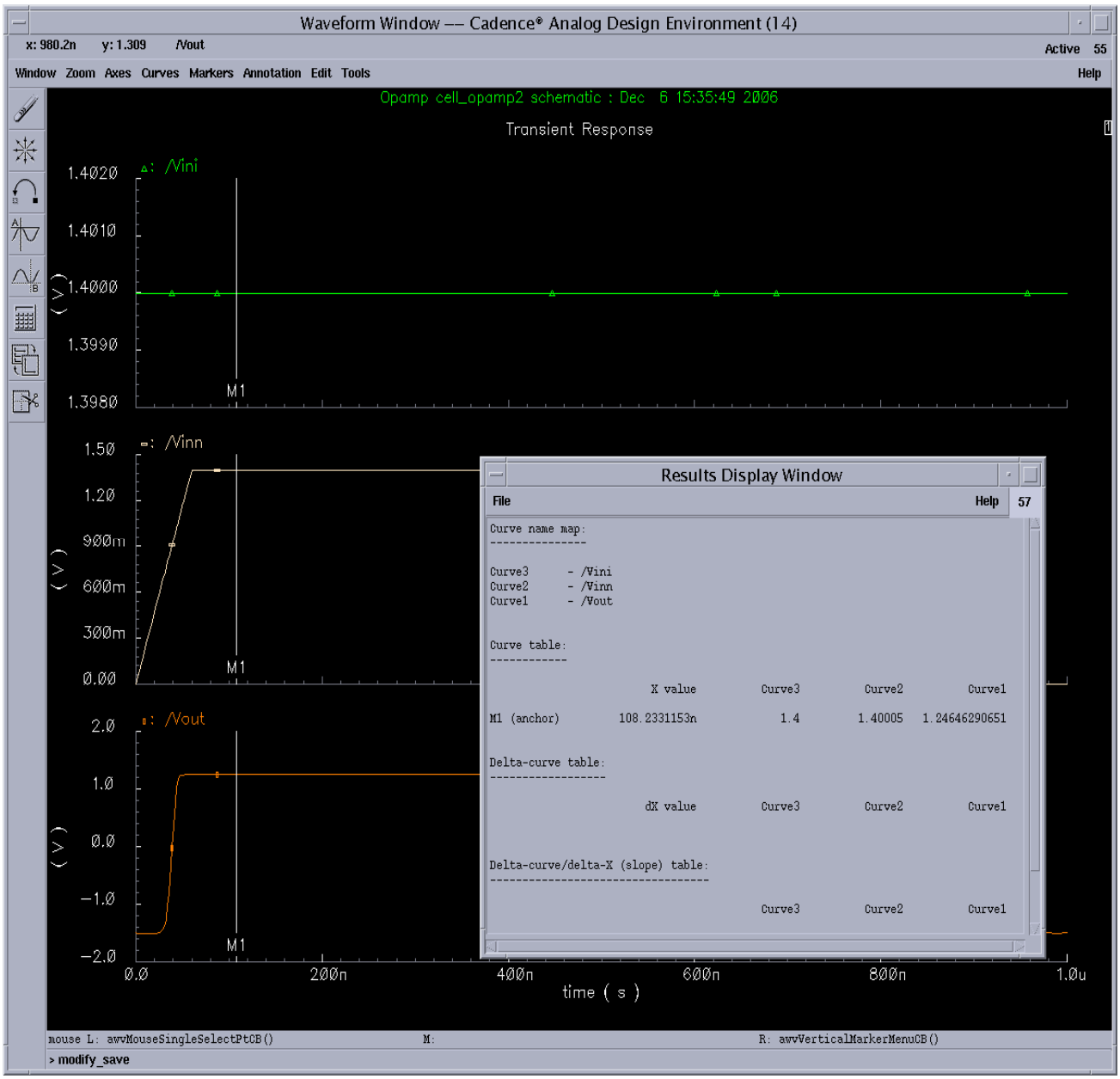


Figure 13: Gain of the op-amp with L3=2.00.

The value of L3 here is 2.00.

Here, the value of the op-amp Vout (curve 1) is 1.246 volts. So, the gain of the op-amp is 24,950 V/V

We observe that the value of gain is increasing with an increase in L3.

Variation in gain with variation in the length L7

The circuit is simulated with different values of L7 (length of channel M7) and the change in the gain of the op-amp is observed.

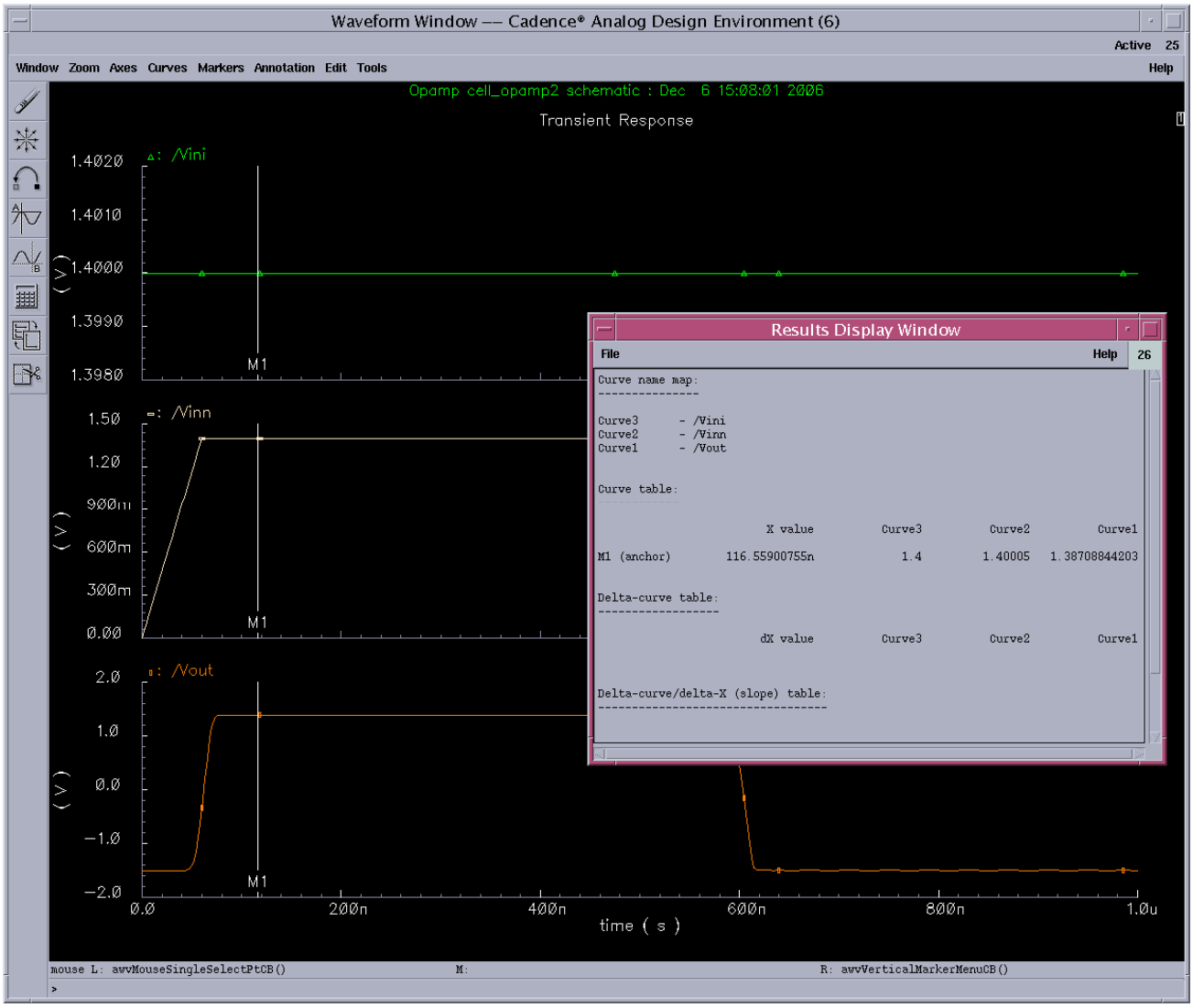


Figure 14: Gain of the op-amp with L7=1.00.

The value of L7 here is 1.00.

Here, the value of the op-amp Vout (curve 1) is 1.387 volts. So, the gain of the op-amp is 27,740 V/V

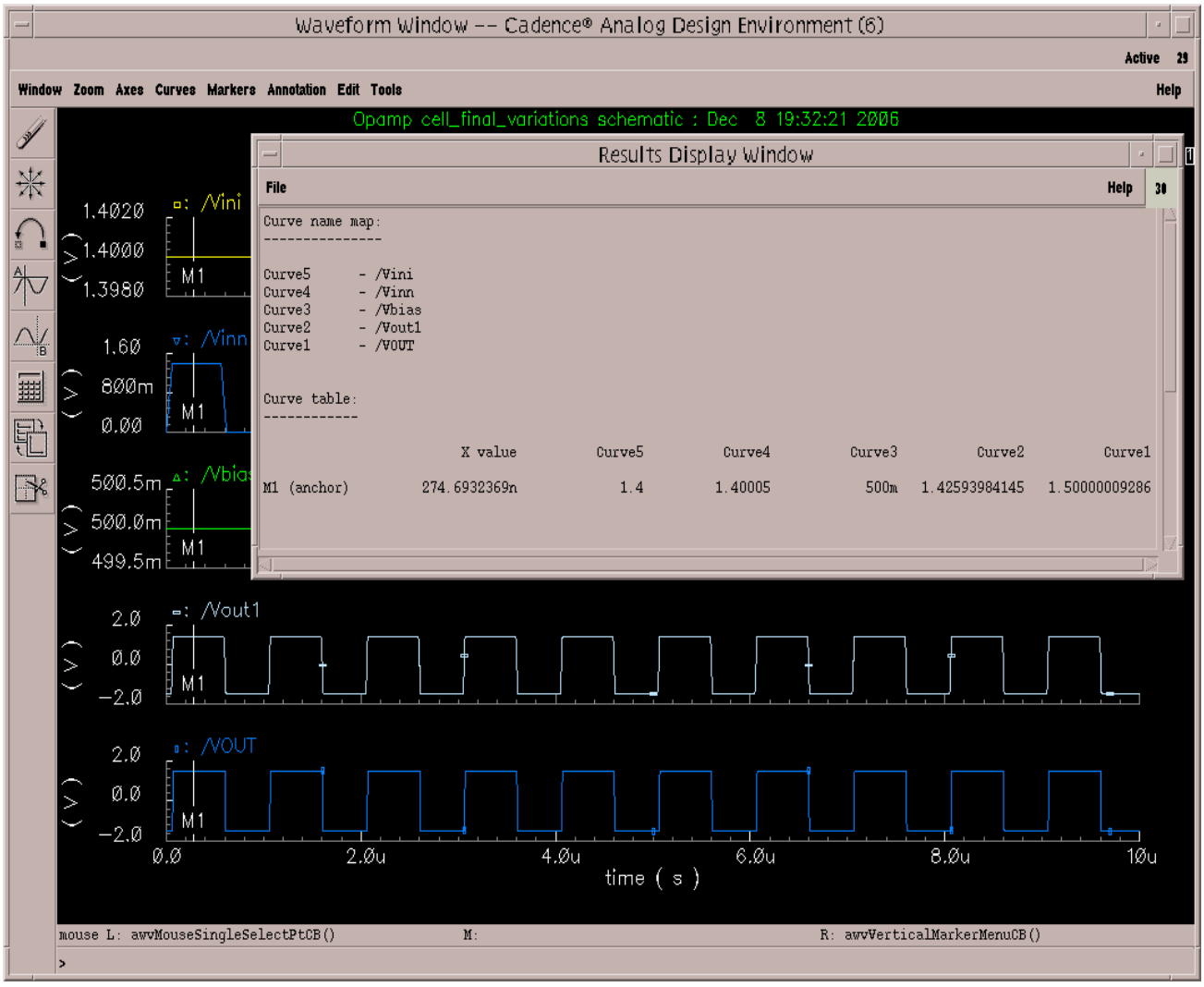


Figure 15: Gain of the op-amp with L7=1.50.

The value of L7 here is 1.50.

Here, the value of the op-amp Vout (curve 2) is 1.4259 volts. So, the gain of the op-amp is 28,520 V/V

It can be seen in the graphs that the output of the buffer (VOUT) swings from 1.5V to -1.5V.

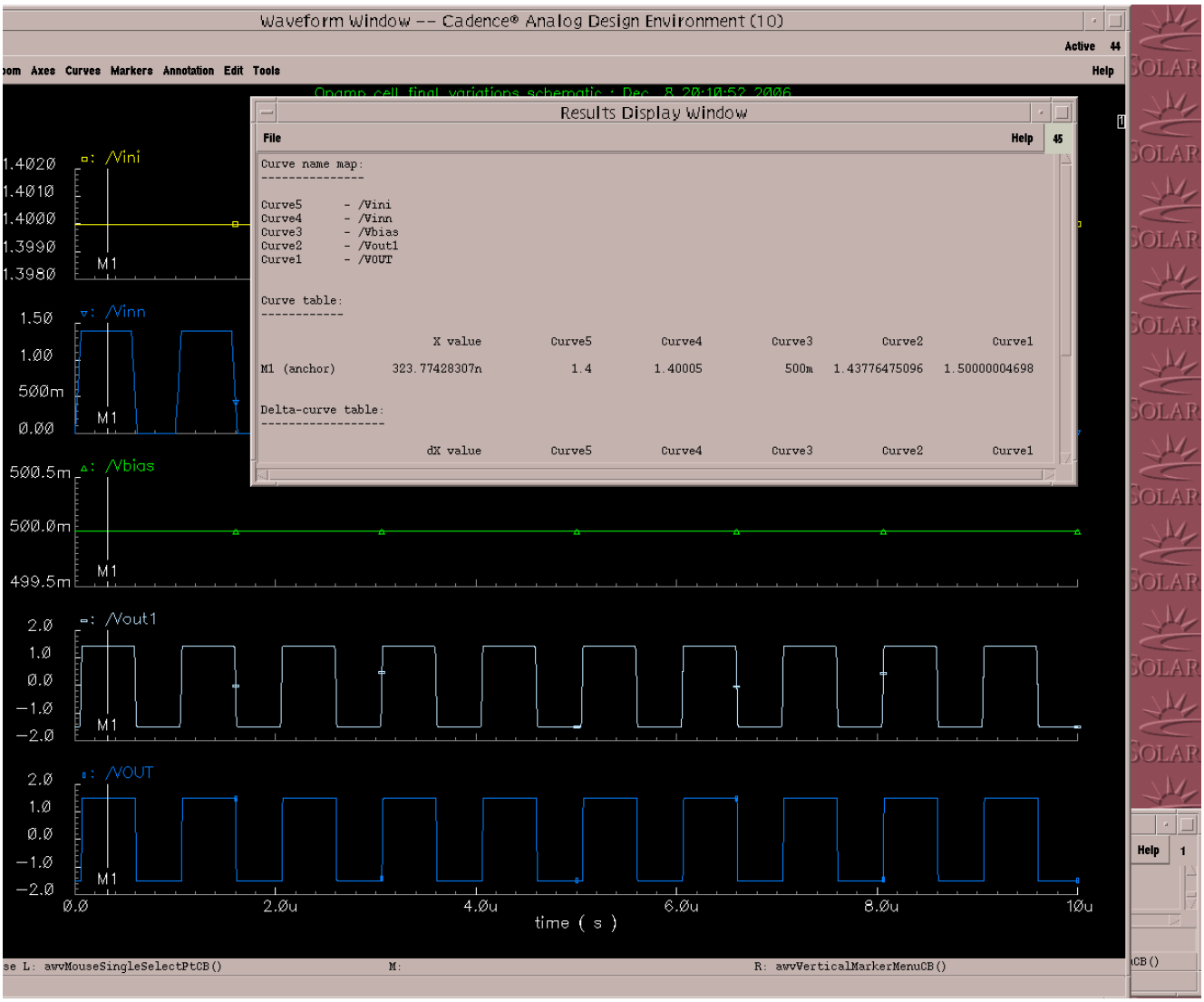


Figure 16: Gain of the op-amp with L7=2.00.

The value of L7 here is 2.00.

Here, the value of the op-amp Vout (curve 2) is 1.437 volts. So, the gain of the op-amp is 28,740 V/V

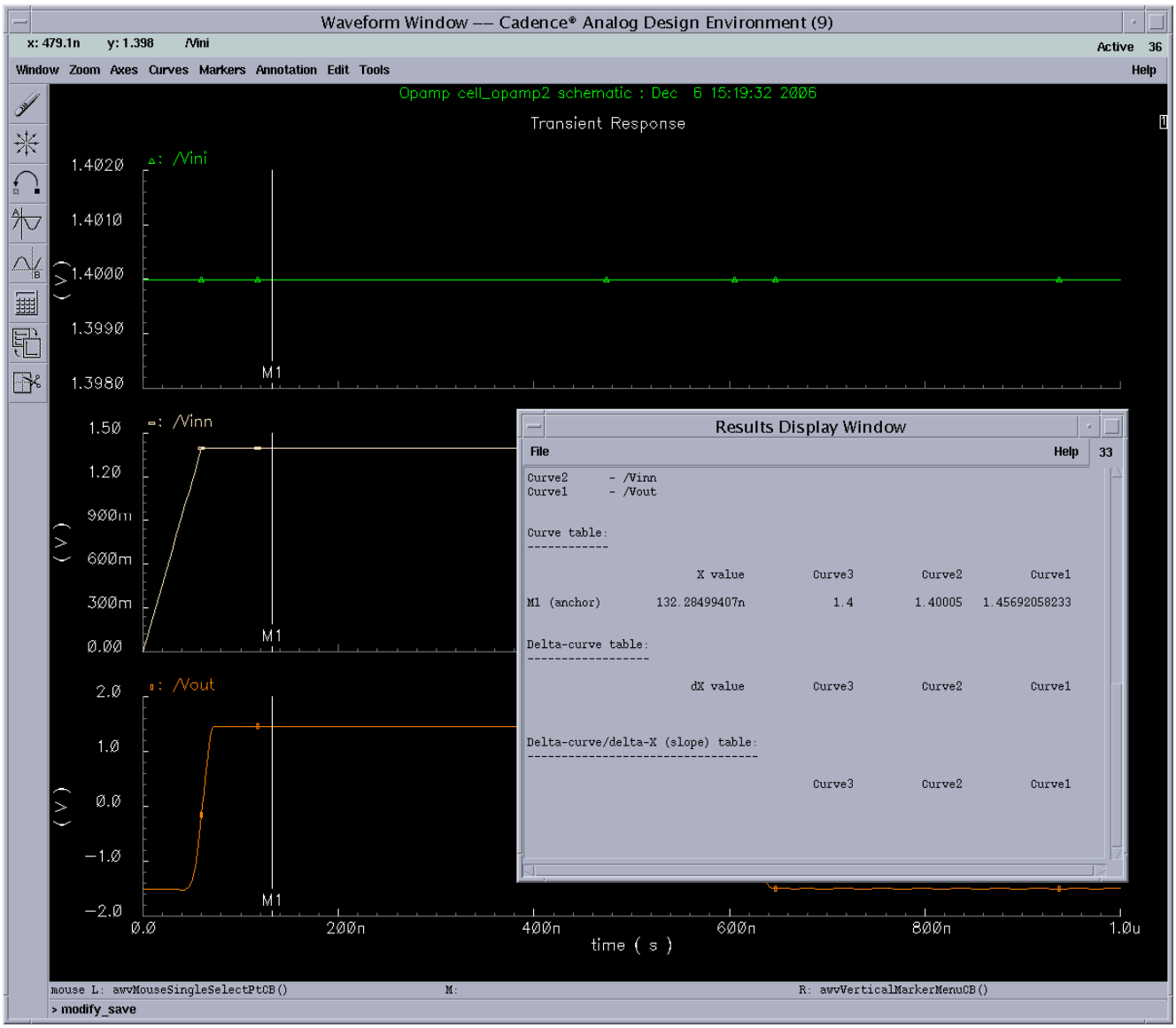


Figure 17: Gain of the op-amp with L7=3.00.

The value of L7 here is 3.00.

Here, the value of the op-amp Vout (curve 1) is 1.4569 volts. So, the gain of the op-amp is 29,140 V/V

We observe that the value of gain is increasing with an increase in L7

Variation in gain with variation in the width W6

The circuit is simulated with different values of W6 (width of channel of M6) and the change in the gain of the op-amp is observed.

Figure 18: Gain of the op-amp with W7=17.

The value of W6 here is 17.

Here, the value of the op-amp Vout (curve 2) is 372m volts. So, the gain of the op-amp is 7440 V/V

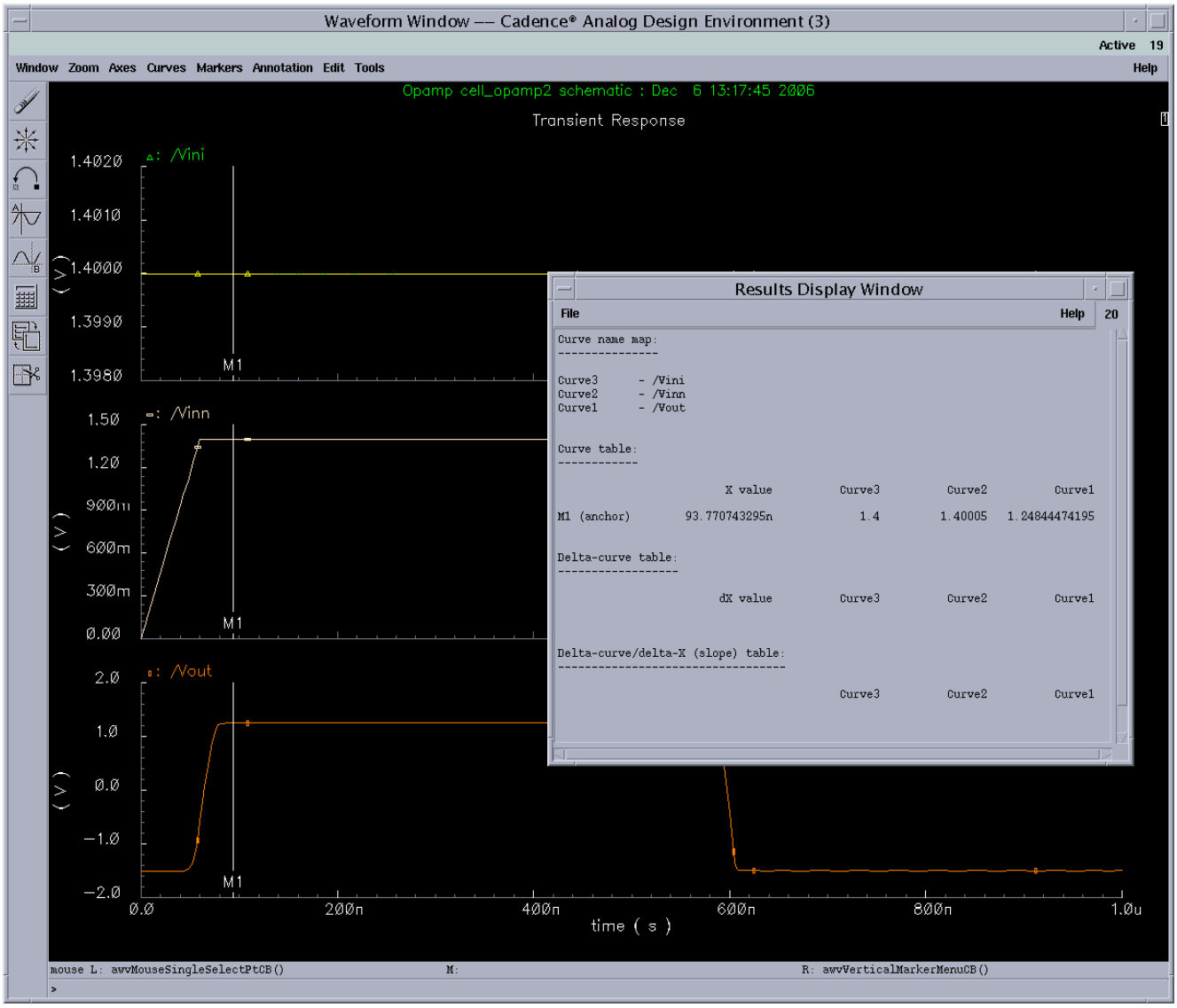


Figure 19: Gain of the op-amp with W7=34.

The value of W6 here is 34.

Here, the value of the op-amp Vout (curve 1) is 1.248 volts. So, the gain of the op-amp is 24,960 V/V

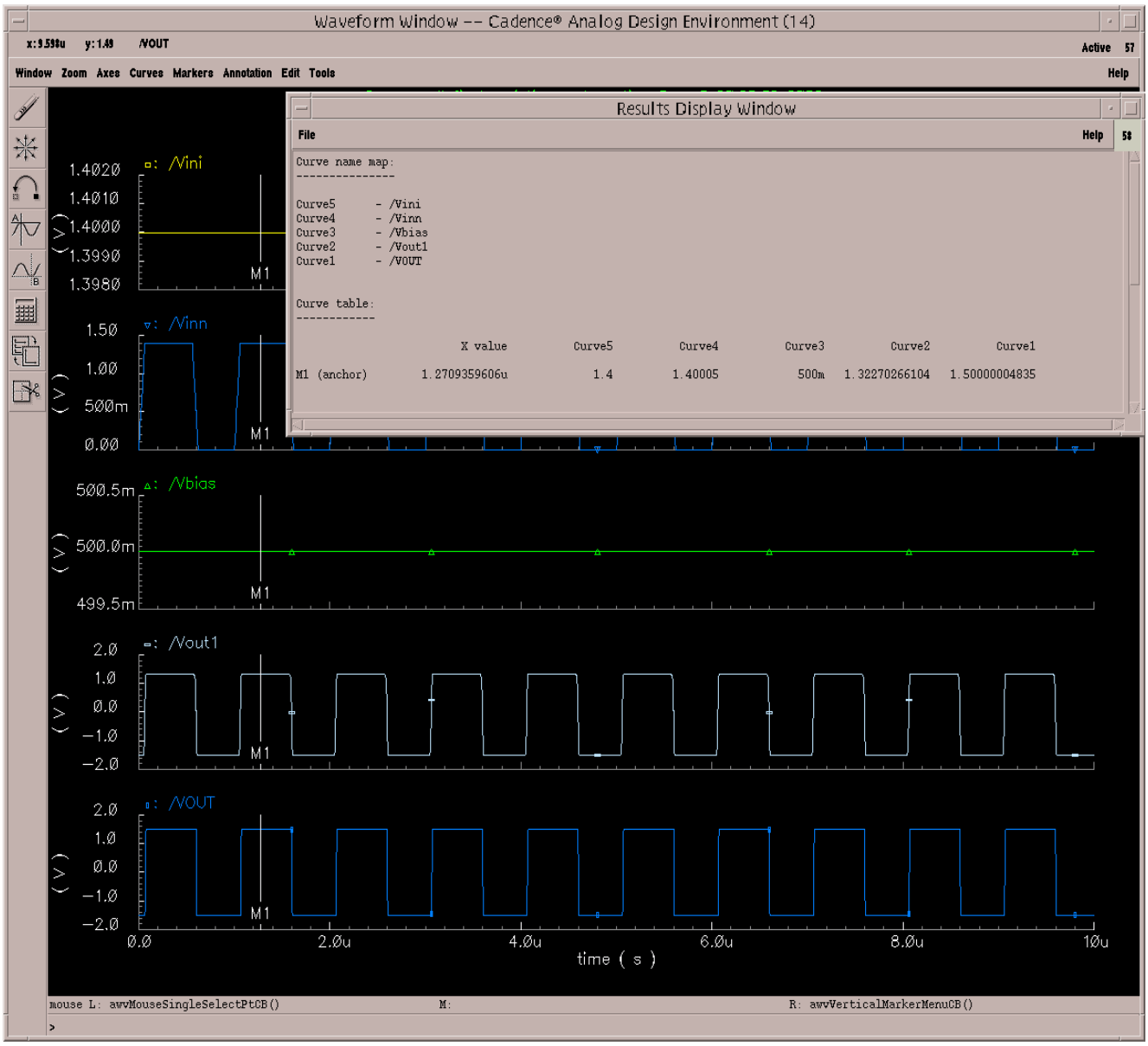


Figure 20: Gain of the op-amp with W6=45.

The value of W6 here is 45.

Here, the value of the op-amp Vout (curve 2) is 1.322 volts. So, the gain of the op-amp is 26,440 V/V

The output of the buffer swings from 1.5 to -1.5 volts depending on the output of the buffer.

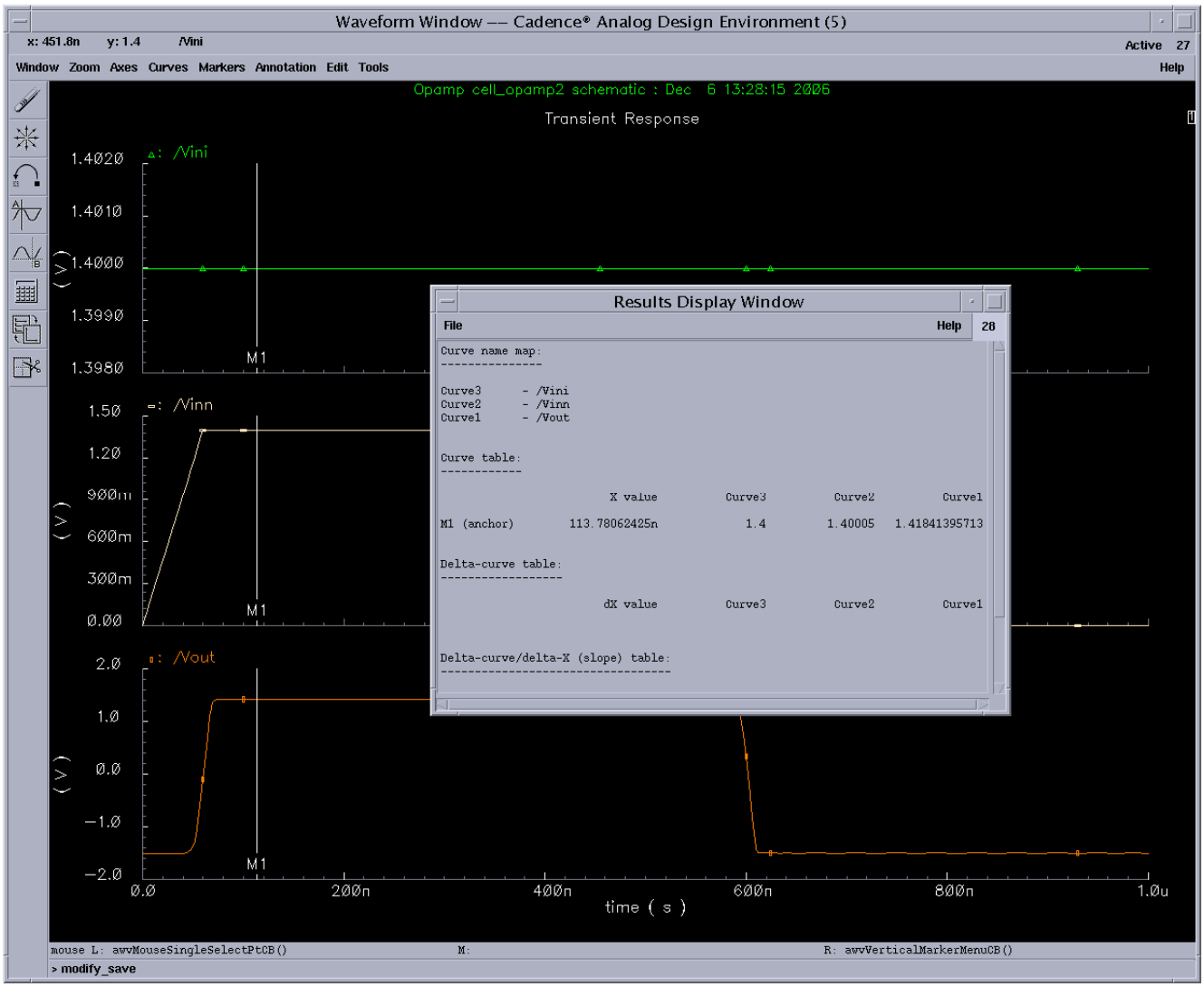


Figure 21: Gain of the op-amp with W6=90.

The value of W6 here is 90.

Here, the value of the op-amp Vout (curve 1) is 1.418 volts. So, the gain of the op-amp is 28,360 V/V

We observe that the value of gain is increasing with an increase in W6.

The Slew-Rate of the Op-amp

The slew rate (SR) is defined as the maximum rate of change of the output of an op amp circuit. The circuit is now simulated with an inverting voltage of 0.5V and a non-inverting voltage of 0.55 volts. The slope of the output curve is observed and the slew-rate is thus obtained.

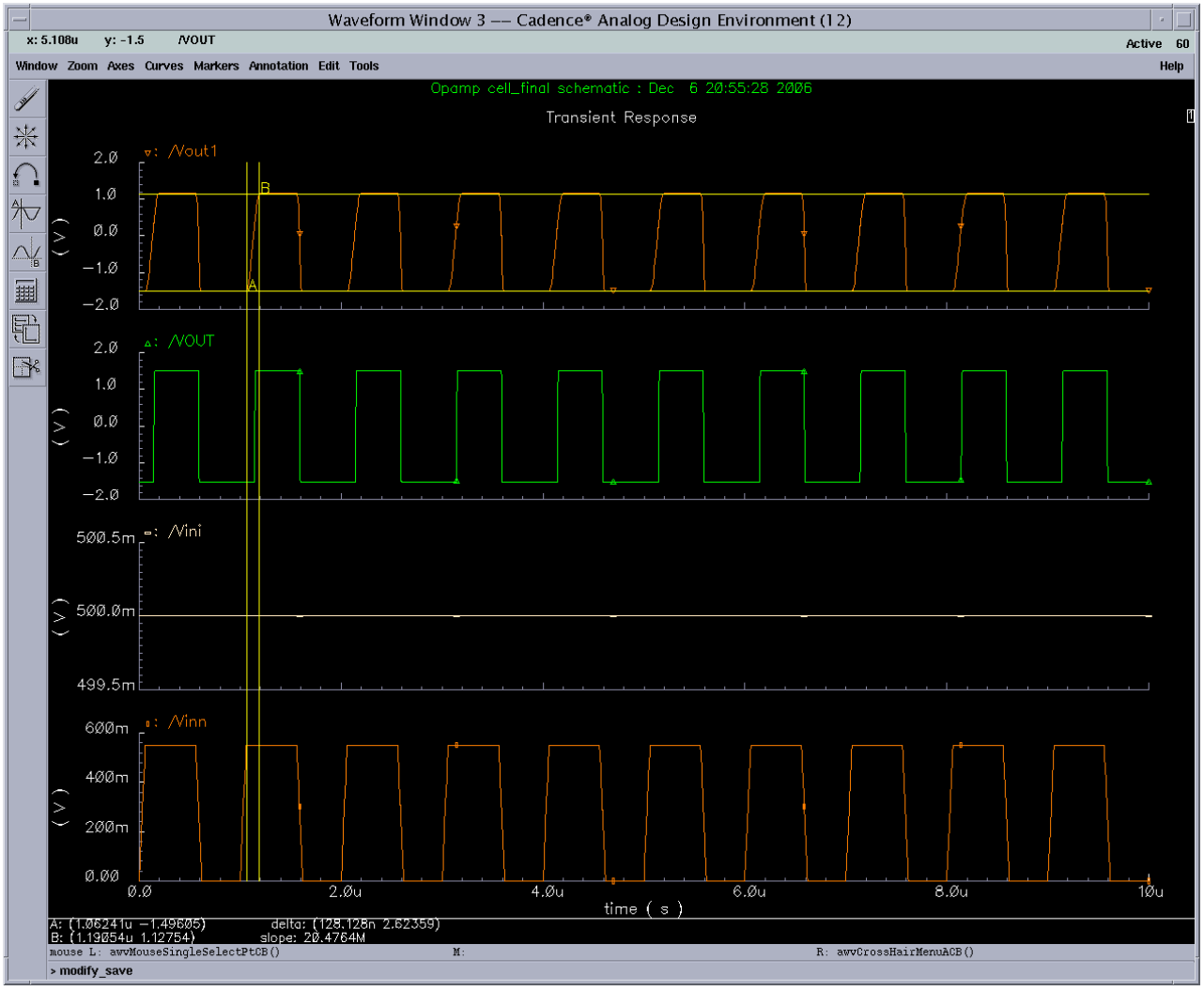


Figure 22: Slew rate of the op-amp is observed.

The output of the op-amp is the curve Vout1. The slope of the curve is 20.476M. Thus the slew rate of the of-amp is 20.476 MV / sec.

Variation in the slew rate of Op-amp with different Cc values

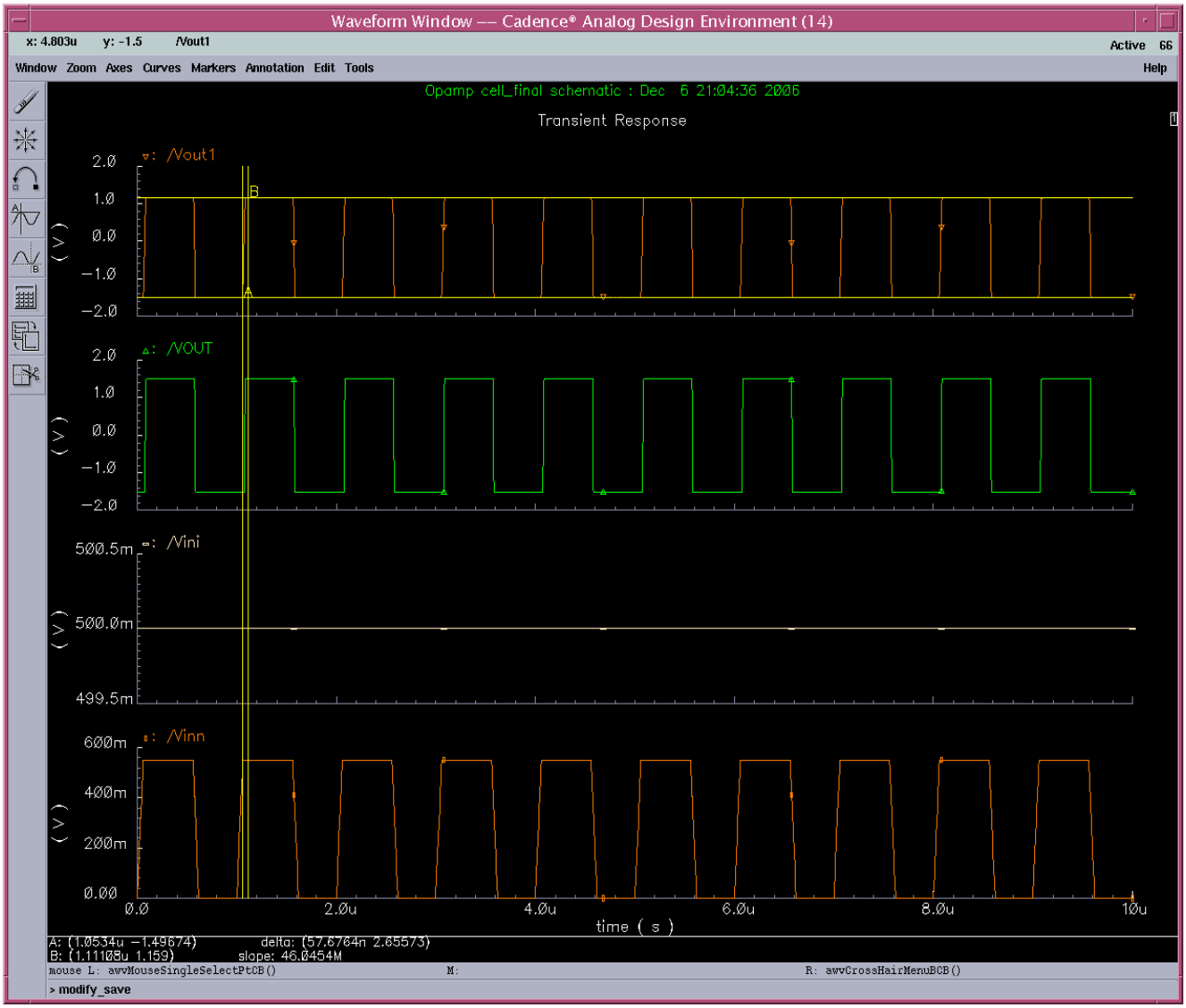


Figure 23: Slew rate with Cc=50fF.

The output of the op-amp is the curve Vout1. The compensation capacitance Cc here is 50fF. The slew rate of the of-amp is 46.045 MV / sec.

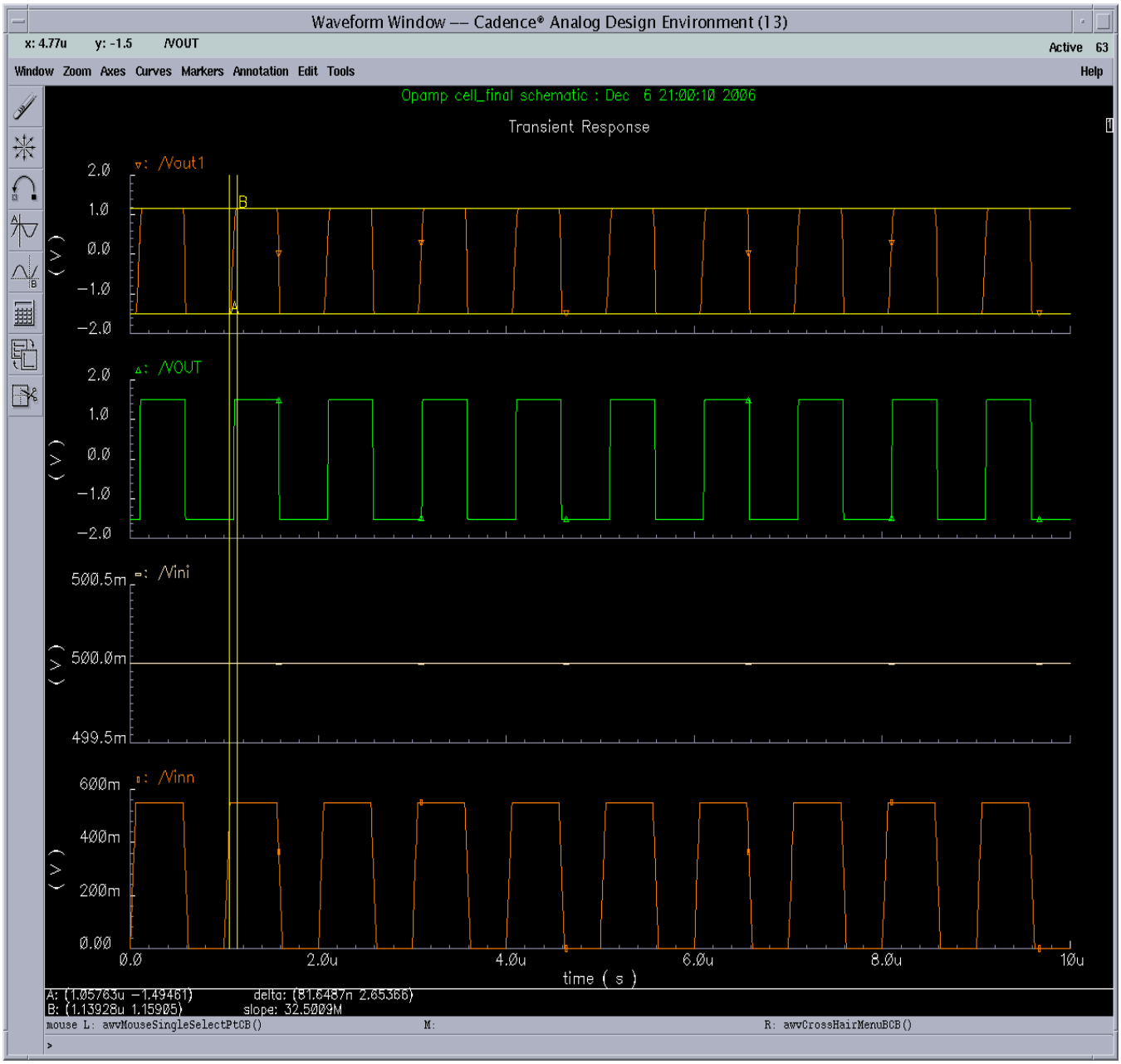


Figure 24: Slew rate with Cc=110fF.

The output of the op-amp is the curve Vout1. The compensation capacitance Cc here is 110fF. The slew rate of the of-amp is 32.5209 MV / sec

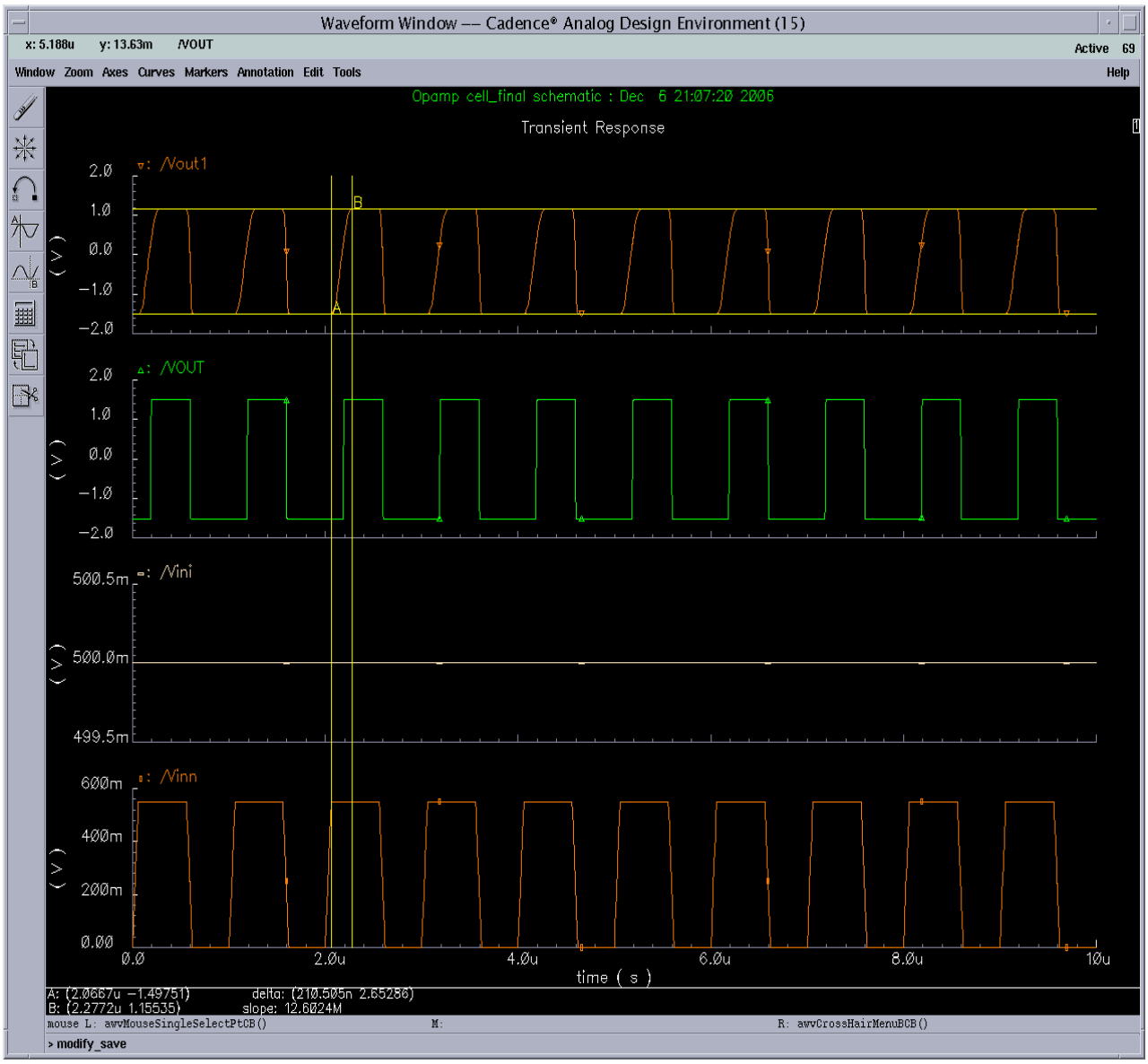


Figure 25: Slew rate with Cc=330fF.

The output of the op-amp is the curve Vout1. The compensation capacitance Cc here is 330fF. The slew rate of the of-amp is 12.602 MV / sec

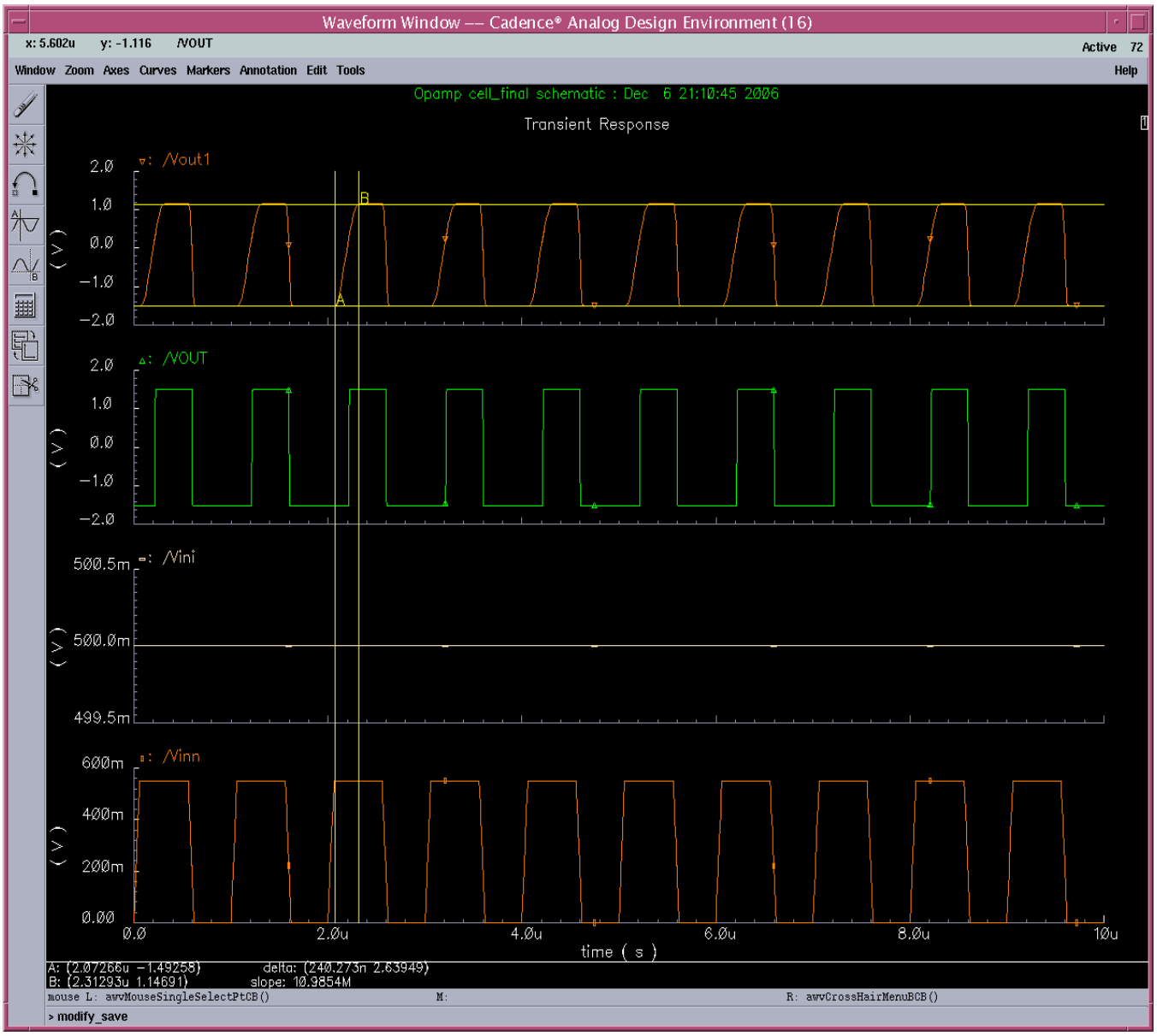


Figure 26: Slew rate with Cc=400fF.

The output of the op-amp is the curve Vout1. The compensation capacitance Cc here is 400fF. The slew rate of the of-amp is 10.985 MV / sec

We observe that the value of slew-rate is increasing with an increase in Cc.

Layout of the Op-amp

The layout of the op-amp is shown below:

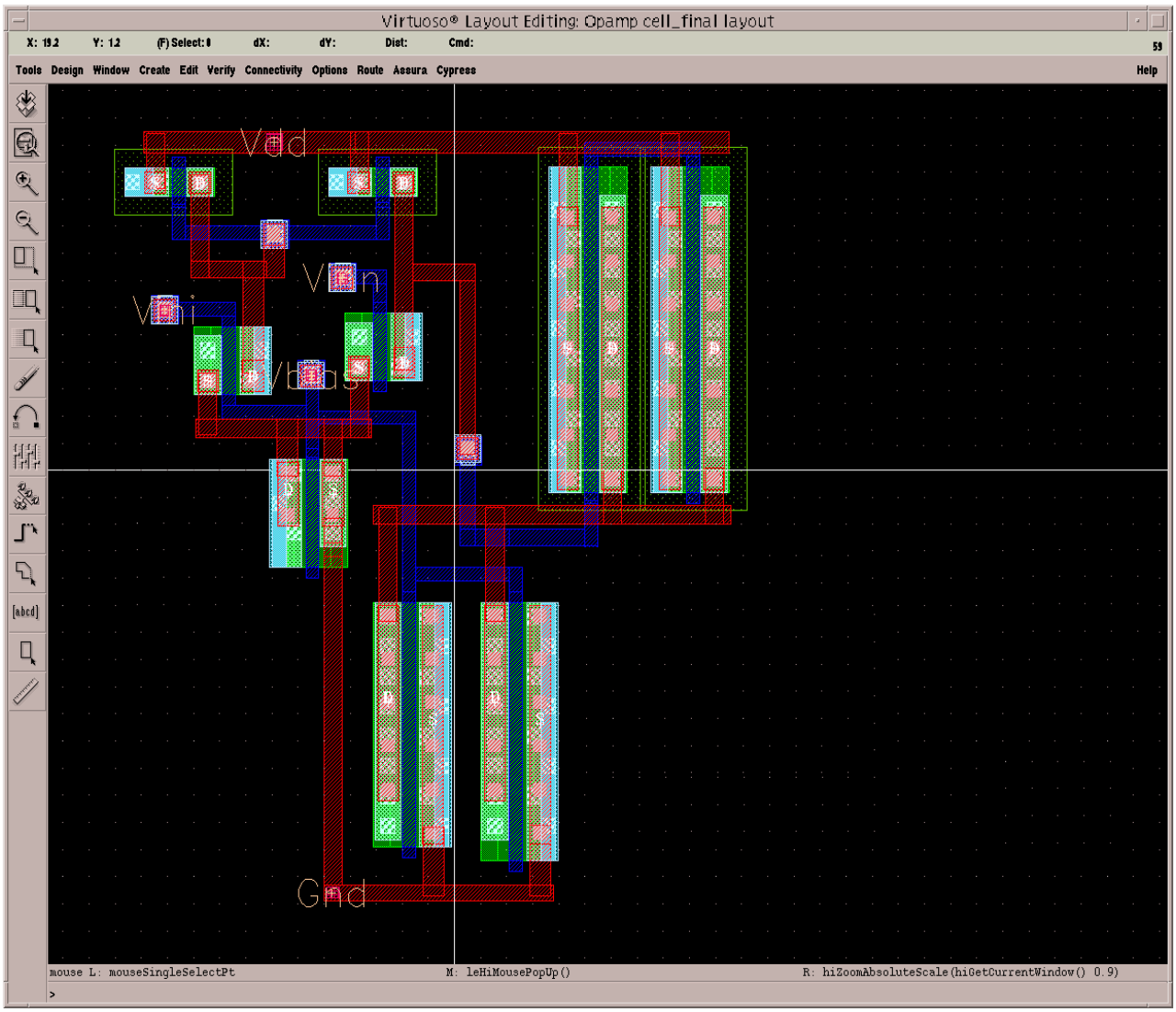


Figure 27 : Layout of op-amp

Layout of the buffer

The layout of the buffer is shown below:

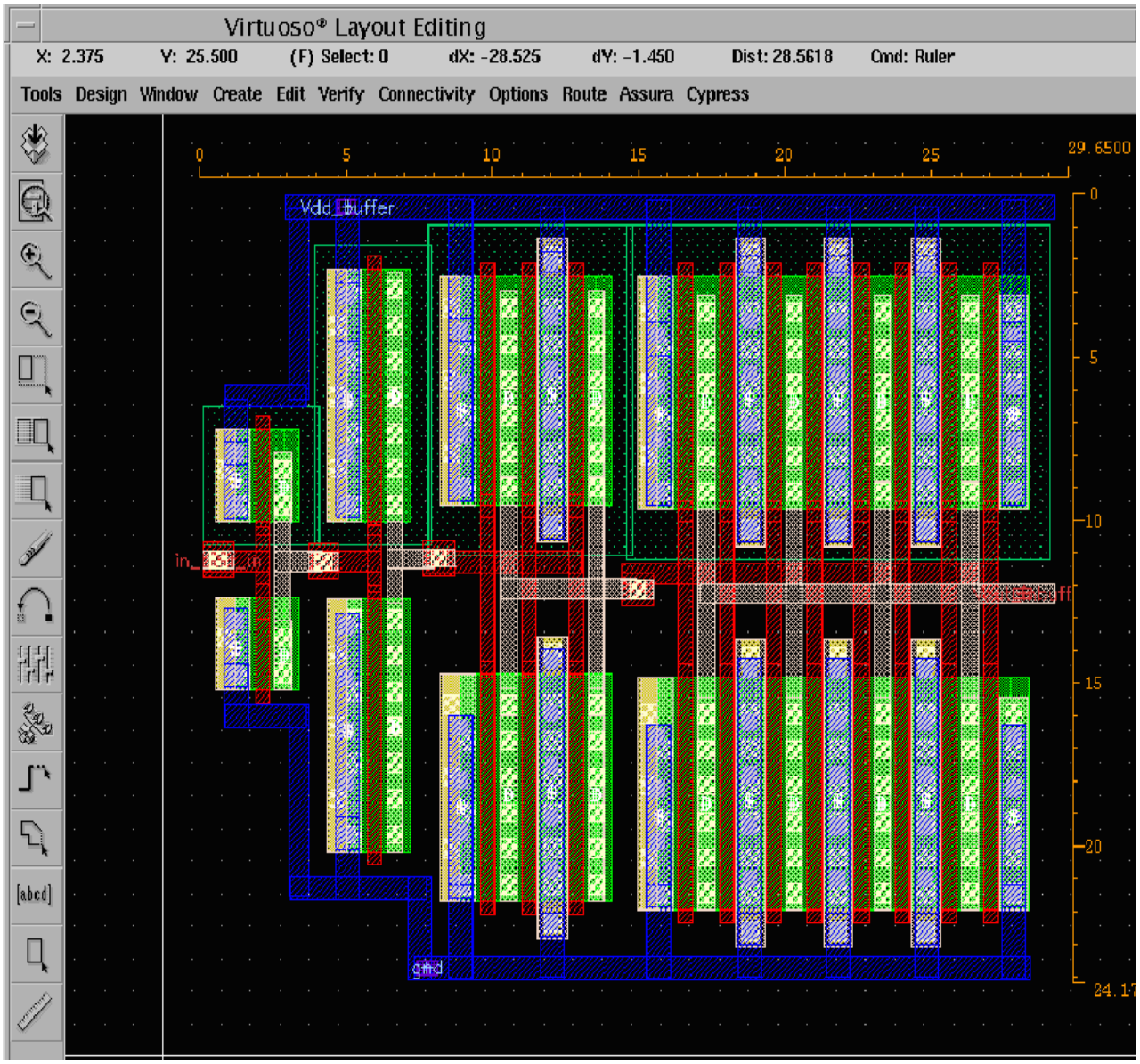


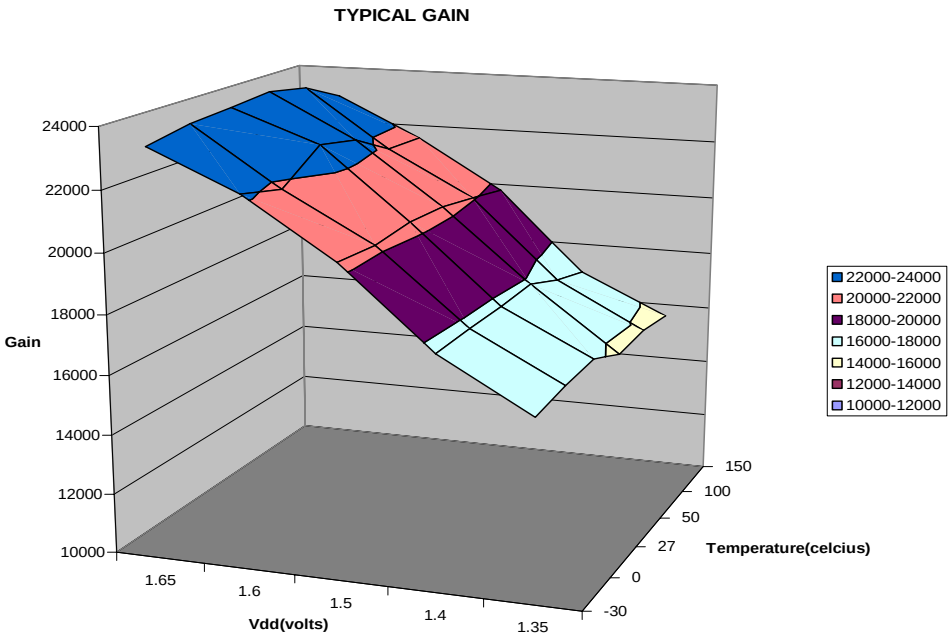
Figure 28 : Layout of Buffer

Corners

The performance of the op-amp varies with parameters like the temperature and the supply voltage. Corners here refer to extreme conditions of temperature and voltage. The performance of the circuit is tested at temperatures varying from -30 to 150 degrees Celsius. The voltage is varied to ±10 % of the specified voltage. Apart from this, during manufacturing process, the mosfets may be slower or faster than the designed value. The circuit is simulated for three cases: slow, typical and fast.

Table 1: Variation of gain with temperature and supply voltage for typical corners

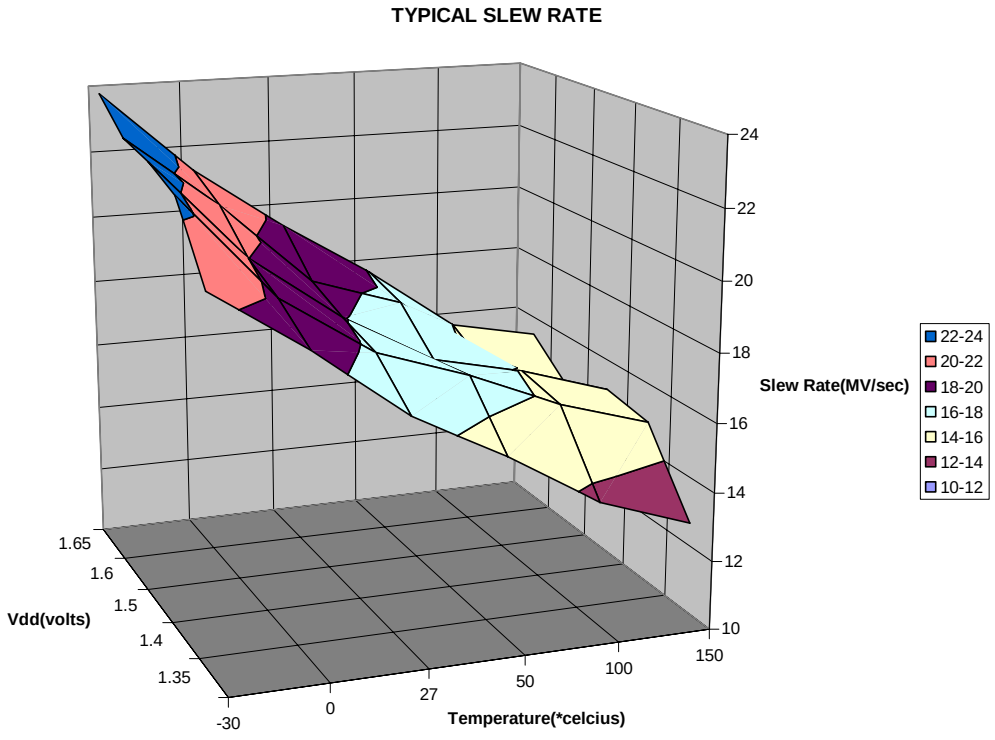
	Vdd (volts)	1.65	1.6	1.5	1.4	1.35
S.No	Temperature (celcius)	Gain				
1	-30	23465	22172	20275	17696	16006.8
2	0	23710	21781	20190.5	17749	16187
3	27	23803	22729.6	20351.6	17760	16271
4	50	23923	22416	20291.5	17843	15669
5	100	23643.8	21616	20054.7	17327.8	15754.8
6	150	22942	21538.9	19786.5	16953	15576



The slew-rate of op-amp is measured at typical corners for varying values of Vdd and temperature

Table 2 : Variation in slew-rate of op-amp with temparature and supply voltage at typical corners

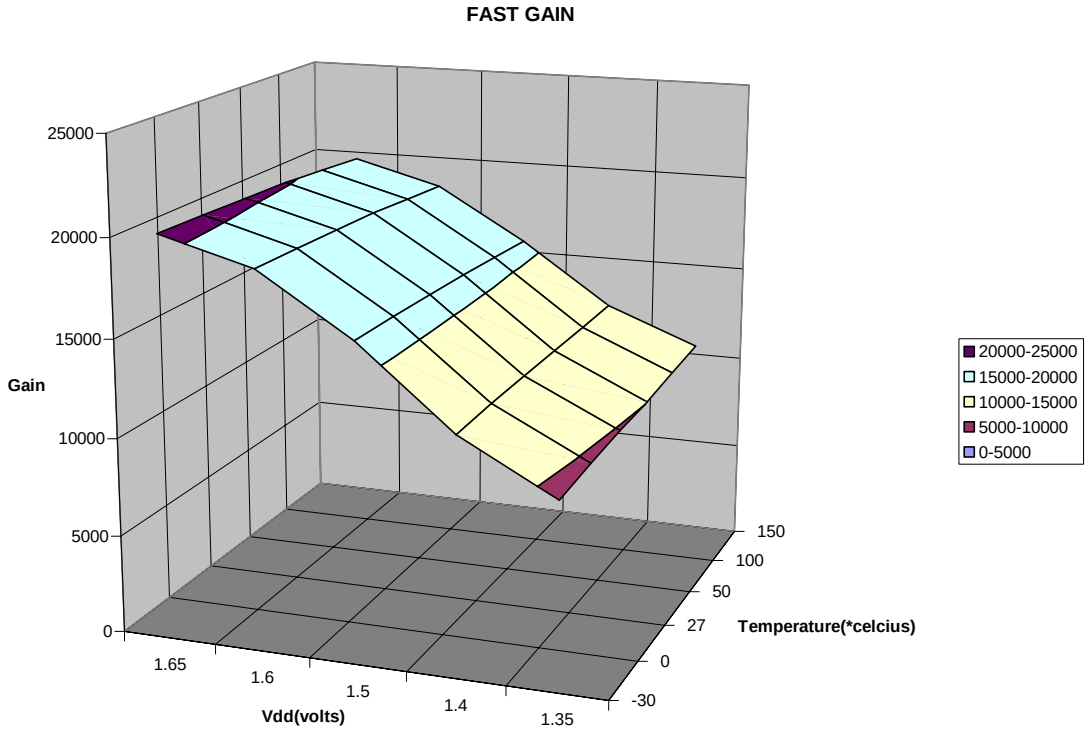
	Vdd (volts)	1.65	1.6	1.5	1.4	1.35
S.No	Temperature (celcius)	Slew Rate				
1	-30	23.974	23.112	22.93	22.513	20.561
2	0	21.51	20.98	20.015	19.4992	18.75
3	27	19.617	18.5	18.05	17.713	16.68
4	50	17.929	17.6	17	16.804	15.24
5	100	15.986	15.317	15.93	15.67	13.61
6	150	15.439	14.375	15.087	14.851	12.674



The gain of op-amp is measured at fast corners for varying values of Vdd and Temperature

Table 3 : Variation in gain of op-amp with temparature and supply voltage at fast corners

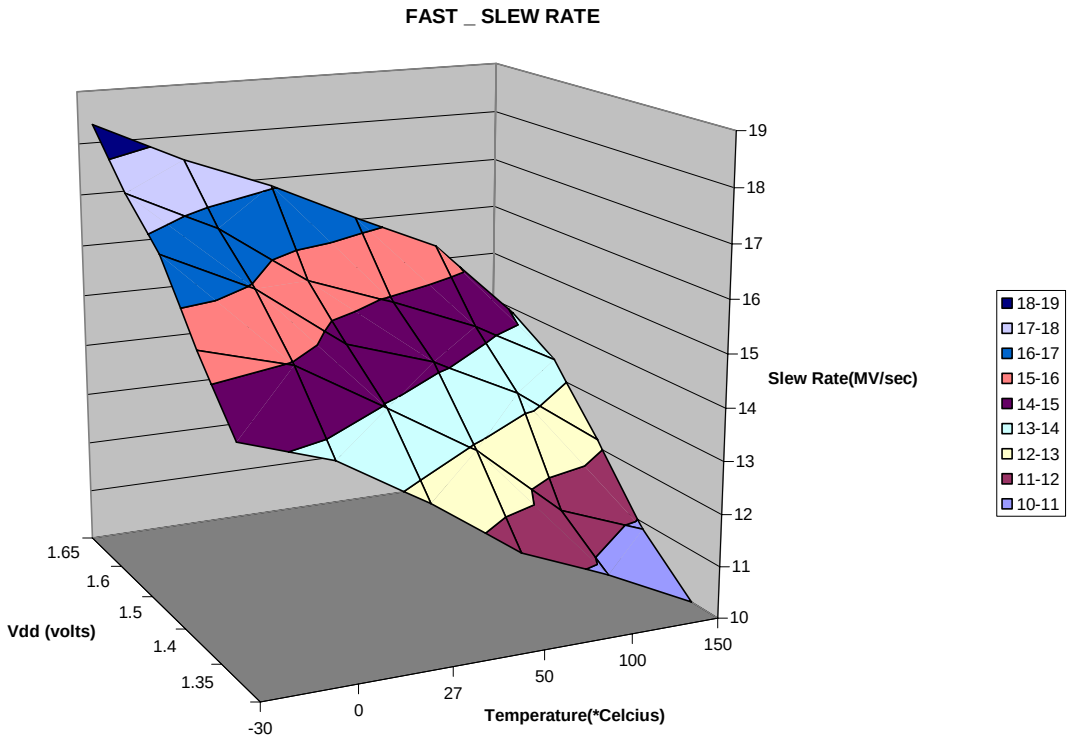
	Vdd (volts)	1.65	1.6	1.5	1.4	1.35
S.No	Temperature (celcius)	Gain				
1	-30	20370.37	19069.88	16054.7	12054.19	9455.59
2	0	20298.55	18990.81	16018.16	12161.67	9715.75
3	27	20177.11	18889.08	15951.45	12212.52	9890.155
4	50	20076.2	18794.19	15881.79	12237.14	10011.24
5	100	19844.9	18572.6	15722.85	12272.95	10233.95
6	150	19615.18	18358.49	15585.42	12324.33	10448.9



The slew-rate of op-amp is measured at fast corners for varying values of Vdd and temperature

Table 4 : Variation in slew-rate of op-amp with temparature and supply voltage at fast corners

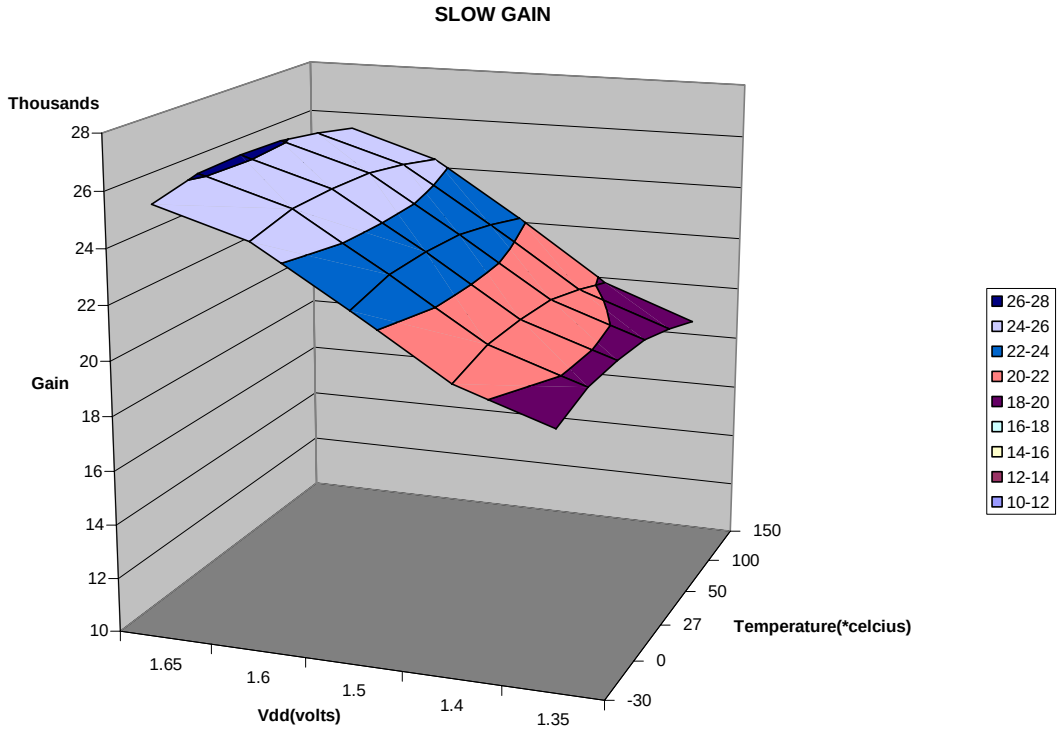
	Vdd (volts)	1.65	1.6	1.5	1.4	1.35
S.No	Temperature (celcius)	Slew Rate				
1	-30	23.974	23.112	20.015	22.513	20.561
2	0	19.971	22.378	20.015	19.4992	18.75
3	27	19.617	20.29	19.2139	17.713	15.126
4	50	17.929	20.038	18	16.804	14.41
5	100	15.986	15.317	15.93	16.22	13.61
6	150	15.439	14.375	15.087	14.851	12.674



The gain of op-amp is measured at slow corners for varying values of Vdd and Temperature

Table 5 : Variation in slew-rate of op-amp with temperature and supply voltage at slow corners

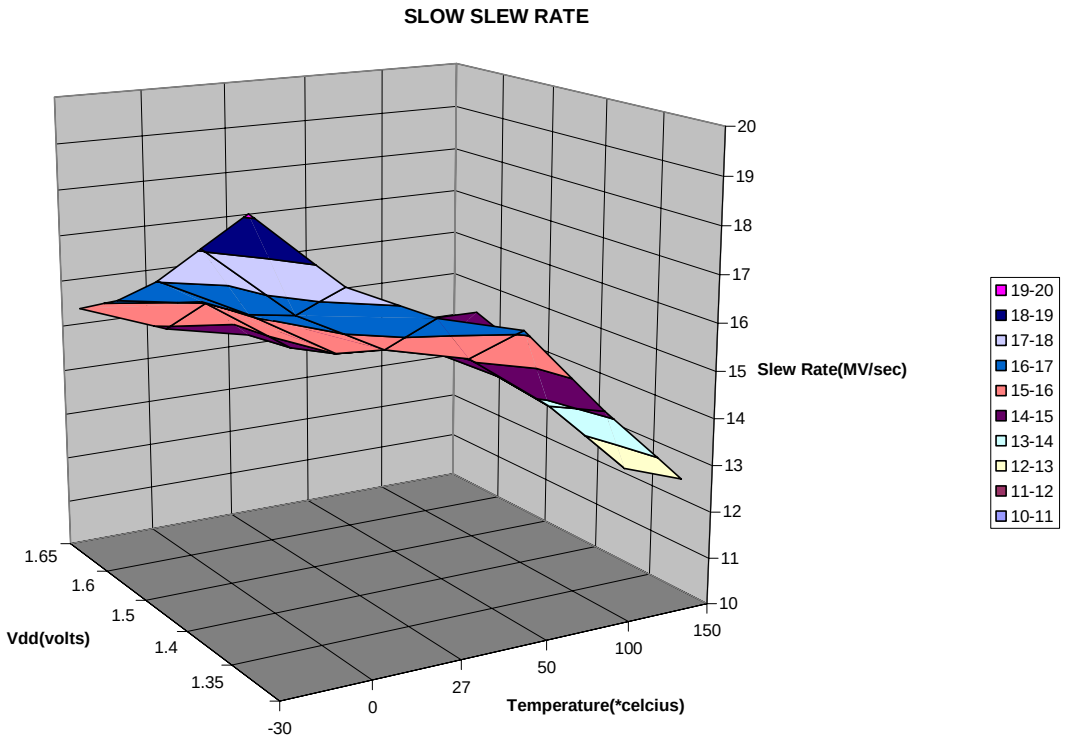
	Vdd (volts)	1.65	1.6	1.5	1.4	1.35
S.No	Temperature (celcius)	Gain				
1	-30	25675.52	24661.44	22584.19	20406.26	19242.83
2	0	26086.22	25075.91	23009.46	20846.28	19688.58
3	27	26126.72	25108.45	23050	20866.31	19693.47
4	50	26059.54	25041.18	22959.74	20757.61	19564.71
5	100	25764.4	24732.88	22610.6	20336.06	19093.97
6	150	25371.09	24324.46	22152.13	19802.02	18523.34



The slew-rate of op-amp is measured at slow corners for varying values of Vdd and temperature

Table 6 : Variation in slew-rate of op-amp with temparature and supply voltage at slow corners

	Vdd (volts)	1.65	1.6	1.5	1.4	1.35
S.No	Temperature (celcius)	Slew Rate				
1	-30	15.61	16.21	17.03	18.07	19.1
2	0	14.9	15.9	16.1	16.52	17.5
3	27	14.5	14.67	15.01	15.56	16.65
4	50	14.39	14.5	14.9	15.1	16.15
5	100	14.29	14.4	13.96	13.8	14.2
6	150	14.27	13.81	12.67	12.1	12.43



Conclusion

The Op-amp is designed and simulated with a six stage output buffer to drive a load of 20 pf and which is the capacitance of the oscilloscope. The gain and slew rate are observed under different W and L values. The layout is drawn and placed to fit in the e-test pad. The performance of the op-amp is tabulated and plotted at different process corners (Fast, Slow and Typical).

Reference

CMOS Circuit design, Layout, and simulation: R. Jacob Baker.

CMOS Analog circuit and design: Phillip E. Allen, Douglas R. Holberg.

Software:

CADENCE.

Microsoft Excel 2003.

Microsoft Word 2003.

Microsoft office project 2003.