

Computer-Aided Design for Manufacturability

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From DSM to DFM

- A new layer of difficulties on top of the complex physics of DSM
- *Advanced manufacturing* introduces new challenges
- It's hard to manufacture a chip in the way we wanted it to be
- Need a whole new strategy:

Design for Manufacturability

What is Design for Manufacturability?

- Design for Manufacturability:
 - A set of techniques addressing key problems of reliability and manufacturability of scaled ICs
- DFM effects and concerns driven by *limitations of manufacturing control*
- Goal of IC design-to-manufacturing link:
 - Silicon = Design
- But, manufacturing equipment and processes are not perfect
 - Distortions, biases, non-idealities, etc...

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Major Ways to Break and Fix Design-to-Manufacturing 'Equation'

- Semiconductor process is not good enough for my design
 - Can't print $L_{gate} = 70\text{nm}$ using available 248nm photolithography machine
 - Design rules are such that some layout features will not print
 - 1st problem:

modify design so that the process can properly manufacture the chip

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Major Ways to Break Design-to-Manufacturing 'Equation'

- Semiconductor process is not sufficiently stable
 - 70% of all chips are fine, but 30% are too slow
 - 2nd problem:
change design so that the chip is less susceptible to process variation
- Semiconductor process is not “clean” enough
 - Dust particles kill 25% of all otherwise good chips
 - 3rd problem:
modify design so that it is less likely to suffer from particles

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Process Variability and Its Impact: Introduction

- Increased device variation
- Increased interconnect variation
- Result
 - Slower speed of digital circuits
 - Greater uncertainty about parameter values
 - Over-conservatism
 - Reduced signaling robustness
 - Increased clock skew

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Process Variability Grows

- Relative magnitude of process variation expected to grow significantly

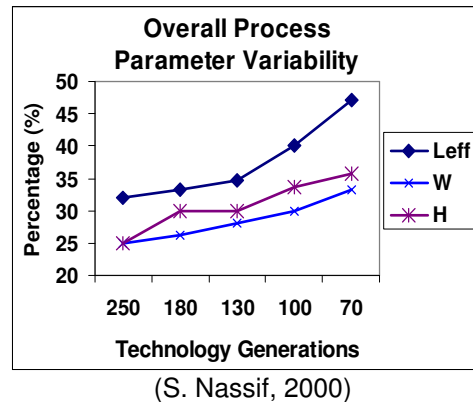
- Manufacturing limitations

- E.g. photolithography

- Fundamental atomic scale randomness

- E.g. dopant placement

- Figure: L_{eff} : effective transistor length; W : wire width; H : wire height



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Component Variation

- Total variation

- systematic variation +
- random variation

- Variation Sources

- Due to photolithographical proximity effect, mask alignment, etching, erosion, dishing, deposition, implant, doping profile, temperature

- Systematic Variation

- Deterministic
- Depending on layout density, orientation, and/or location

- Random variation

- Due to random process variations
- Due to fundamental randomness

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Variation Scope

- Inter-Die Variation
- Intra-Die Variation

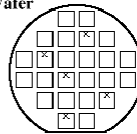
Lot-to-Lot



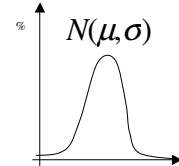
Wafer-to-Wafer
(or within Lot)



Within Wafer



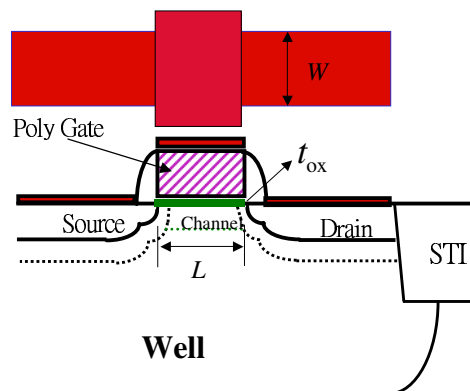
Intradie



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Device Parameter Variations

- W, L variations
 - Due to photolithography proximity effect or etching
 - Layout density dependent
 - Location dependent
- t_{ox} variation
 - Well controlled by a product spec.
- V_{th} variation
 - Due to doping

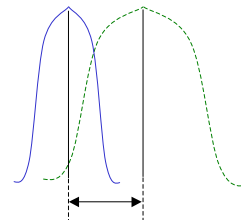
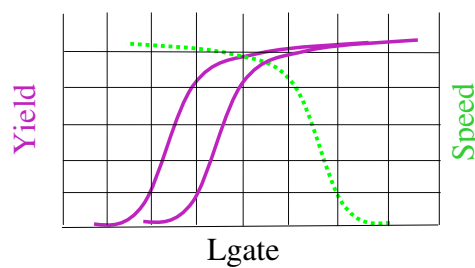


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Key Component of Variation: Lgate Variation

- Control of gate (channel) length of transistor – Lgate – is extremely important
- Economics of high-performance chips is very sensitive to Lgate variation
- E.g. every nm of Lgate spread reduction means about \$10 of more revenue per CPU chip...

Source: ITRS 1999



\$7.5/nm/chip for the 0.25μm technology

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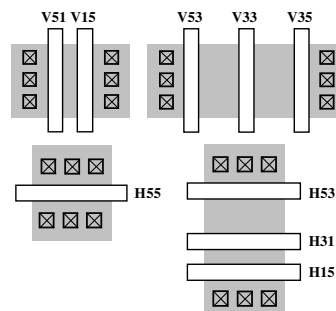
Complex Patterns of Intra-Chip Lgate Variation

- Intra-chip variation becomes significant
 - E.g. in 0.13μm CMOS, intra-chip variation of effective transistor length is 35% of total variation
- Lgate exhibits very complex patterns of intra-chip variation
 - Most of it is systematic
- Variation depends on the layout

A) Distance to neighboring gate (proximity effect)

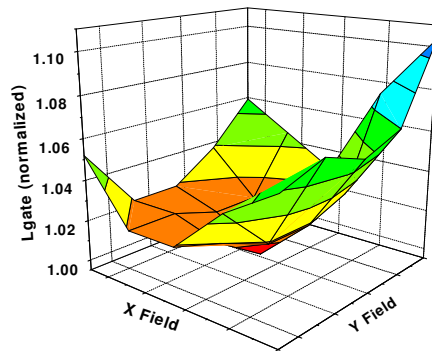
B) Left vs right neighbor position (coma effect)

C) Vertical vs horizontal orientation

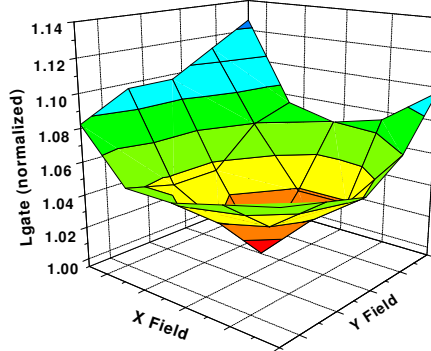


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Different Spatial Variation Patterns Depending on Local Layout



Category V53



Category V33

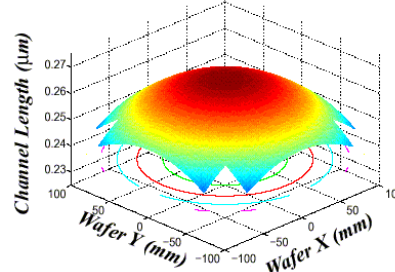
- Global intra-chip spatial variation patterns are different for different local layout patterns
- Separate models need to be used at the CAD level

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Components of Lgate Variation: Within-Wafer Variation

- Intra-chip component can theoretically be 'accessed' by CAD tools through manipulation of layout
- Within-wafer variation component is encountered as random additive noise – cannot be corrected by CAD tools
- A large random, unmodeled component of variation is left
- This component will have to be dealt with by probabilistic circuit-analysis techniques

Simulated Wafer-Level Variation



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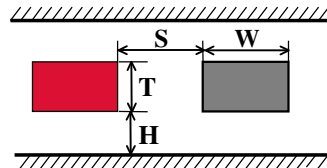
Lgate Variability

- Much of Lgate variability is systematic within a chip? Can we do anything?
- For systematic portion, much of variability is compensated by optical proximity correction (OPC) and phase-shift masking (PSM)
- Spatial variation – which is most troubling – is not currently dealt with
 - It is theoretically *possible* to compensate systematic spatial variability, but economically probably unfeasible
- Remaining random component of variation will have to be dealt with through probabilistic CAD tools

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Interconnect Parameter Variations

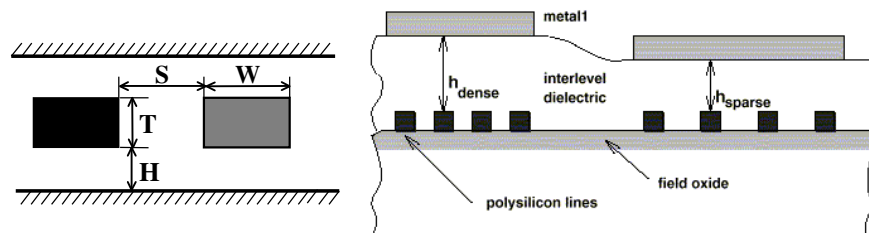
- Line width(w), spacing(s)
 - Due to photolithography proximity effect or etching
 - Layout dependent
 - Location dependent
- Metal thickness(T)
 - Due to erosion, dishing
 - Layout density dependent
- Dielectric thickness(H)
 - Due CMP
- Dielectric Constant(ϵ_0)



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ILD Thickness Variation

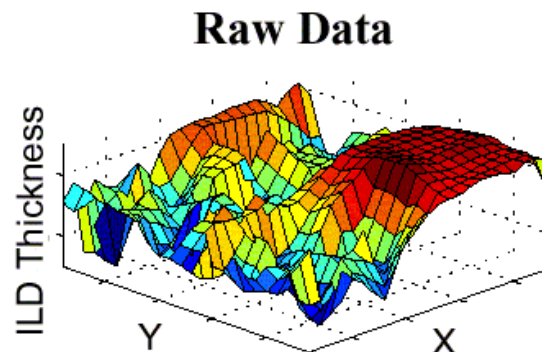
- Major source of interconnect parameter variation is
 - ILD thickness variation
- Inter-Layer Dielectric(ILD) thickness depends on the underlying pattern density



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Intra-Chip ILD Thickness Variation

- Because there are significant differences in wiring density, within chip variation may be quite large
 - Up to 20%
- Most of ILD thickness variation is systematic – can be corrected
- The rest is 'random'



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Process Variation: Summary

- Many other sources of device and interconnect parameter variation
 - Resistivity of vias and interconnect lines
 - Threshold voltage fluctuation
- Most types of parameter variation we didn't mention are 'random'
 - Have to be dealt with by probabilistic, rather than systematic correction, circuit-analysis techniques
- What is more important than process parameter variation *per se* is its impact on circuit performance!

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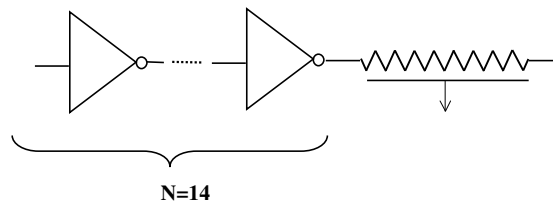
Impact of Process Variation on Circuit Performance: Major Factors

- Traditionally: device variability is dominant
- Deep Sub-Micron: interconnect delay contribution grows
- Perhaps *interconnect variability dominates*
- Realistic analysis has to consider device and interconnect variability *jointly*
- Need to distinguish *global* and *local* interconnect

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Modeling Framework: a Canonical Critical Path Circuit

- Critical path circuit:
 - 14-stage gate chain
 - 2-input NANDs with average FO=2.5
- Gate stages separated by local interconnect lines
- There is one global interconnect line *buffered by repeaters*



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Variability Modeling

- Variability model: $V_{TOT} = \sum_{i=1}^n V_i$
- Assume linear *delay* response:

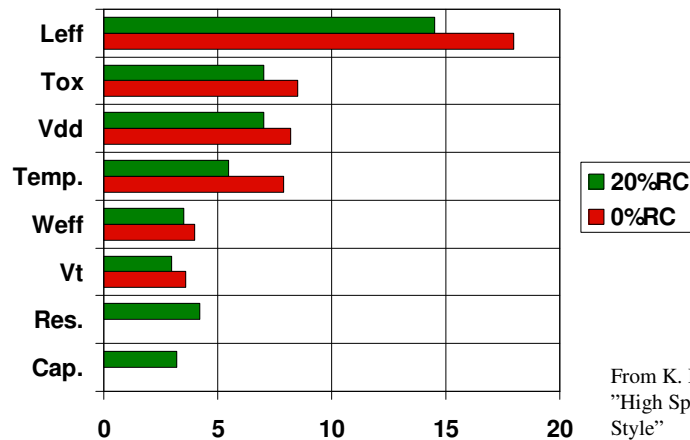
$$\Delta D = \sum_{\{P_{dev}\}} \frac{\partial D}{\partial p_i} \Delta p_i + \sum_{\{P_{loc}\}} \frac{\partial D}{\partial p_i} \Delta p_i + \sum_{\{P_{gl}\}} \frac{\partial D}{\partial p_i} \Delta p_i$$

- Variability of each source is $V_{p_i} = \left(\frac{\partial D}{\partial p_i} \right)^2 \sigma_{p_i}^2$

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Sensitivity of Delay to Process and Environment Variation

- Each process parameter varies with 3 sigma, vdd +/- 8%, and +/- 50 temperatures.

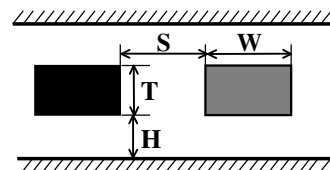
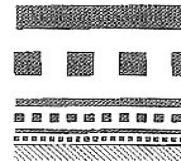


From K. Bernstein, et al.,
"High Speed CMOS Design
Style"

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Variability Decomposition: Example

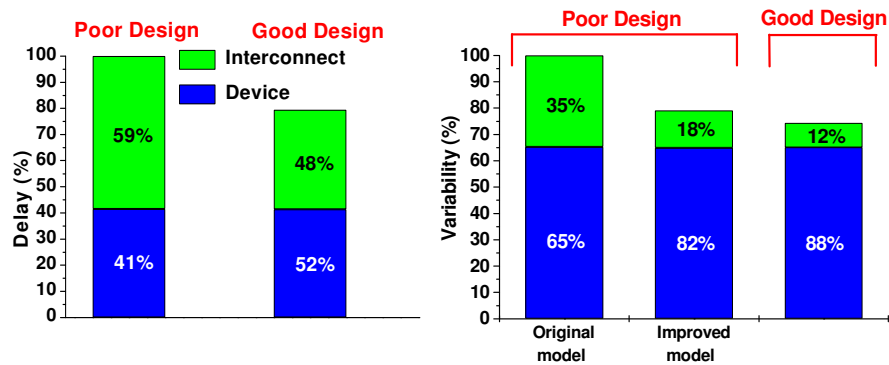
- Overall variability is determined by (a) sensitivities, and (b) variances
- Need to assume specific variance values
 - Values depend on design/technology choices
- "good design": wide pitch for global interconnect, min pitch for local connections;



Technology Choice	Lgate	W/S	Wg/Sg	H/Hg	Tox/T/Tg
Good	0.15	0.12	0.015	0.15	0.02
Poor	0.15	0.12	0.09	0.15	0.02

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Variability Decomposition: Results



- Only for poor designs, a sizable portion of variability (35%) is due to interconnect
- For good designs interconnect variability contribution is small (12%)

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Summary of Variability Effects

- Theoretical analysis shows that device variability may still be responsible for the majority of circuit performance variation
- However, this very much depends on
 - Technological choices
 - Design choices

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Outline

- Introduction: DSM vs. DFM
- Deep submicron effects
 - Device and technology challenges
 - Circuit design challenges
- Design for Manufacturability
 - Process and circuit variation
 - **Systematic approaches: printability and planarity**
 - Probabilistic approaches
- And the winners are...: What are the truly hot issues?

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Systematic DFM Techniques

- We know and can model some of the sources of process parameter variation
 - E.g. proximity dependent L_{gate} variation
 - E.g. density-dependent ILD thickness variation
- For these systematic variation components we can come up with preventive or corrective measures
- For the rest, we have no choice but to treat them as random distributions

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DFM: Resolution Enhancement Techniques for Printability and Planarity

- To reliably manufacture nanometer-scale chips, need an enhancement of the process capabilities *from the design side*
- Reason: the process capabilities can't keep up with scaling requirements
- Two major problems
 - Quality of photolithography (printability)
 - Wire uniformity (planarity)

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Printability

- Creating a GDSII 'tape' used to be the last step of circuit design
 - Silicon was a 'copy' of layout
- Advanced processing leads to significant distortions of layout patterns
- We are no longer in the era of "what you see is what you get"
- Need to apply special techniques to get a predictable silicon pattern

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Printability: Introduction

- “Basic” photolithographic sequence
 - Based on layout (GDSII), a mask is created
 - Mask pattern is shone onto resist with light to project pattern

- Minimum ‘printable’ feature size depends on wavelength of light

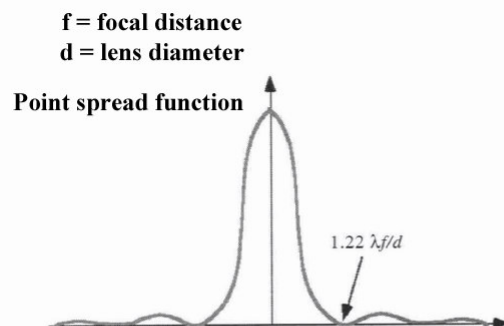
$$L_{\min} \propto \frac{\lambda}{NA}$$

λ is wavelength of light, NA is numerical aperture

- CMOS scaling requires using smaller wavelengths of light for photolithography

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Resolution in Projection Printing



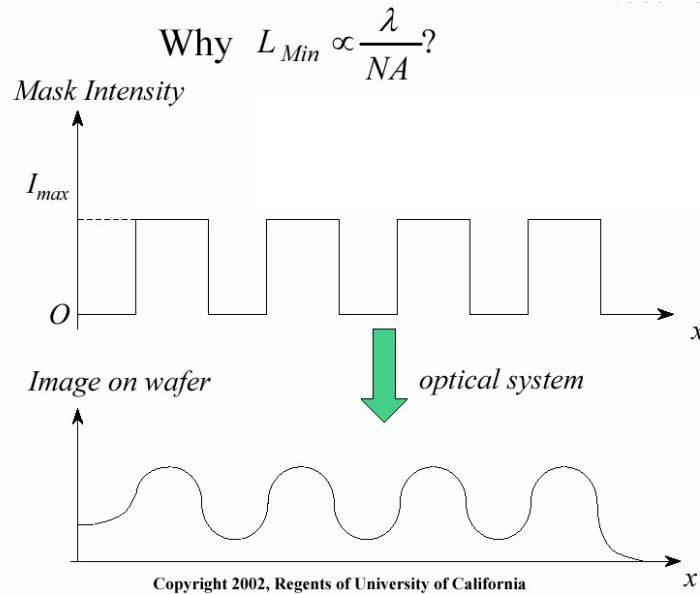
Null position

$$1.22\lambda \left(\frac{f}{d} \right) = 0.61\lambda \left(\frac{f}{\frac{d}{2}} \right) = 0.61 \frac{\lambda}{NA}$$

Copyright 2002, Regents of University of California

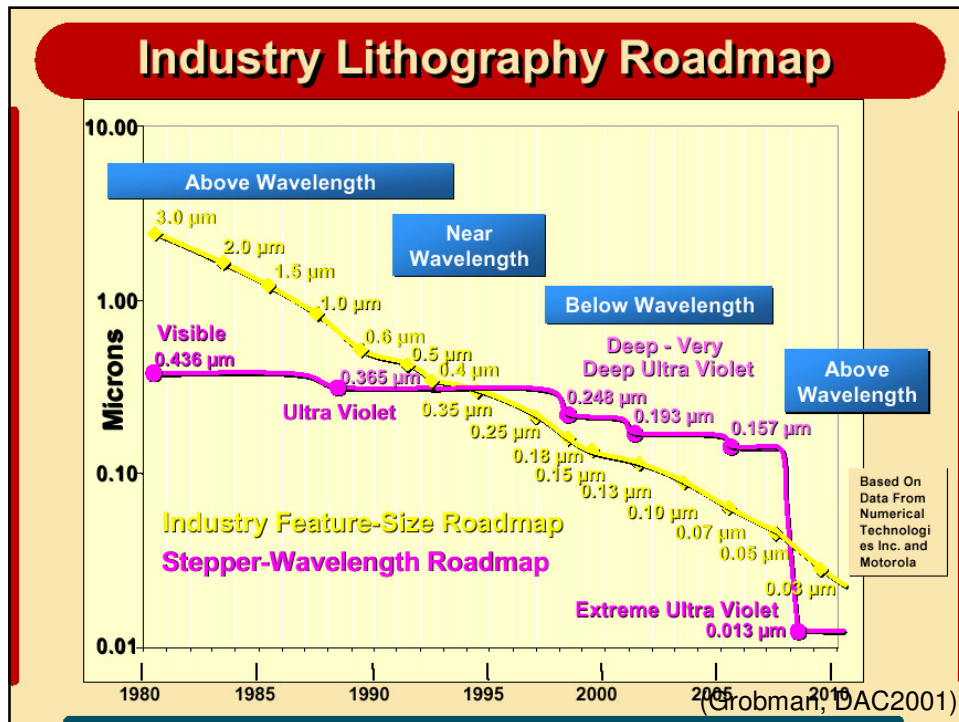
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Why Is Image Degraded?



Fundamental Issue: Sub-wavelength Photolithography

- Smaller wavelengths of light required for scaling
- Difficulty: cannot easily reduce wavelength
 - New illumination source
 - New resists
 - Capital expenditures
- Forced to print features below wavelength
- Pattern degradation



What Can Be Done

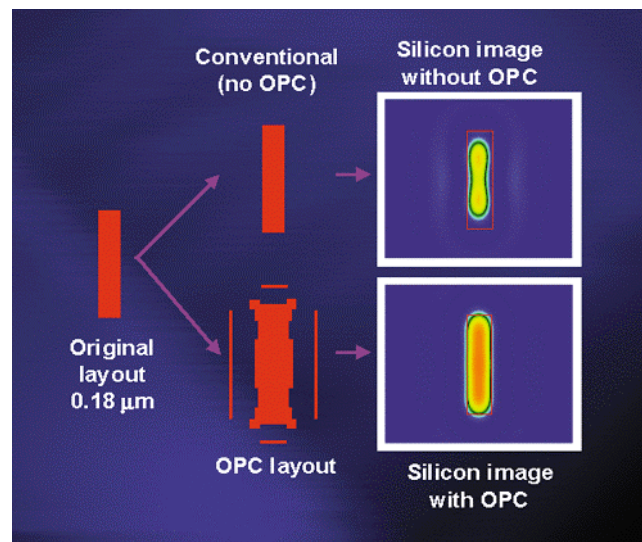
- Optical proximity correction (OPC)
- Phase-Shift Masking
- Sub-resolution assist features
- Tiling for interconnect planarity

Optical Proximity Correction (OPC)

- Close mask features interact to distort the wavefront
- By predicting the result, can try to compensate the distortion
- Optical Proximity Correction intentionally introduces additional features into the mask to compensate for the effects of proximity of two features

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OPC - Overview



(Numerical Technologies, Inc.)

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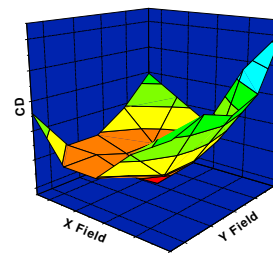
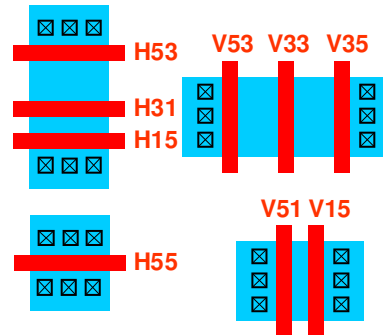
Distortion Types: Line Width Variation

- **Separation-dependent (poly) line-width variation**

- Isolated lines – least affected, narrowest
- Dense lines – most affected, wider than isolated lines

- **May also depend on**

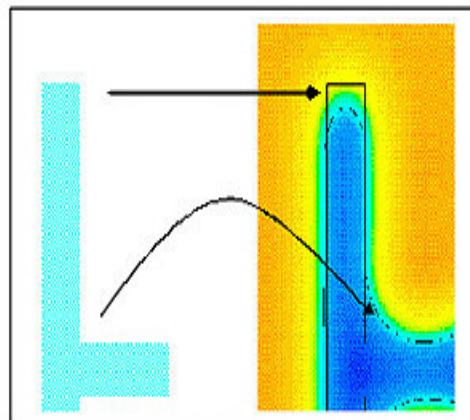
- Poly-line orientation (vertical / horizontal)
- Left and right neighboring lines
- May have spatial variation across chip



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Other Distortions

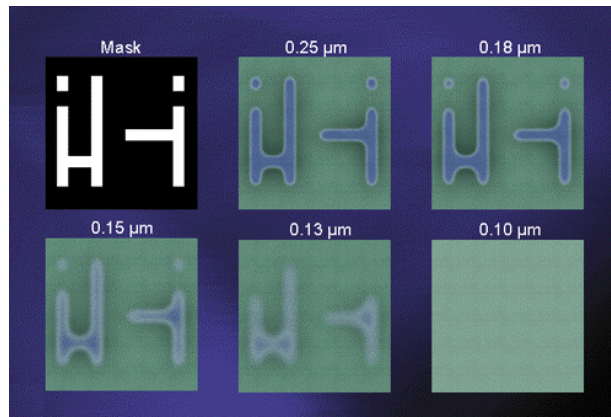
- **Line-end shortening**
- **Corner-rounding**



(Numerical Technologies, Inc.)

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The New Subwavelength World



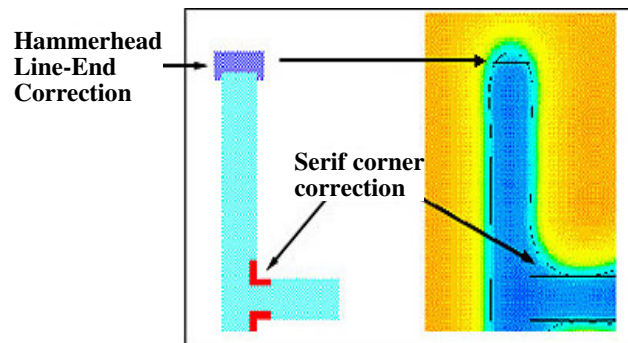
(Grobman, Wang, "Practical IC Design in the Subwavelength Regime")

- Using today's lithography equipment, feature sizes below 0.15μm will not form at all on silicon

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Optical Proximity Correction (OPC)

- Create a bias on width depending on isolated / dense structure for line-width control
- Add hammerhead line-end correction
- Add serifs for corner correction

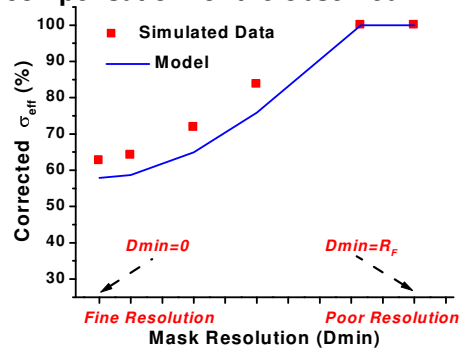


(Numerical Technologies, Inc.)

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Mask-Level Lgate Correction Algorithm

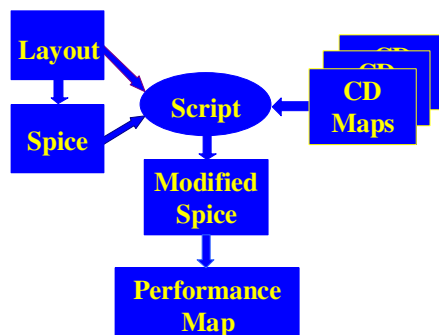
- Another way to reduce spatial Lgate variability: *mask-level correction*
 - A mask is fabricated with compensation for the observed aberration profile
- Complete correction is impossible
 - Finite mask resolution
- Up to 35% variability reduction seems to be possible



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Addressing Systematic Process Variation at Circuit Level

- To compensate effect of spatial Lgate can incorporate spatial information into circuit timing analysis
- Standard CAD tools need modifications
- Very expensive approach
 - Spatial maps are die-specific



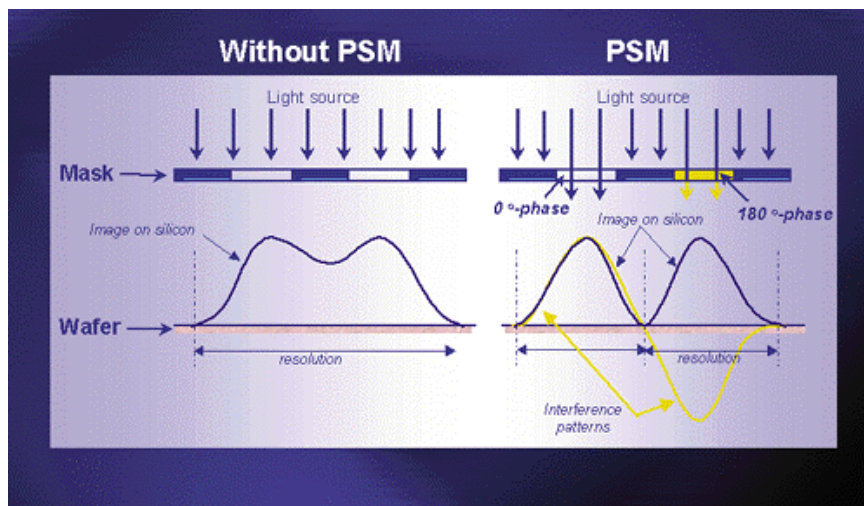
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Phase Shift Masking

- A more effective way of controlling printability
- Direct modification of the optical wavefront
- Produces out-of-phase wavefronts for nearby features
- Reduces optical interference for nearby features
 - Higher effective resolution
 - Higher DOF

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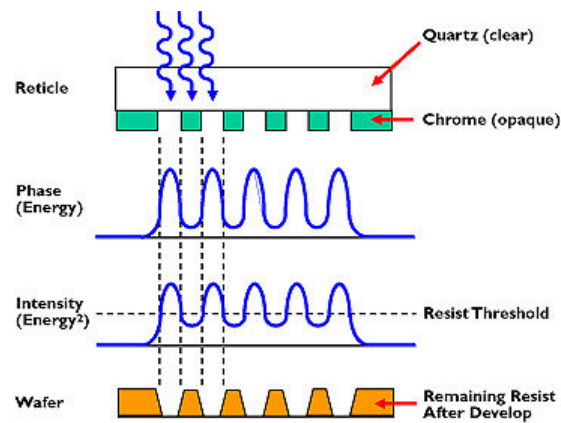
Changing Optical Wavefront: Phase Shift Masking



(Numerical Technologies, Inc.)

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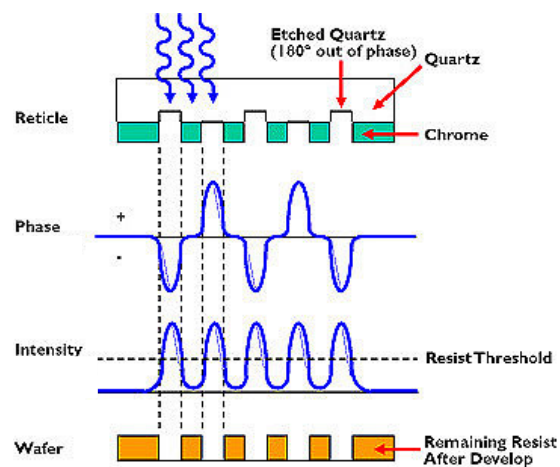
Mask Types: Binary Mask



(ASML MaskTools)

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Mask Types: Alternating PSM (AltPSM)

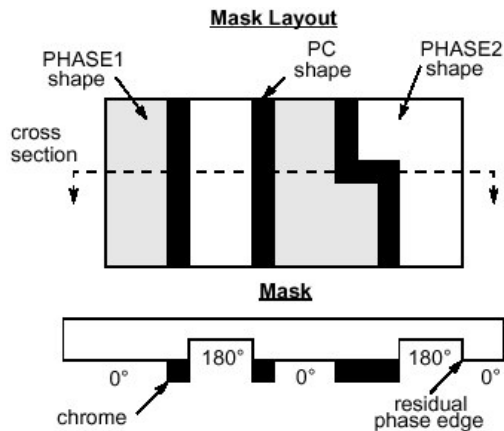


(ASML MaskTools)

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Phase Assignment in PSM

- Partition layout into regions of opposite phases



- Critical and non-critical features

- Critical features require a phase transition
- Non-critical features don't require a phase transition

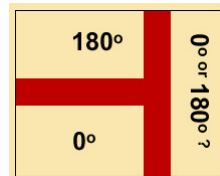


(Liebman, DAC2001)

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Verification in PSM Designs

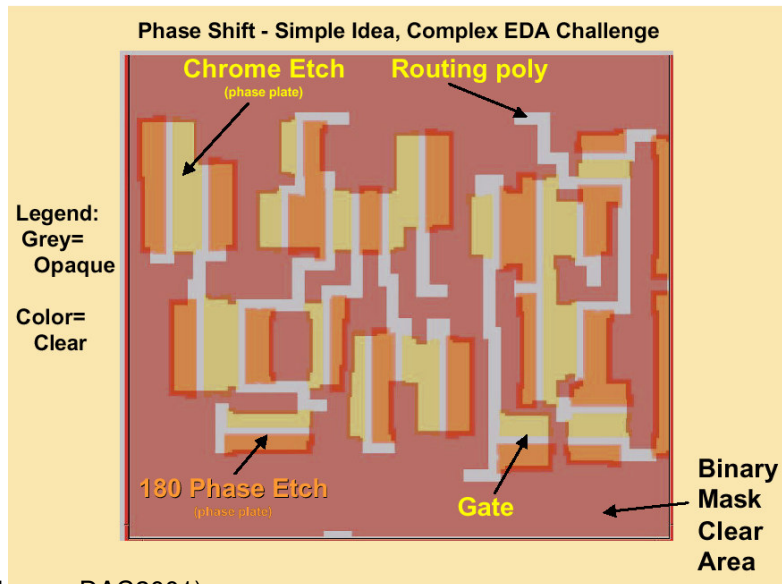
- Phase conflicts are possible during phase assignment



- Solution
 - Change spacing
 - Change feature sizes
 - Layout density may have to be relaxed
- Failure to correctly assign phases may lead to yield problems
 - Accurate DRC needed
- Rule-based
 - Faster, may not be flexible enough
- Model-based
 - LVS (Layout vs. Silicon): an EM simulation, rather than simple geometrical property checking

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EDA Solution for PSM is Difficult



(Grobman, DAC2001)

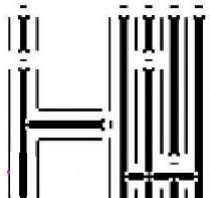
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Sub-Resolution Assist Features

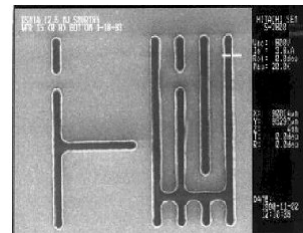
- Also known as *scattering bars*
- Lithography equipment does not form images of these features
- Creates a diffraction pattern for isolated lines more like dense lines
 - Match Iso & dense lines



Designed layout



Final layout



Wafer

(Schellenberg, DAC2001) 52

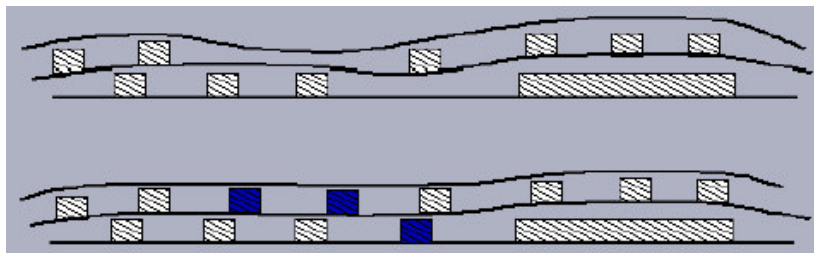
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Planarity of Al Metal CMP Processes

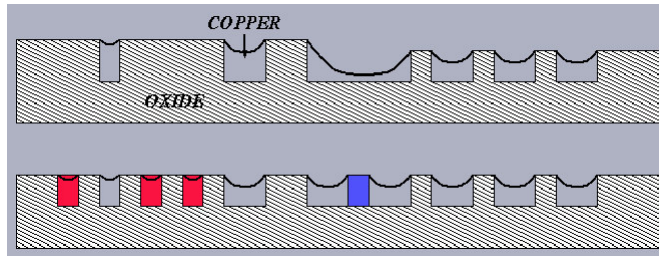
- Chemical-mechanical polish (CMP) rate is different for sparse and dense areas
- Tiling: adds new features in sparse areas to ensure better planarity
- Design problem: determine location and amount of dummy features needed to achieve a planarity



(Grobman, DAC2001)

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Planarity In Copper CMP Processes



- For Cu processes have two problems
 - Oxide erosion
 - Copper 'dishing'

(Grobman, DAC2001)

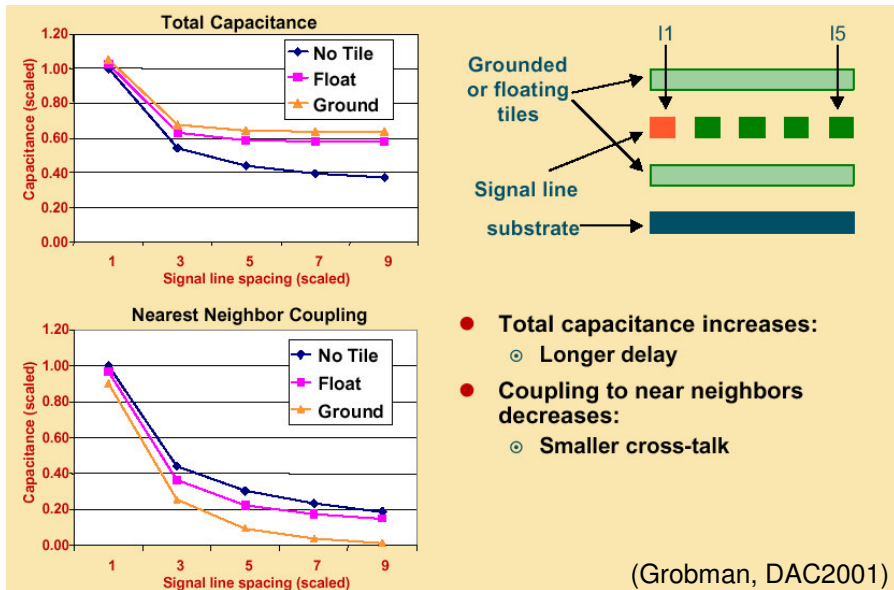
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Tiling as and EDA Problem

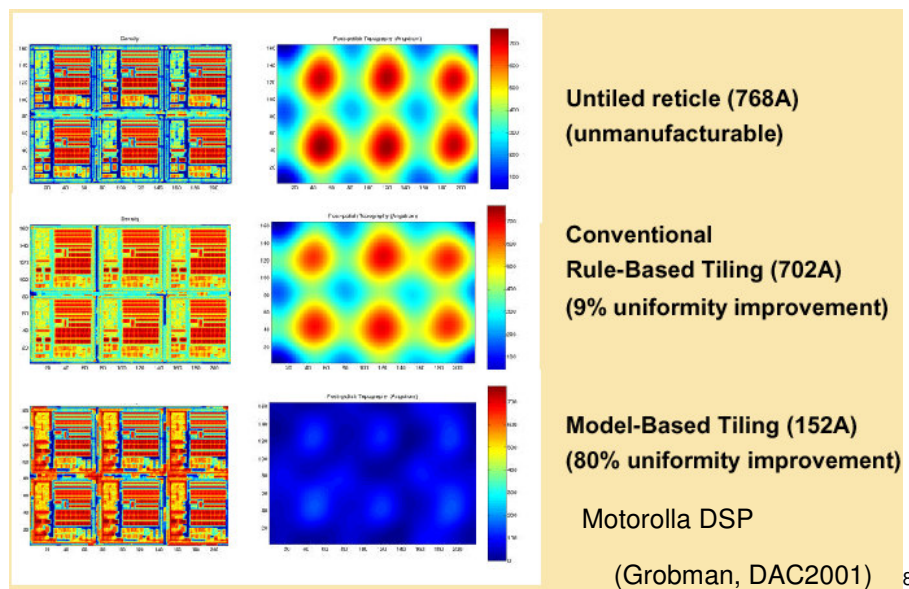
- Rule-based vs. Model-based Tiling
 - Some Designs Become *LESS* Planar with Rule-based!
 - Model-based tiling is computationally very expensive
- Tiling effects coupling and delay!!!
 - EM Modeling for Total Capacitance and Crosstalk
 - Dependence on Grounding or Floating of Tiles
 - Tile Size vs. Wire Pitch is Important
- Tiling May Cause Mask Verification Problems

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Effect of Tiling: Delay and Cross-Talk



Tiling for Better Planarity



RET: Summary

Ret: Increasingly Affecting Design

	0.25 um	0.18 um	0.13 um	0.10 um	0.07 um
Rule-based OPC	●	●	●	○	●
Model-based OPC			●	○	●
Scattering Bars		○	●	○	
AA-PSM			●	○	●
Weak PSM			●	○	●
Rule-based Tiling		●	●	○	●
Optimization-driven MB Tiling			○	○	●

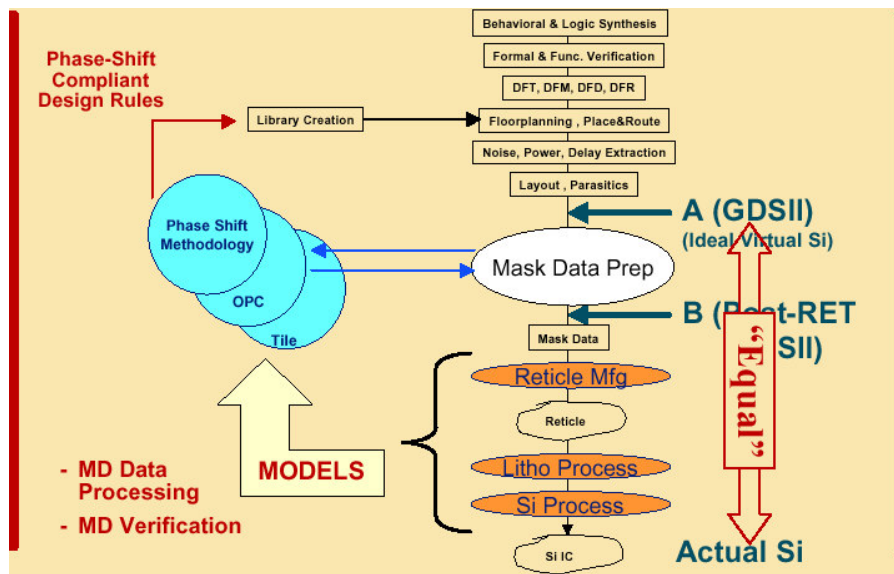
Number Of Affected Layers Increases / Generation

- 248 nm
- 248/193 nm
- 193 nm

(Grobman, DAC2001)

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New Back-End Design Flow



(Grobman, DAC2001)

0

Printability and Planarity: Summary

- Ensuring printability and planarity of small features is very difficult in sub-wavelength lithography
- Impacts design flows and requires new tools
- Designers will have to learn to take into account these factors, and techniques to improve manufacturability

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 - Probabilistic approaches
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Probabilistic DFM Techniques

- For some sources of process parameter variation we can derive a deterministic model
 - E.g. proximity dependent Lgate variation
 - E.g. density-dependent ILD thickness variation
 - For these systematic variation components we can come up with preventive or corrective measures
- For other source of variation, we have no choice but to treat them as random statistical distributions
 - E.g. random remaining Lgate variation
 - Threshold voltage variation
- Statistical treatment of process variation is closely linked with the problem of parametric yield

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Parametric Yield

- Process variation impacts circuit behavior, reduced parametric yield
 - Percentage of chips meeting performance specs
- Need to assess the impact of process variation on circuit behavior
 - What are the important factors / mechanisms
 - Which extraneous factors may 'screen' out the true causes
- Need to model these impacts within the CAD tools
 - Requires accurate physical models
 - Algorithms to work with them

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Circuits Require Smaller Tolerances

- **Smaller tolerance to process variations required**
 - Low-power circuit design
 - Higher operating frequencies
 - Reduced die size
- **Advanced semiconductor manufacturing**
 - Increased process variability
 - More complex variability patterns

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Factors Leading to Circuit Performance (e.g. Timing) Variation

- **Environmental factors**
 - Power -> temperature
 - External temperature
- **Circuit Context**
 - Crosstalk coupling
 - IR drops
- **Process Variation**
 - Device parameter variation
 - Interconnect parameter variation

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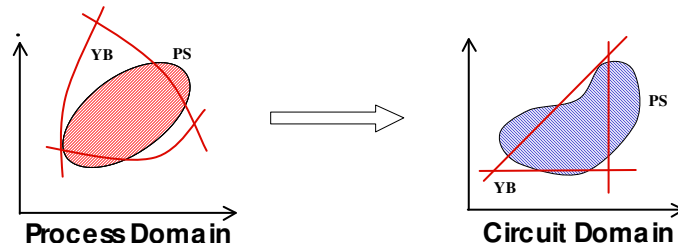
What We Can Do For Parametric Yield

- Analysis techniques for crosstalk-aware timing analysis are available
- Analysis techniques for variation-aware timing analysis are being developed
- Impact of process variation on circuit can be mitigated at
 - Process level
 - Circuit level
 - Need statistical models to link process variation to circuit performance variation

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Parametric Yield Problem

- Parametric yield maximization: max yield of circuits properly operating under variability and uncertainty
- Parametric yield optimization requires
 - Statistical models of key design and process parameters
 - Tools relating circuit performance to sources of variation
 - Methodologies to integrate statistical models and tools
- Statistical modeling: linking process and circuit parameter distributions



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Parametric Yield Problem

- Let $f(x_{proc})$ be *pdf* for process parameters $x_{proc} = \{x_1 \dots x_n\}$
- Let $p_{ckt} = \{p_1 \dots p_m\}$ be circuit parameters of interest
- Design is controlled through design parameters $d = \{d_1 \dots d_l\}$
- Circuit performance *pdf* is then: $f(p_{ckt}, d)$
- Parametric yield of a circuit

$$Y(d) = \int_{yB} f(p_{ckt}, d) dp_{ckt}$$

- Parametric yield optimization maximizes $Y(d)$

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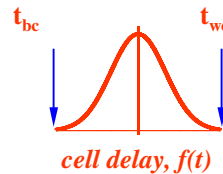
CAD Tools for Parametric Yield?

- Variation-aware timing
- Cross-talk aware timing analyzers

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Impact of Process on Variation on Timing: Probabilistic Nature of Timing

- Gate and wire delay cannot be predicted exactly
 - Process variation
- Gate and wire delays should be modeled as random variables
- Standard approach: gate and wire delays are numbers
 - E.g. cell delay = $[\mu - 3\sigma, \mu + 3\sigma]$



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Deficiencies of Current Approach

- Can't correctly predict parametric yield (speed binning curve)
- May be overly conservative
- Cannot catch timing violations due to un-correlated path delays
 - E.g. Hold time violations due to uncorrelated logic and clock delays
- Roadmap for Semiconductors, 2001:
“Statistical timing analysis tools must comprehend parasitics, delays and geometries that are parameterized as probabilistic distributions”

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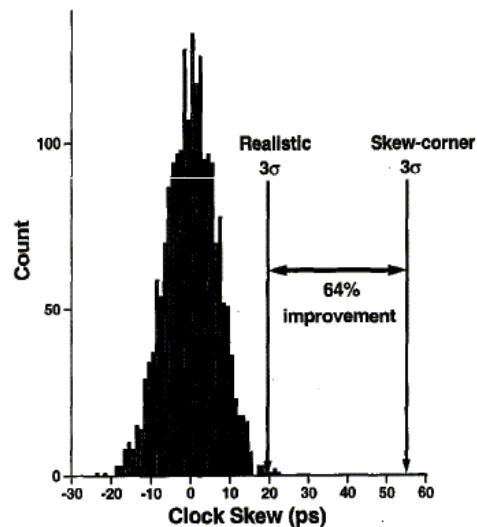
Why We Can't Use Old Approaches: Larger Intra-Chip Variation

- Process variations
 - inter-chip (between chips)
 - intra-chip (within same chip)
- Intra-chip variation becomes significant
 - E.g. in 0.13um CMOS, intra-chip variation of effective transistor length is 35% of total variation
- Affects both transistors and wires
 - Random threshold voltage variation
 - Layout-dependent wire thickness variation

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Worst-Case Analysis is Too Conservative

- Why is traditional worst case approach to timing analysis not feasible?
- Overly conservative



Characterization of Delay Variation

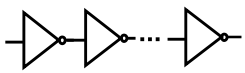
- Process variation leads to variation of circuit performance characteristics
 - Delay
 - Power
- Delay variation
 - **Correlated:** gates, wires, and paths become slower or faster simultaneously
 - **Un-correlated:** some gates or wires are faster, others on the same chip slower
- Correlated delay variation happens if
 - Only inter-chip variation is present, *and*
 - Sensitivities of gate / wire delays to process variation are the same

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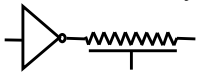
Characterization of Delay Variation

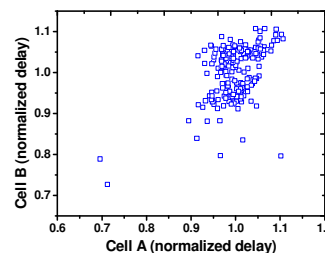
- Different sensitivities lead to un-correlated delay variation *without* intra-chip variation
- Different sensitivities of logic and interconnect

Path 1: Logic heavy path



Path 2: Wire heavy path

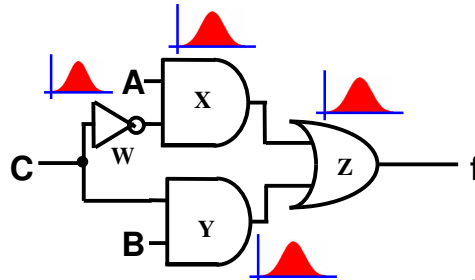

- Different cell sensitivities
 - Latch vs. sense amplifier



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Probabilistic Timing

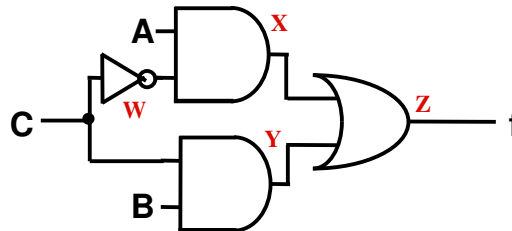
- Standard timing analysis *implicitly assumes* perfect gate and wire delay correlation
 - Only then is analysis with numbers, not random variables, justified
- Gate delays partially correlated
 - **Cannot avoid treating delays as random variables**
- Will find a probabilistic clock cycle distribution
 - To replace worst-case estimates



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Traditional Timing Verification

- Compute longest path on DAG
- E.g. for gate Z, and inputs X and Y



$$\text{Final-Delay}(Z) = \max\{\text{delay}(X), \text{delay}(Y)\} + \text{delay}(Z)$$

- STA requires two algebraic operations on delay
 - Summation of delay
 - Taking maximum
- Taking max allows making a decision as to which path is responsible for longest delay

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Computations with Random Variables

- For numbers, if $\max\{X, Y\} = X$, then
$$\max\{Z + X, Z + Y\} = Z + X$$
- Can define *probabilistic max operator*
$$\max_P(X, Y) = \begin{cases} X, & \text{if } P\{X \geq Y\} \geq P\{X \leq Y\} \\ Y, & \text{if } P\{X \geq Y\} < P\{X \leq Y\} \end{cases}$$
- Then, if $\max_P(X, Y) = X$ it **does not follow** that
$$\max_P\{Z + X, Z + Y\} = Z + X$$
- Why? Because of correlations between X,Y,Z
- Can't use longest path algorithm
 - ⦿ Should consider multiple paths

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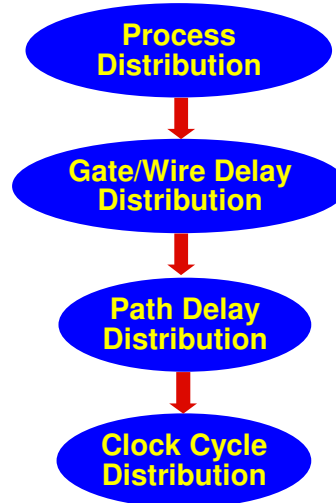
Proposed Probabilistic Framework

- Fully analytical probabilistic computation
- Gate and wire delay correlations taken into account
- Bounds on distribution of probabilistic maximum (clock cycle) derived

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Overview

- Assume distribution of process parameters
- Relate process variation to gate delay response
 - Find gate delay distribution
- Path delay distribution found from gate delays
- Find distribution of clock cycle as max of path delay
$$\max\{D_1 \dots D_N\} \leq T_{\text{clock}}$$



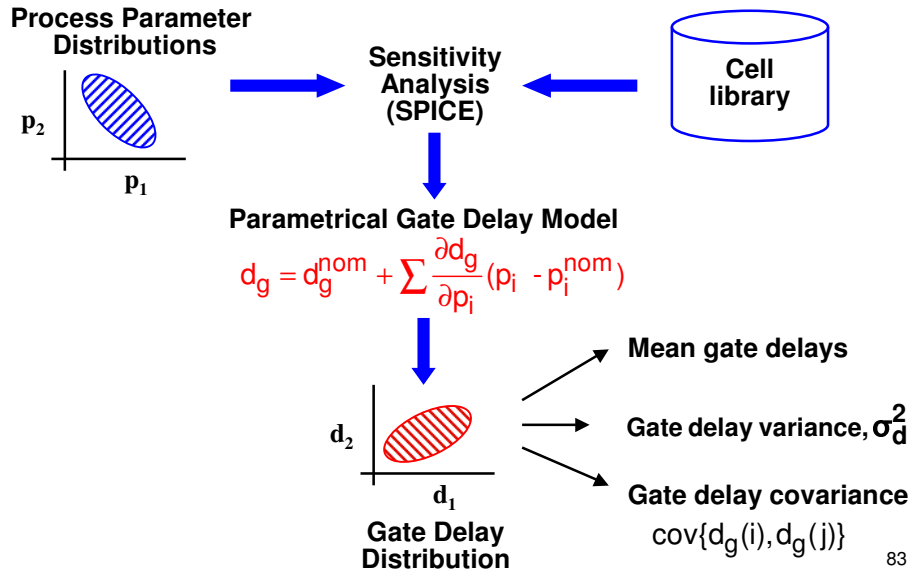
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Probabilistic Timing: Formulation

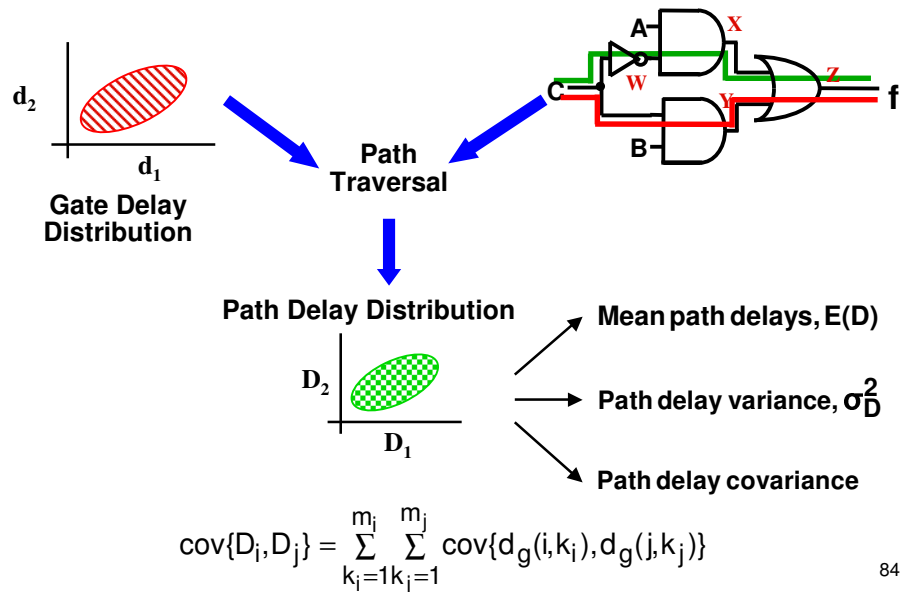
- Consider a combinational netlist with N paths
- Path delays form random vector $D = \{D_1 \dots D_N\}$
where D_i is the delay of the i_{th} path
- The clock cycle is given by
$$\max\{D_1 \dots D_N\} \leq T_{\text{clock}}$$
- Find cumulative probability function of $\max\{D_1 \dots D_N\}$
$$F_{\max}(t) \triangleq P\{\max\{D_1 \dots D_N\} \leq t\}$$
- Assume Gaussian process parameters

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Gate Delay Distribution



Path Delay Distribution



Path Delay Distribution: Example

- Process parameter variation

$$L_{\text{eff}} \sim N(L_0, \sigma_L^2)$$

- Cell sensitivities

$$d_{\text{AND}} = d_{\text{AND}}^{\text{nom}} + \frac{\partial d_{\text{AND}}}{\partial L} (L - L_0)$$

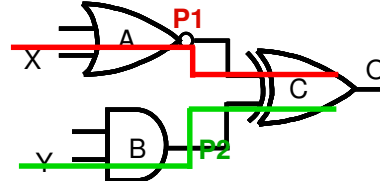
- Gate delay variance: $\text{var}(d_{\text{AND}}) = \left(\frac{\partial d_{\text{AND}}}{\partial L} \right)^2 \sigma_L^2$

- Gate delay covariance: $\text{cov}(d_{\text{AND}}, d_{\text{XOR}}) = \left(\frac{\partial d_{\text{AND}}}{\partial L} \right) \left(\frac{\partial d_{\text{XOR}}}{\partial L} \right) \sigma_L^2$

- Path co-variances

$$\text{var}(D1) = \text{var}(A) + \text{var}(C) + 2 \text{cov}(A, C)$$

$$\text{cov}(D1, D2) = \text{cov}(A, B) + \text{cov}(A, C) + \text{cov}(C, B) + \text{var}(C)$$



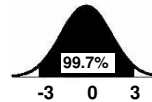
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Clock Period Distribution

- Combining the derived bounds, we can bound $\max\{D\}^k$ at k_{th} percentile of its distribution by

$$T_{\text{clk}}^k = \max\{D\}^k \leq E \max\{D\} + z_k \sigma_{\text{max}}$$

where z_k is value of standard normal at k_{th} percentile

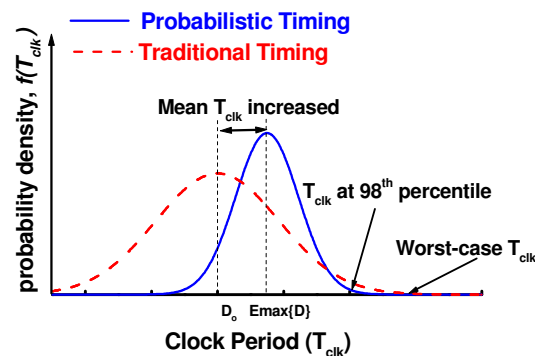


- Example: compare probabilistic T_{clk} estimate with standard analysis
- Best illustrated using a well balanced circuit
 - Many paths with close mean delays
 - Different path correlations

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Clock Period Distribution: Example

- Probabilistic mean T_{clk} is longer than standard estimate
 - Result of taking max of partially correlated path delays
- Spread of probabilistic T_{clk} is tighter
 - Path variance reduction due to partial gate correlation



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Probabilistic STA: Summary

- Timing analysis has to be variation-aware
- An analytical framework for probabilistic timing based on Gaussian process theory
 - Derived analytical bounds on distribution of clock cycle
- Results show that
 - Probabilistic predictions are less conservative
 - Un-correlated path delay variation degrades typical clock period

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Summary: Process Variation and Parametric Yield

- **Process variation increases**
- **Complexity of variation patterns increases (intra-chip)**
- **Sensitivity of circuits to process variation increases**
- **Need variation-aware CAD tools**

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